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Research paper

Estimation of Power for Reversible Subtractors

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Abstract

In recent years Reversible Logic Circuits (RLC) are proved to be more efficient in terms of power dissipation. Hence, most of the researchers developed Reversible logic circuits for low power applications. RLC are designed with the help of Reversible Logic Gates (RLG). Efficiency of the Reversible gates is measured in terms of Quantum cost, gate count, garbage output lines, logic depth and constant inputs. In this paper, measurement of power for RLG is done. Basic RLGs are designed using GDI technology and compared in terms of power dissipation. 1 bit Full subtractor is designed using EVNL gate [1] and also with TG& Fy [6] gates. The power dissipation is compared with 1 bit TR gate [5] full subtractor. Then 2 bit, 4 bit and 8 bit subtractors are designed and compared the powers. Proposed 4 bit and 8 bit full subtractors are dissipating less power when compared to TR gate 4 bit and 8 bit subtractors.

Keywords: Reversible Logic Circuits (RLC), Reversible Logic Gates (RLG), Power Dissipation, Full Subtracto

1. Introduction

Launder's principle states that, Energy E=ST must be emitted into the environment where S is the amount of added entropy. If 1 bit of logical information is lost then the amount of energy that must be emitted to the environment is $E \geq kTln2$. For system where many into one mapping is done, the entropy change occur and heat transfers. For reversible system this heat transfer does not take place according to Bennett theorem since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible logic circuits generate a unique output vector from each input vector and if input vector is interchanged with the output vector then input vector is placed at the output. The major goal in reversible logic design is to minimize the number of reversible logic gates used and garbage outputs produced [3].

The paper is organized as follows: Section 2 gives the power measurement of reversible logic gates. Section 3 deals with the reversible subtractor circuits using EVNL gate, TG & Fy gate and TR gate. These gates are designed with GDI technique and simulated and measured the power. Section 4 describes the performance analysis of reversible subtractors and Section 5 gives conclusion and future scope.

2. Estimation of Power in Reversible Logic Gates:

It is a basic building block to design reversible circuits. A gate is said to be reversible if it is having pairs of input and output ports and input vector can be retrieved from the output vector. According to second law of thermodynamics, no heat transfer takes place by the reversible gates. Hence heat generated by the gate within the system does not affect the neighboring gates within the system and increase the reliability by reducing the overall power dissipation.Table 1 shows power dissipated by basic RLG and number of transistors used. HNG gate and EVNL gate are dissipating more power since they are 4x4 gates and require more transistors for the design. TR gate is dissipating less power when compared to EVNL gate. Since GDI technology is used for the design, buffers are used at the output ports to compensate the voltage swing degradation. Hence, power dissipation increases as port size increases.

Table 1: Comparison of Reversible Logic Gates

S.No	Gate	NxN	No. of Transistors	Power (µW)
1	Fy.Gate	2x2	5	12.387
2	Fredkin	3x3	6	17.21
3	Taffoli	3x3	8	24.528
4	M gate	3x3	14	33.67
5	L gate	3x3	8	19.183
6	BJN	3x3	8	21.504
7	TR gate	3x3	11	34.98
8	Taffoli	4x4	11	34.15
9	HNG	4x4	22	70.401
10	EVNL gate	4x4	22	79.401

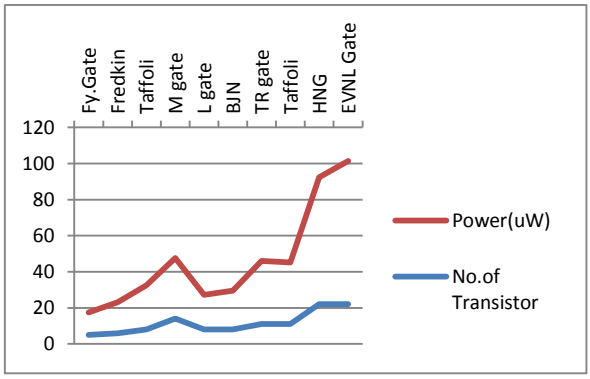


Fig1: Analysis of power for different Reversible Gates

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3. Estimation of power in Reversible Subtractor

Literature on reversible full subtractors is less when compared to the other reversible combinational circuits. TR gate based and EVNL gate based full subtractors [1] are compared with respect to Quantum Cost, number of gates required, constant inputs and garbage outputs. Power measurement is also a major concern for these circuits. In [2] EVNL gate based and conventional full subtractors power was measured and concluded that reversible full subtractor is dissipating less power as bit size is increasing. In this paper we designed full subtractor using TR gate[4], TG & Fy gates and EVNL gate with GDI technique and measured power.

3.1. 1 Bit Subtractor Using Taffoli (TG) and Feyman (Fy)Gates

Taffoli gate is 3x3 gate and Feyman is also 3x3 gate. The fig 2 shows the full subtractor implementation using TG and Fy gates. It require 5 reversible gates, 31 transistors.

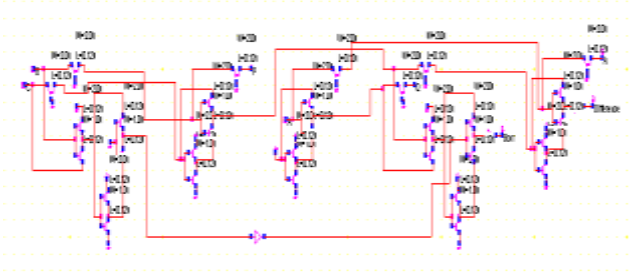


Fig2: Transistor Implementation of TG&Fy 1 bit Full subtractor

3.2. 1 Bit Subtractor Using TR Gate

TR gate is 3x3 reversible gate. Fig 3 shows the full subtractor using TR gate [5]. It requires 2 reversible gates, 22 transistors.

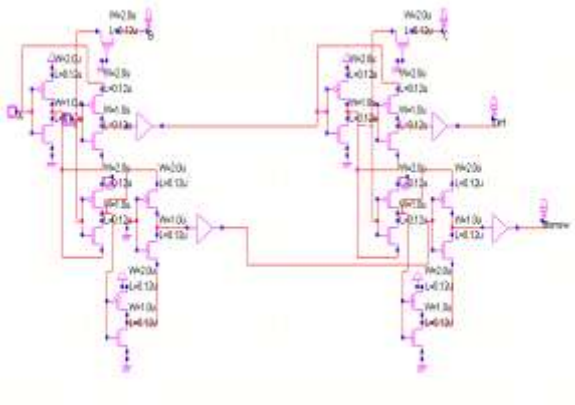


Fig3: Transistor Implementation of TR gate 1 bit Full subtractor

3.3 1 Bit Subtractor Using Proposed EVNL Gate

Proposed gate is 4x4 reversible gate. Fig 4 shows the full subtractor using proposed gate. It requires 1 reversible gate, 24 transistors.

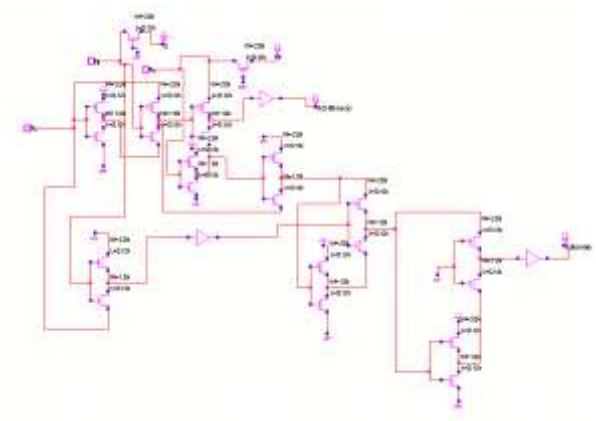


Fig4: Transistor Implementation of EVNL gate 1 bit Full subtractor

4. Result:

Table 2 shows the comparative study of reversible full subtractors with respect to the no. of reversible gates required, no of transistors and power. 1 bit subtractors are dissipating more power when compared to 2 bit because we simulated for all 8 input combinations, hence the dynamic power is more. 2 bit, 4 bit and 8 bit subtractors are simulated for one input combination. TR 1 bit and 2 bit are dissipating less power than the other two but require more reversible gates than the proposed one. Proposed 4 bit and 8 bit subtactors are dissipating less power and require less number of RLG when compared to the other two. Fig 5 to fig 7 shows the simulated waveforms of TR, TG&Fy and EVNL 4 bit subtractors. Fig 8 shows power analysis of TR, TG&Fy and EVNL subtractors, from which it is shown that EVNL subtractor is dissipating less power as the bit size is increasing.

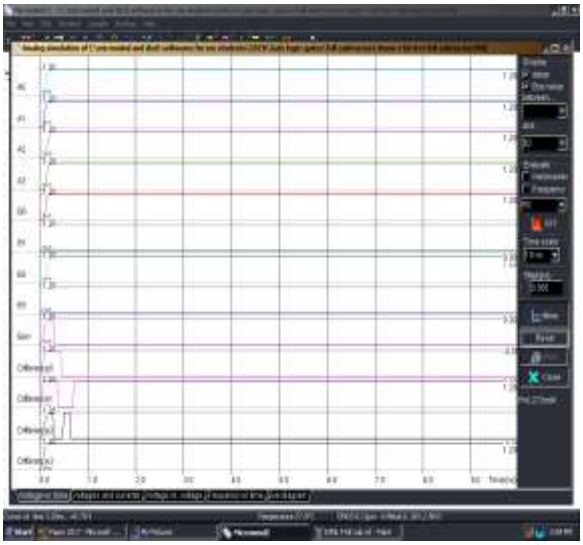


Fig5: TG and Fy gate gate 4 bit subtractor simulated wave form

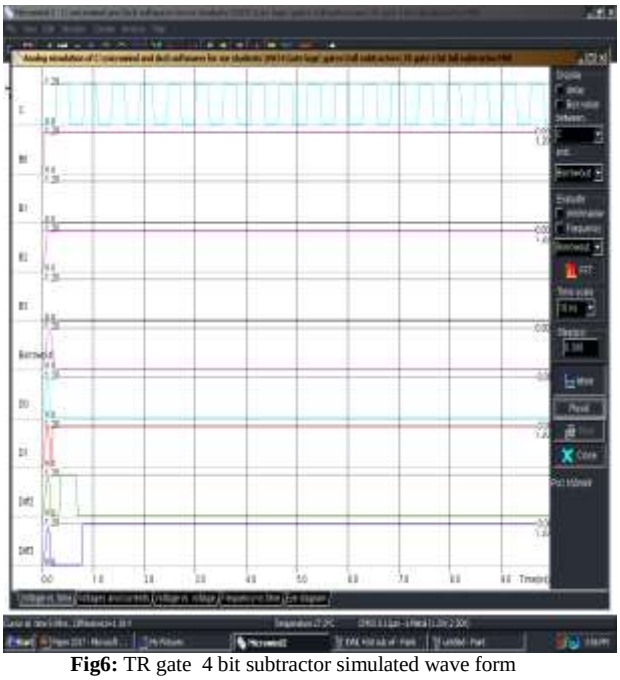


Fig6: TR gate 4 bit subtractor simulated wave form

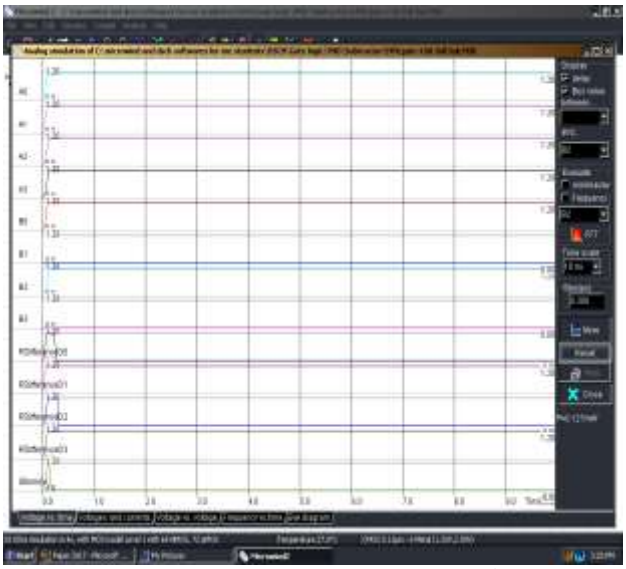


Fig7: EVNL gate 4 bit subtractor simulated wave form

Table 2: Comparison of Reversible Full Subtractors

Full Subtractor	No. of Rev gates	No. of transistors	Power (µW)
TG, FY 1 bit	5	31	103
TR 1 bit	2	22	87.88
EVNL 1 bit	1	24	100
TG, FY 2 bit	10	62	98.5
TR 2 bit	3	33	29.175
EVNL 2 bit	2	48	47.35
TG, Fy 4 bit	15	124	273
TR 4 bit	7	77	165
EVNL 4 bit	4	86	127
TR 8 bit	15	165	330
EVNL 8 bit	8	192	205

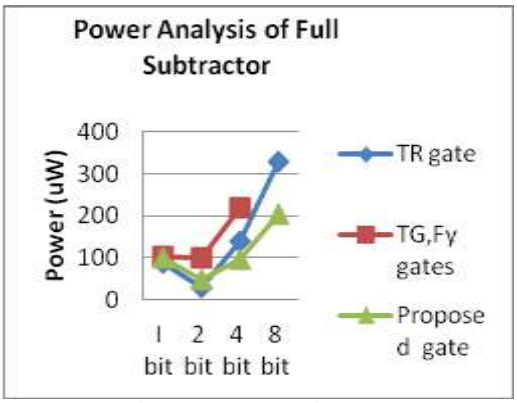


Fig8: Performance Analysis of Reversible Subtractors

5. Conclusion and Future Scope

We concluded that the power dissipated by the proposed gate is more when compared to other gates because it is a 4x4 gate and require more transistors for implementation. Though individual gate is dissipating more power, when it is used as a subtractor it is dissipating less power when compared to the other subtractors for higher order bits with less number of reversible gates. Hence, in the design of higher order subtractors EVNL gate can be used for low power application with minimum number of reversible gates

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