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Research paper

Coplanar Qca Adders for Arithmetic Circuits

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Abstract

A quantum-dot cellular automaton (QCA) is one of the most perspective nanotechnologies for future computing paradigm. We propose low complexity QCA adders for arithmetic circuit design. The proposed majority-gate based full adder is coplanar layout, and on the basis of clock-phase crossover technique. The results of the proposed structures from the QCA simulator tool are analyzed and compared with previous works.

Keywords:QCA technology, half adder, full adder.

1. Introduction

The next stage in computer production is nanoelectronic technology. The ITRS report highlights the results of future possible design technologies, like quantum-dot cellular automata (QCA), tunneling phase logic (TPL), single electron tunneling (SET), and carbon nanotube (CNT). One of the promising nanoelectronic technologies is QCA.

QCA also offers a new way in the computation of information. In QCA, the cell connects two free electrons, and the logical values '0', '1' depend on the position of the electrons inside the quantum dot cell, which are due to the Coulomb force. Changing the logic value from '1' to '0' does not lead to the discharge of the capacitor, unlike the usual CMOS [1-3].

In this paper, we propose the QCA design of coplanar half and full adders, which are used to implement arithmetic circuit design. The purpose of this work is to develop the design of coplanar adder due to its high scalability.

2. Related Works

2.1. Quantum-dot Cellular Automata

This section focuses on a brief explanation of QCA. This technology is based on interaction of quantum cells. The cells are in square forms and have four quantum dots along with two mobile electrons, as shown in Fig. 1(a). There are two positions in each QCA cell which can encode the binary information. Designers can be able to create any functions using the majority and inverter gates. The inverter is shown in Fig. 1(b). The majority gate is composed of five cells as illustrated in Fig. 1(c). Logic AND gate or OR gate areimplemented using majority gate by fixing one of three inputs to -1 or +1, respectively.

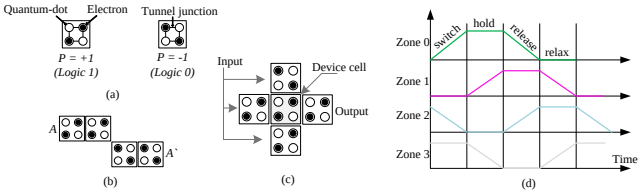


Figure 1:. QCA elements: (a) QCA cell, (d) inverter, (c) Majority gate (Maj3), (d) QCA clocking.

In QCA circuits a clock is required to supply the power gain for the cells and control the data flow. It has four phases; Relax, Switch, Hold and Release; as shown in Fig. 1(d). Also, there is issue with crossing the wire in QCA technology, and different available cross-wiring techniques, such as: coplanar and multilayer [1-5].

2.2. QCA Adders

Arithmetic operations: addition, subtraction, multiplication and division are realized using an adder schemes. There are adder schemes: a half adder and full adder. The half adder is a circuit that has two inputs (A, B) and two outputs (Sum and C_{out}), and defined as follows:

$$C_{out} = Maj_3(A, B, 0); \quad (1)$$

$$Sum = XOR(A, B); \quad (2)$$

The full adder is implemented from two half adders and composed of three input lines (A, B and C_{in}) and two output lines ($Sum$and C_{out}). The expression of the result in QCA using Maj3 gate is defined as follows:

$$C_{out} = Maj_3(A, B, C_{in}); \quad (3)$$

$$\backslash Sum = Maj_3\big(Maj_3\big(A, \overline{B}, C_{in}\big), Maj_3\big(A, B, \overline{C_{in}}\big), Maj_3\big(\overline{A}, B, C_{in}\big)\big); \quad (4)$$

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After the proposed a majority gate with five entrances, the QCA full adder was proposed based on that majority gate (Maj5). It has some advantages for designing stacking structures with low complexity. In fact, an effective implementation of 3-input exclusive-OR (XOR) gates and 5-input majority gates can improve the implementation of the QCA full adder.

3. The Proposed Adders

We introduce a new design of QCA half and full adders. The half adder consists of two components: QCA exclusive-*OR* gate [2] and 3-input majority gate units without crossover as shown in Fig. 2. We set the QCA fixed cell (logic '0') for both units (Maj_3 and *XOR*) for being compact circuit. Fig.3 shows the majority gate based proposed full adder using QCA clock-phase crossover, and defined as follows:

$$Sum = Maj_3\left(Maj_3\left(A, B, \overline{C_{in}}\right), \overline{Maj_3(A, B, C_{in})}, C_{in}\right); \quad (5)$$

Note that C_{out} is implemented using only one Maj_3. Implementation of thefull adder consists of 57 quantum cells with one clock cycle delay. The proposed low complexity adders are more compact and suitable for designing arithmetic circuit, especially for implementing QCA incrementer and decrementer with high performance.

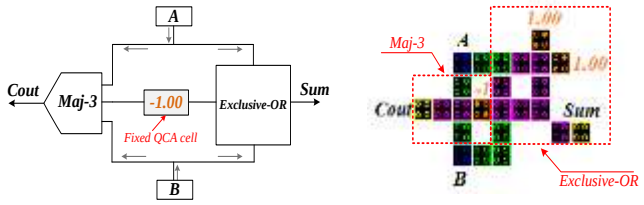


Figure 2:. Block diagram and QCA design of the proposed half adder.

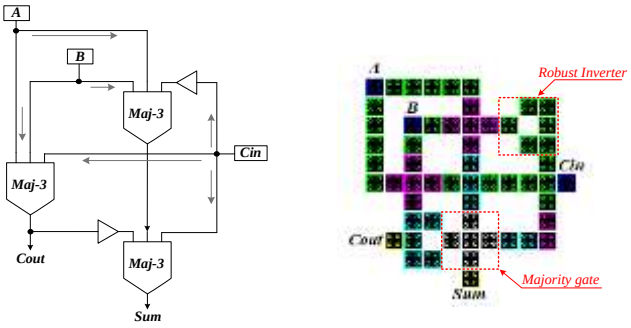


Figure 3:. Block diagram and QCA design of the proposed full adder.

4. Analyzing and Future Work

The functionality of the presented designs is conducted using QCADesigner tool (version 2.0.3) which is accurate simulation tool for designing QCA circuits. The simulation result of the full adder is given in Fig.4. It confirms that the result of the full adder is correct and stable.

Table 1 shows a comparison among the proposed designs and previous designs in terms of cell count, area and latency aspects. The table confirms that the proposed adders have achieved significantly over the previous works. In contrast, our full adder occupies almost half area compare to other full adders. Hence, this advantageous can give us significant improvements to design QCA arithmetic circuitswith low area. We will demonstrate the effective methodology of incrementer and decrementer with optimized delay in our further work.

Table 1. Comparison of QCA adders

	Circuits	Cell count	Total area (μm^2)	Latency
Full Adders	[5]	82	0.07	1.00
	[4]	73	0.08	1.00
	[3]	69	0.07	1.00
	Proposed design	57	0.04	1.00
Half adder	Proposed design	24	0.02	0.50

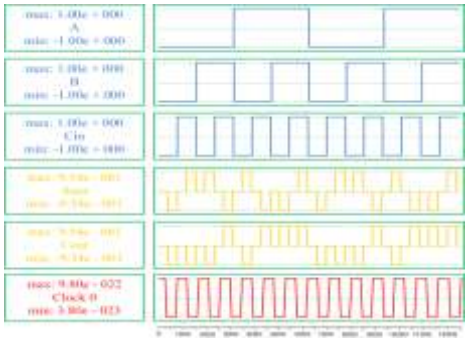


Figure 4:. Simulation result of the proposed full adder in QCA.

Acknowledgment

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References

[1] N. Safoev and J. C. Jeon, Cell Interaction Based QCA Multiplexer for Complex Circuit Design, J. Advanced Science Lett. 23 (2017), 10097-10101.
[2] A. M. Chabi et al., Towards ultra-efficient QCA reversible circuits, Microprocessors and Microsystems. 49 (2017), 127-138.
[3] M. Kianpour, R. S. Nadooshan and K. Navi, A novel design of 8-bit adder/subtractor by quantum-dot cellular automata, J. Computer and System Sciences. 80 (2014), 1404-1414.
[4] H. Cho and E. E. Swartzlander, Adder and multiplier design in quantum-dot cellular automata, IEEE Transactions on Computers. 58 (2009), 721-727.
[5] A. Chudasama, T. N. Sasamal and J. Yadav, An efficient design of Vedic multiplier using ripple carry adder in Quantum-dot Cellular Automata, Comp. and Elec. Engineering. 65 (2017), 527-542.