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Research paper

Low Power Clock Gated Delay Buffers

1M. Maria Dominic Savio, 2Anudeep Bonasu , 3Sanjeevan Goswami , 4K N S Reshma

*[1]*Department of Electronics and Communication Engineering SRM Institute of Science and Technology, Kattankulathur, Chennai, India*
**Corresponding author E-mail: [1]mariadominicsavio.m@ktr.srmuniv.ac.in , [2]anudeepbonasu97@gmail.com ,*
[3]goswamisanjeevan6@gmail.com , [4]reshmarao1998@gmail.com

Abstract

Power efficiency is the most important factor in todays electronics. The other factors that are also considered to determine the standard of electronic products are area and speed. Industries are competing to develop products of lesser power consumption, smaller size and faster speed. Though, clubbing all the three factors has not been possible till date, researchers are trying to infuse any of the two factors in todays electronic products. Thus, the idea of reducing power consumption and area in an SRAM based Delay Buffer came up. Portable devices have the requirement of delay buffer when transmitter and receiver work in different frequencies. Existing Delay Buffers use quad gated clock tree ring counter with three levels of gating of the master clock. A SRAM Delay Buffer has been designed with octa and octaX2 gated clock and a clock synchronizer called ADPLL. Clock gating is a technique which limits the clock for idle Memory units. Findings: The Delay buffers were normally designed with quad gated clock tree distribution. The proposed work shows that the octa and octaX2 gated Delay buffers added with ADPLL adjust the frequency dynamically in run time between transmitter and receiver to achieve low power. The simulation result shows great improvement in power consumption. A 64 x 8 buffer is designed with both octa and octaX2 clock gating, and then the simulation result is compared with quad gated existing delay buffer. The simulation is done using Modelsim 6.6d and power analysis is done both in Altera Quartus and Cadence. Application: Wherever the minimum power is required the follwing buffers are used in any SOC(system-on-chip) application.

Keywords :*Clock Gating , synchronizer , ADPLL ,Ring counter, DET-Dual Edge trigger Flip-flop, DCO-Digital Control Oscillator*

1. Introduction

In today's electronics, delay buffer plays a crucial role when data is shifted from one memory array or processor (sender) to another memory array or processor (receiver). SRAM are used to implement this delay buffer when control and addressing line is added. Recently three primary technologies have been used in building memory hierarchies. Main memory uses Dynamic Random Access Memory (DRAM), whereas cache uses SRAM. Even though DRAM is slower, it is costly then SRAM, because less area is used by DRAM. Buffers are created with different method. If the buffer length is shorter SISO shift register is used for addressing the memory. Since, 64*8 memory is a long buffer memory, it has been implemented using ring counter method for the address generation process. Then the ring counter is modified with octa and octaX2 gated clock forreducing power consumption. In this paper the proposed SRAM with the base of ring counter and ADPLL technique is to be employed. ADPLL will reduce the size of buffer by tuning the transmitter clock frequency in reference with receiver clock frequency.

2. Various Buffer Architecture

A First In First out (FIFO) circuit is constructed by a flip-flop is the simplest way to address the memory in the buffers. The length of the FIFO is taken according to the level of frequency difference in transmitter and receiver.

2.1. Clock Gated Synchronizer

The flip-flop present in FIFO is activated through clock pulses. So the clock pulses have distributed to the entire span of addressing circuit and all the flip-flops are activated with clock at all the time. But a single bit '1' is passed to entire FIFO where the memory unit has to be activated. The clock gating technique has to be implemented so as to reduce the power consumed by clock. Moreover, in FIFO repeatedly we have to pass the bit '1'. To overcome this complication the ring counter is used. Here 64-bit ring counter is employed to generate the addressing scheme for 64*8 memories. This ring counter is used to address the memory with different width but length should be identical. The dual edge trigger (DET) flip-flop is used in ring counter to reduce the clock cycle frequency to half. The 64 bit ring counter is divided into 8 blocks (octa) and 4 blocks (octaX2). Each block consists of 8 DETs and 16 DETs respectively. The Master clock is distributed to all blocks through gated clock logic. The clock gating is done with help of C-element. The C-element consists of two input and one output. It reaches the ON state from OFF when both inputs are logic '1' and again it falls to OFF state until both inputs reach to logic '0' and the output equation is given as

$$C^{NS} = AB + AC + BC \tag{1}$$

Where NS-Next State. This behaviour is useful to construct the ring counter with gated clock. The figure 1.shows the architecture of clock gated ring counter.

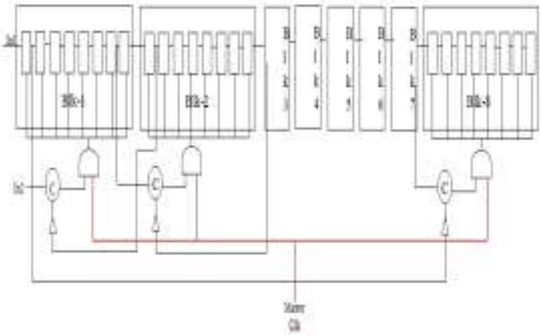
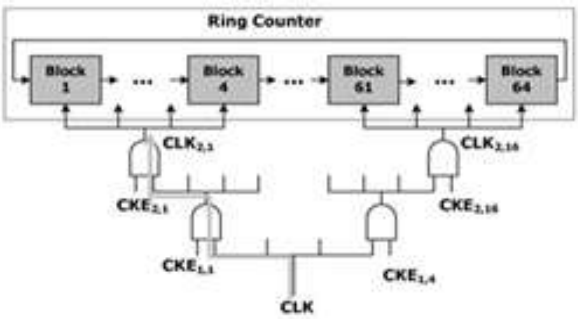
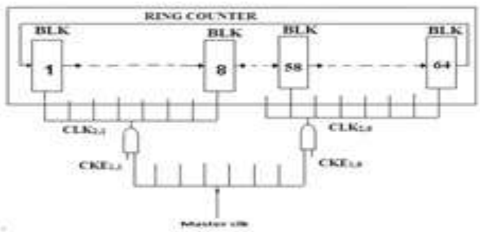


Fig 1: Ring counter gated by octa tree

In this diagram in1 and in2 are initializing inputs. It should be given as '1' only in first clock cycle then resetting all the DETs makes all the inverter to logic '1' as shown in the structure. In this case the first block C-element gets ON and Master clock is supplied only for the first block. When the in1 is shifted to 7th flip-flop(in case of octa tree) or to 15th flip-flop(in case of octaX2 tree), the 2nd block C-element gets ON so the shifting variable successfully transmitted to 2nd block. Now, when the shifting variable crosses the first flip-flop in the 2nd block, it switches OFF the first C-element. As we clock is supplied through clock tree distribution method. In earlier research quad tree distribution is implemented while in the proposed method Octa and OctaX2 tree distribution is implemented and the structure shown in the figure 2.



(a)



(b)

Fig 2: (a) Quad tree distribution (b) Octree Clock distribution

Here, for octatree clock, Master clock node is divided into 8 leaf nodes and this 8 leaf nodes are further divided into 8 nodes and this moves on level by level. But, for octaX2 clock tree, Master clock node is divided into 4 leaf nodes and this 4 leaf nodes are further divided into 16 nodes each. The clock gating can be done for single stage or multi stage depends on the trade-off between area and power. To reduce power consumption single stage of clock gating is simulated and synthesised. Next, the data path for input data byte is perfectly routed to active memory element activated by address generator. By collecting signal from different levels of ring counter and given to OR gate, then OR gate output drives the different level data path through tri-state inverter.

2.2. ADPLL

All Digital phase lock loop (ADPLL) is a normal PLL circuit with the advent that it locks the clock pulses .We track the phase as well as frequency in ADPLL. ADPLL uses DCO instead of VCO in PLL. Where VCO produces a low to high frequency oscillation in variance with analog input voltage, but in DCO the input is a signed binary number. The block diagram of ADPLL is shown in figure 3.

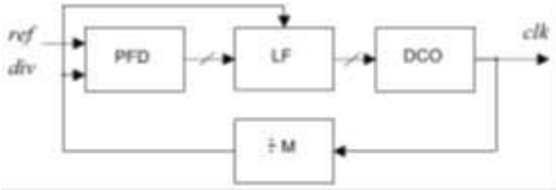


Figure 3: Block Diagram of ADPLL

A phase-frequency detector, a LF (Loop Filter), a digitally controlled oscillator (DCO) and a frequency divider (÷ M) are included as the components of ADPLL The signed binary code developed by Phase –frequency detector (PSD) in variation with transmitter clock to receiver clock. In order to diminish the noise level and to eliminate the high-frequency components the produced code which is processed by a low-pass filter, controls the DCO. The frequency divider is introduced since the clock frequencies exceed the limits of the operational frequency of digital circuits. In the current case the divide factor (M) is set to be 4. As a result, the operational frequency of the LF is 250 MHz rather than 1 GHz.

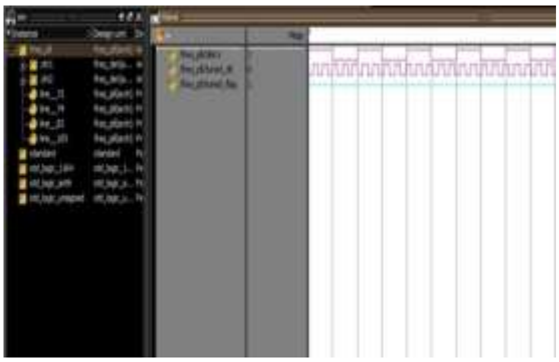
3. Buffers with Adpll

The clock gated buffer implemented in FPGA has the limitation that the length of the buffer should be large otherwise data gets wasted. Instead of increasing the buffer length the method of incorporating ADPLL with transmitter and receiver reduce both area and power. The ADPLL tunes the transmitter frequency in reference with receiver frequency if transmitter frequency five times faster than receiver frequency then transmitter frequency gets matched with receiver frequency in 16.9 ns, until tuning is over and buffer retains the data. Once tuning is done it sets tuned flag and transmission starts.

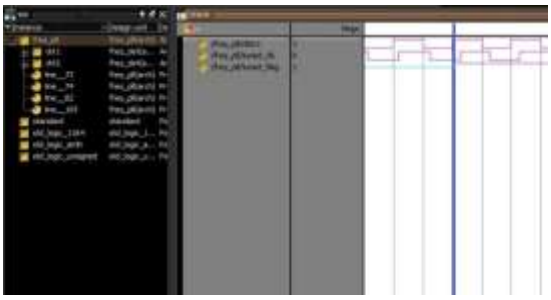
4. Results

Functional verification for every modules is simulated in modelsim and power analysis has been done in Altera Quartus, more over RTL schematic also captured from Quartus.

ADPLL clock tuning simulation for scenario of 16.9 ns shown in figure 4. Here the figure 4. (a) Shows initial simulation time of tuning. Figure 4. (b) Shows both the clock gets locked in 16.9 ns.

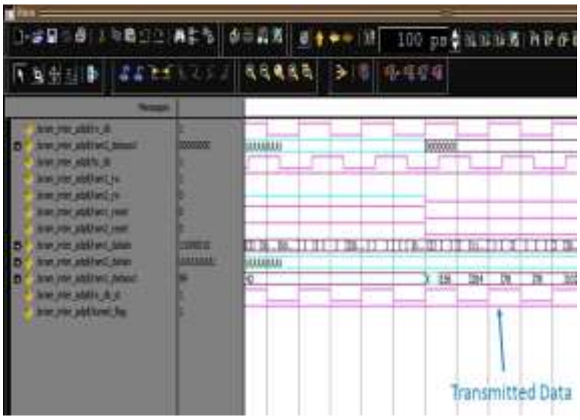


(a)



(b)

Figure 4: (a) Initial tuning (b) Tuned flag set in 16.9ns.



(a)

(b)

Figure 5: (a) Transmitted data (b) Received data

Transmitter data which the system delivered and in receiver the same data appears without loss through implementation ADPLL shown in figure 5.

RTL Schematic proposed System as shown in figure 6.

Figure 6. RTL View of Buffer with ADPLL.

Power analysis of all the three tree structures (quad, octa and octaX2) done in Cadence is shown in Table 1

Table 1: Power analysis of all three tree structures

S.No	Structure	Quad(mV)	Octree(mV)
1	Clock Tree	33.2	31.05
2	Input driver Tree	143	93.31
3	Output driver tree	94.94	92.72

The power analysis in done in Quartus Tool, table 2 shows power difference between quad and octree buffer.

Table 2: Power analysis of Quad and Octa tree

	Quad Tree	Octa Tree	OctaX2 Tree
Power (nW)	657496.525	675477.417	604661.482
Area (cells)	652	372	140

The power analysis of buffer with and without ADPLL is tabulated in table 2.

Table 3: Power consumption Buffer

S.No	Structure	Power consumption (mV)
1	Buffer	31.29
2	Buffer with ADPLL	29.99

5. Conclusion

A design of frequency synthesizer for adaptable input frequency adjusting is designed as a ADPLL logic circuit. A clock divider with a frequency counter is employed to detect the input frequency changes and to adapt its own frequency with respect to input fluctuations. A transceiver network circuit in which ADPLL is present at both ends for parallel duplex transmission. The timing and power level synthesised output are obtained using Quartus II synthesizer and behavioural verification of the logic circuit is verified using Modelsim tool.

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