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Research paper



High performance multilayer transformer for RF applications

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Abstract

In this paper, multilayer on-chip transformer is proposed to enhance the operation of device in terms of primary quality factor, primary inductance, coupling coefficient and self-resonant frequency. Multilayer transformer is designed by considering the multilevel fabrication concept in RF-VLSI. The demand for miniature on-chip passive components is increased due to the advancement in RF-VLSI design process. The proposed multilayer on-chip transformer is simulated using High Frequency Structural Simulator and the results are compared with conventional planar transformer. The proposed multilayer transformer shows 40% improvement in terms of primary quality factor, 15% improvement in terms of primary inductance and 20% improvement in terms of coupling coefficient when compared to conventional planar transformer. Proposed transformer performance is validated by scaling up the dimensions of transformer from µm scale to mm scale and fabricating the transformer on FR4 substrate using PCB fabrication techniques. Measurements of fabricated transformer are carried out using vector network analyser 8719A. Simulated results and experimental results are in good agreement in terms of quality factor, inductance and coupling coefficient. The proposed multilayer transformer is designed using 0.18 µm RF-VLSI technology and has an on-chip area of 100-µm × 100 µm making it compatible for RF integrated circuit (RFIC).

Keywords: *Coupling Coefficient; Inductance; on-Chip Inductor; Quality Factor; RFICS.*

1. Introduction

In recent trends, the demand for silicon based on chip passive components is increased in RF integrated circuits due to the development in integration mechanism of devices, effective fabrication cost and rapid market growth [1]. In literature, different transformer architectures are proposed using thin-film magnetic cores, monolithic materials and commercial CMOS devices. These transformers have variable inductance and low parasitic capacitance value which limits its performance in RF impedance matching circuits and in signal conversion techniques [2]. In addition to architectures another main parameter to be considered for the design of transformer is losses in core which degrades its performance greatly. Skin effect and proximity effect are the two lossy parameters that are considered generally while analysing transformer performance. Skin effect can be reduced by increasing outer diameter of the device and proximity effect can be reduced by increasing width of conductor [3]. But, to increase the frequency range of operation of transformer we have to minimize the on-chip area of the device. Thick substrate and high conductivity material is used as an alternative mechanism to reduce skin and proximity effect on the device respectively.

On-chip area of device is miniaturized to µm-scale, so the parameters extraction of on-chip transformer is frequency dependent. Semi-analytical extraction mechanism can be used to obtain figures-of-merit of on-chip transformer developed based on s-parameters. This analysis is validated up to GHz frequency range to extract transformer parameters [4]. Lumped circuit model is considered for obtaining inductive coupling, quality factor (Q-factor) and parasitic values which is operating at higher order frequencies. This efficient analysis leads to get good agreement between measured and simulated results of on-chip transformers [5]. On-chip transformers are widely used in RF circuits as matching circuits, in LNA's and in broadband amplifiers. Turns ratio of the transformer is to be chosen according to type of application which may be step up, step down or centre tapped [6] [7]. Symmetric and asymmetric layout transformer are considered to obtain same or different primary and secondary quality factor respectively. Symmetric transformer architecture is considered in the presented design. Proposed on-chip multilayer transformer is designed and simulated in High Frequency Structural Simulator (HFSS) in µm scale. The area occupied by the proposed transformer is 100 µm×100 µm which is suitable for RFIC design. Due to fabrication difficulties at µm scale, the proposed multilayer transformer is fabricated on FR4 material using PCB fabrication in mm scale to validate the simulation results. Section II comprises of detailed explanation of multilayer transformer, Section III discusses briefly about results and comparison and section IV is conclusion.

2. Multilayer transformer

Basically, there are two types of on-chip transformer presented in literature- Active transformers and Spiral transformers. CMOS active transformers mainly consists of MOS transistors and the performance of device in the specified frequency range is quite inductive with signal swing [8]. Active inductors suffers with high noise level and low linearity. Spiral transformers offers high linearity and low noise but its performance is greatly affected by its physical geometry. The main drawbacks are low Q-factor, low Self-resonating frequency, low inductance and large silicon area. The proposed architecture is designed in order to improve the performance of spiral transformer in terms of Q-factor, Inductance, coupling coefficient and frequency of operation. Quality factor of the device is increased by considering high substrate thickness and high conductivity material like copper. This consideration decreases losses in the device

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and improves quality factor. Multilayer design is considered for the improvement of inductance by increasing distance between opposite current carrying conductors such that reducing negative mutual inductance of the device. The structure of proposed transformer is shown in Figure 1. Two different colours indicates primary and secondary windings of a transformer. Based on number of turns of the conductors we define turns ratio. The number of turns of transformer shown in Figure 1 is 1.5. So, the turn's ratio of transformer is 1.5:1.5. The 3-D view of the transformer is shown in Figure 2.

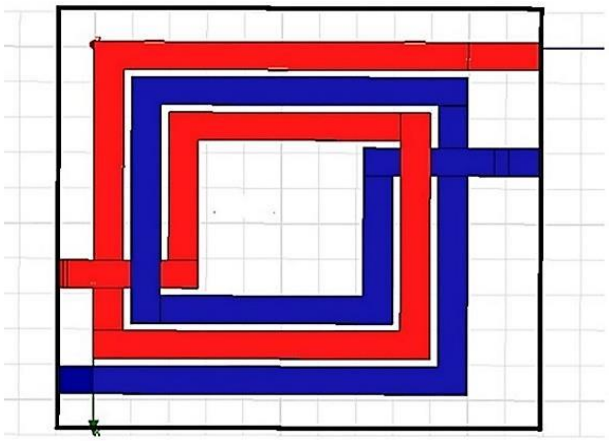


Fig. 1: Top View of 3-D Transformer with 1.5:1.5 Turn Ratio.

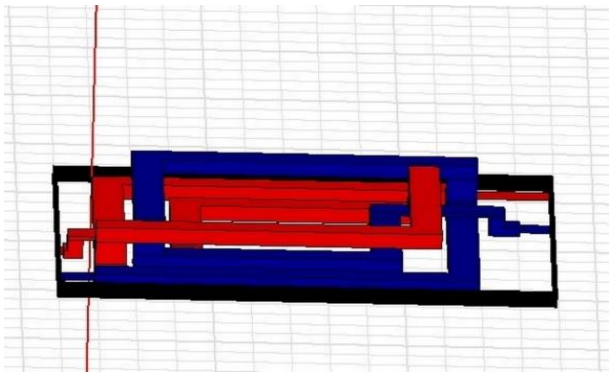


Fig. 2: 3-D View of 3-D Transformer with 1.5:1.5 Turn Ratio.

The construction of transformer is, each half turn of conductor in a transformer of primary and secondary windings is placed in two different layers and the conductors are connected through vias. As the number of turns of primary and secondary windings are same, the proposed transformer is a symmetric type. Due to this type, the primary and secondary Q-factor and inductance values of the presented transformer are same.

3. Results & discussion

Multilayer On-chip transformer design and analysis is carried out in High Frequency Structural Simulator (HFSS) as a four port device, using hybrid lumped model for parameter extraction. Proposed multilayer transformer layout parameters are analysed in terms of Primary Quality factor, Primary Inductance, Coupling coefficient and its performance is compared with existing planar transformer. From the results as shown in Figure 3, Figure 4 and Figure 5, it is observed that 3-D transformer shows a maximum of 40% improvement in terms of Q-factor, 15% improvement in terms of Inductance and 20% improvement in terms of Coupling Coefficient when compared to reported planar transformer. From the result as shown in Figure 4, the proposed multilayer transformer has a self-resonant frequency at 80 GHz and shows 45.4% improvement when compared to reported planar transformer. Proposed transformer is a reliable model for the use as integrated transformer in industrial applications. The values of primary and secondary inductance is in order of nH and coupling coefficient k is <1. The expressions [1] to [3] are used for obtaining figures-of-merit of multilayer transformer [3],

$$\text{Primary Quality factor}(Q_p) = \frac{\text{Im}\{Y_{11}\}}{\text{Re}\{Y_{11}\}} \quad (1)$$

$$\text{Primary Inductance}(L_p) = \frac{\text{Im}\{Y_{11}\}}{2*\pi*f} \quad (2)$$

$$\text{Coupling Coefficient}(k) = \sqrt{\frac{Z_{12}Z_{21}}{Z_{11}Z_{12}}} \quad (3)$$

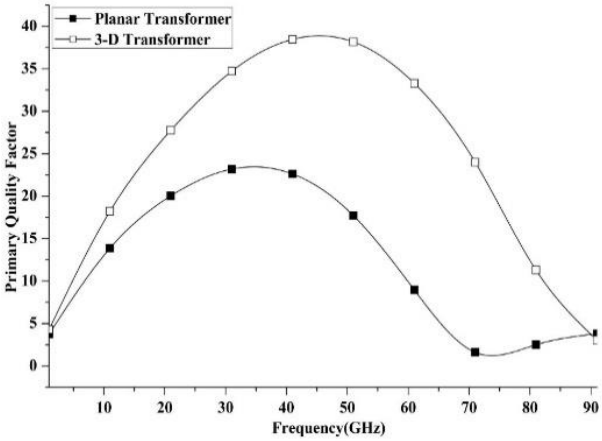


Fig. 3: Comparison of Transformer in Terms of Q-Factor.

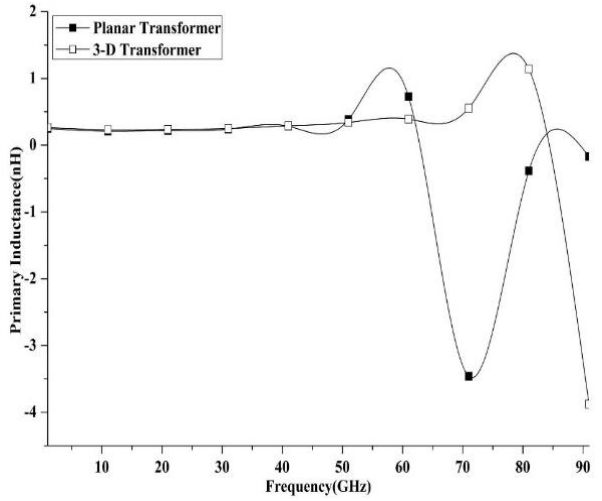


Fig. 4: Comparison of Transformer in Terms of Inductance.

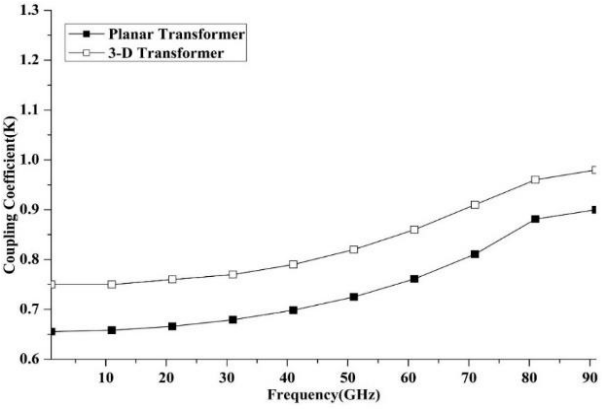


Fig. 5: Comparison of Transformer In Terms of Coupling Coefficient.

3.1. PCB based multilayer transformer

Fabrication of an on-chip multilayer transformer in micrometre scale is bit difficult, so the proposed model is validated experimentally by fabricating multilayer transformer on PCB with area of 1.5

mm × 1.5 mm. FR4 material is used for fabricating the transformer, dielectric value of material is 4.4 and thickness is 1.6 mm. Multilayer transformer fabricated on FR4 substrate is shown in Figure 6. Experimental setup of the fabricated transformer is shown in Figure 7. Device performance is analysed by using vector network analyser (8719A) of frequency range from 0.5 GHz to 13.5 GHz. From the results as shown in Figure 8, Figure 9 and Figure 10, it is observed that simulated results obtained from HFSS and measured results from VNA are in good agreement with each other. Hence, based on the above results proposed multilayer transformer simulation results can also be validated at high frequencies, if fabricated.

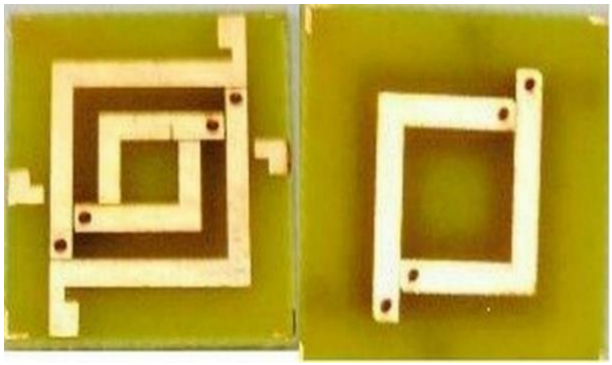


Fig. 6: Fabricated Multilayer Transformer on FR 4(Top and Bottom Layers).

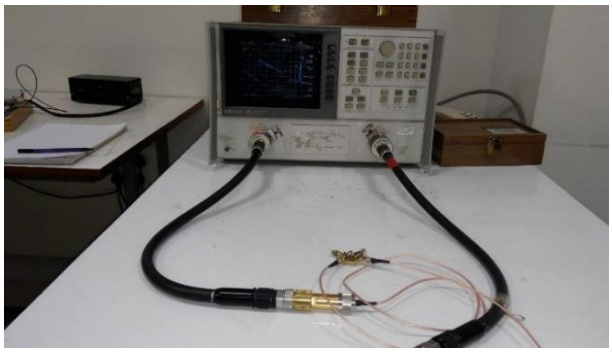


Fig. 7: Experimental Setup of Multilayer Transformer Using VNA.

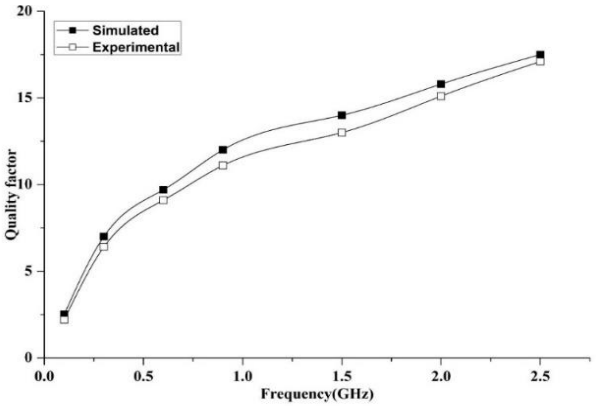


Fig. 8: Comparison of Simulated and Experimental-Q Values.

The performance parameters of proposed multilayer transformer is compared with existing structures in terms of primary inductance (Lp-nH), primary Q-factor (Qp), coupling coefficient (k), self-resonant frequency (SRF) and area (µm2) are reported in Table 1. From the Table 1, it is observed that the proposed structure shows better performance in terms of Lp, Qp, SRF and area. As the coupling coefficient of the transformer is high, so the presented transformer has better performance in matching circuits and it is operated at 80 GHz.

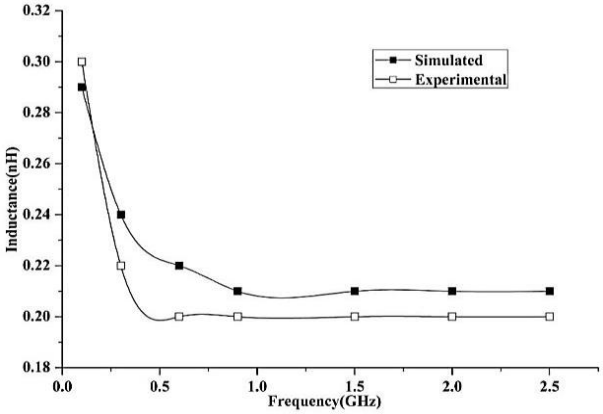


Fig. 9: Comparison of Simulated and Experimental-L Values.

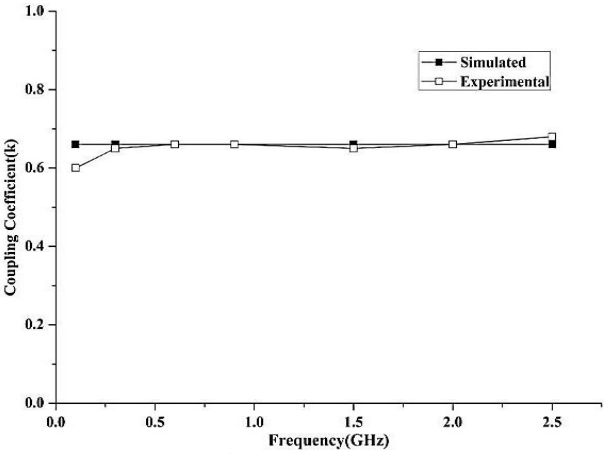


Fig. 10: Comparison of Simulated and Experimental-K Values.

Table 1: Comparison of Transformer Performance

Ref	Type	L_p(nH)	Q_p	k	SRF	Area(µm2)
[2]	Solenoid	175	16	0.96	100 MHz	712*2286
[6]	Solenoid	1.5	14	0.65	3 MHz	----
[8]	Spiral	88	5.9	0.98	20 MHz	----
Proposed Work	Spiral	1.8	38	0.99	80 GHz	100*100

4. Conclusion

On-chip multilayer transformer with enhanced performance in terms of quality factor, inductance, coupling coefficient and self-resonant frequency is presented. Proposed transformer shows 40% improvement in terms of quality factor, 15% improvement in terms of inductance and 20% improvement in terms of coupling coefficient when compared to conventional planar transformer. Proposed transformer model is scaled up to mm scale to validate the results experimentally. There is a good agreement between measured results of PCB transformer and simulated results in HFSS. Hence, the proposed model can also be validated at µm scale, if fabrication is made possible. On-chip area occupied by the presented multilayer transformer is 100 µm×100 µm, suitable for RFIC applications.

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