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Research paper

Power analysis of single precision floating point multiplication using Vedic with proposed techniques

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Abstract

In design of arithmetic circuits low power consumption is one of the basic requirements in recent years. The speed of the device depends on the supply voltage degradation. In this work, a floating-point multiplication for single precision numbers using vedic with different existing techniques like full adder, 4x1 multiplexer, 3:2 compressors and proposed techniques such as modified 2x1 multiplexer moel1 and model2, modified 4:2 compressor logics XOR-MUX and XNOR-XOR-MUX logics are analyzed. The main block involved in the implementation of floating-point multiplication is 24-bit mantissa multiplier block. Further, the optimized techniques are introduced multiplier block to reduce the power dissipation. The proposed techniques such as 2x1 multiplexers, 3:2 compressor with XOR-MUX and XNOR-XOR-MUX logics and 4:2 compressor with XOR-MUX and XNOR-XOR-MUX logics for single precision floating-point multiplication provides better solution in terms of power related issues. The power analysis of single precision floating point multiplication is done and compared with the existing and modified. in terms of Power. Further, the performance metrics of vedic multiplier are analyzed for both existing and proposed techniques are compared. These floating point modules are programmed using Verilog and synthesized using Xilinx Vivado Simulator. From the simulation results, it is concluded that 4:2 compressor with XNOR-XOR-Mux logic achieves better response in terms of power.

Keywords: *Vedic; Compressor; Multiplexer; Verilog.*

1. Introduction

In many applications, floating point arithmetic operations are mostly used, especially in numerical processing and signal processing applications. The IEEE defines the standard [1] for different floating-point formats like single-precision and double-precision. To improve the performance in any digital system, the multiplication is the core operation among all the floating-point arithmetic operations. Hence, an efficient implementation of floating-point multipliers is the major concern.
Floating point arithmetic solves these two problems at the expense of accuracy. The decimal point placement can float relative to the significant digits of the number. From last few decades, a lot of work has been contributed towards the improvement in performance of the floating-point computations [2]. Many works are also focused on implementation in FPGA platforms[3,4].
Many multiplier and adder designs have been proposed in the past to achieve various parameters such as high speed and lesser area and low power dissipation. For multiplication, to add partial product, many adders are available like ripple carry adder, carry save adder, carry select adder and carry skip adder. Any adder can be used to generate sum of the partial products but depends on the requirements of the application, the appropriate adder must be chosen.
In this paper, different modified techniques like 2x1 multiplexers, 3:2 compressor with XOR-MUX and XNOR-MUX logics and 4:2 compressor with XOR-MUX and XNOR-MUX logics are introduced in vedic multiplier in single precision floating point multiplication to improve the performance in terms of power consumption. Further, performance comparison is done through synthesis for both existing and proposed techniques in terms of power.
The remaining portion of the paper is planned as follows: In section 2 Hierarchy of the multiplication is discussed, floating point representation is explained in Section 3, vedic multiplier is discussed in Section 4, in Section 5, Summarized proposed work is discussed and in Section 6, simulation results are explained.

2. Multiplication hierarchy

Multiplication is one of the key operation in most Digital Processing Systems. Since multipliers are composite circuits which are essential parts of the design to improve the performance. In general, multiplication process involves in in two steps called partial products generation and addition. Generation can be done using simple AND gate and addition can be done using different adders. To improve the performance of multiplier a lot of works have been dedicated, at all levels like implementation and algorithmic level. The addition process in the multiplier is carried out with the parallel execution of ripple carry adder to reduce the delay [8]. Other method also introduced to reduce the delay which is based on Carry look ahead adder but this increases the interconnection complexity [9]. Many multipliers are introduced to improve the delay, area and power consumption of the digital system [10].

3. Floating point representation

Floating Point format for Single Precision numbers is represented with 32 bits. Figure 1 illustrates the representation of single precision number.

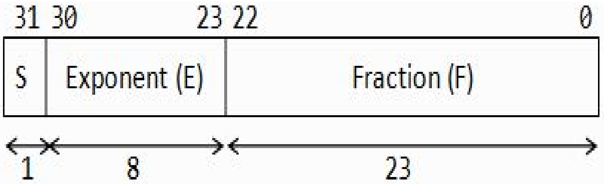

Fig. 1: Single Precision Floating Point Number.

Floating point multiplication of given single precision numbers is performed in three-steps [2]: exponent addition of given numbers and subtraction from the bias value from the result. Next step is multiplication of the two mantissa's of given numbers. Finally, sign bit generation using logical XOR operation of two MSB bits.

4. Vedic multiplier

Vedic multiplier is developed based on Urdhava Triyakbhayam sutras [3-4]. In this method, vertical and crosswise technique is used to generate partial products and then those partial products are added parallelly by using different adders. In this paper, mantissas of the two numbers are multiplied using vedic multiplier which works on the principle of Urdhva Tiryagbhyam sutras [6]. In this sutra both generation and summation of the partial products done in one step and which causes' the minimization of the carry feeding from LSB to MSB. Because of this speed of the multiplier is improved as compared to the existing multipliers [5] [7].

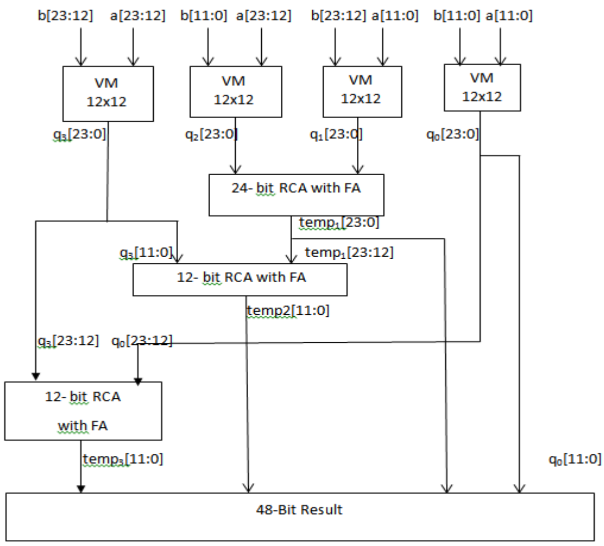

Fig. 2: 24-Bit Mantissa Multiplication Using Vedic Multiplier.

5. Proposed work

In this work, vedic multiplier with different proposed techniques like proposed 2x1 multiplexer model 1 and multiplexer model 2, modified 4:2 compressor models like XOR-Mux and XNOR-XOR-Mux logics are used to optimize the single precision floating point multiplication performance.

An optimized vedic multiplier is developed by incorporating different modified techniques called 2x1 multiplexer model 1 and model 2s and those are used for Floating point multiplication of single precision numbers.

An optimized vedic multiplier is developed by incorporating different modified techniques called 4x2 compressor models like XOR-Mux and XNOR-XOR-Mux logics those are used for Floating point multiplication of single precision.

Finally, the performance comparison is made between vedic based floating point multiplication with different techniques with respect to Power

a) FPM using Vedic multiplier with Proposed 2x1 Multiplexer Models:

In place of full adders multiplexers are used to add partial products addition. In his work, to add partial products in vedic multiplier, modified 2x1 multiplexer model1 and model2 are used and which are explained using figure 3 and figure 4. From below figures, full adder operation is designed using two 2x1 multiplexers and these modified models are used in vedic multiplier.

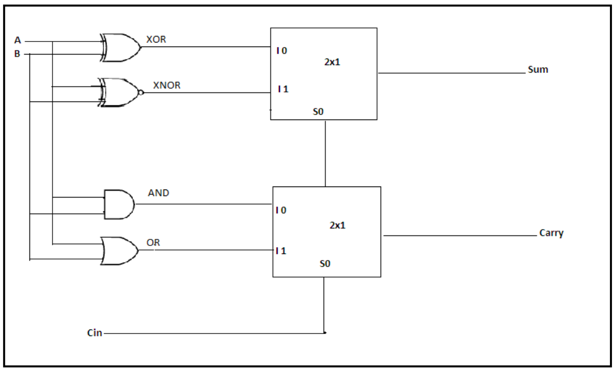

Fig. 3: Full Adder Using Proposed 1 2x1 Multiplexer

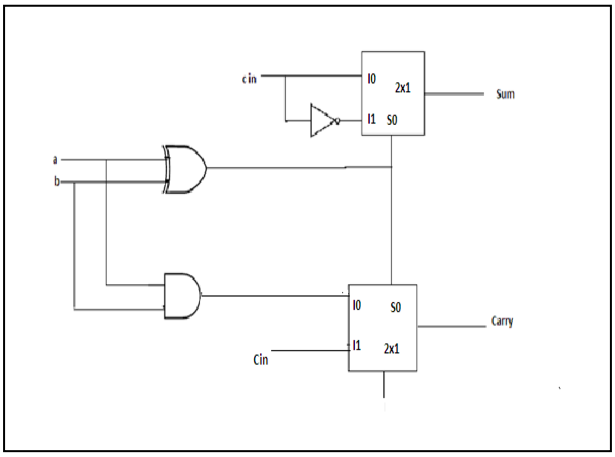

Fig. 4: Full Adder Using Proposed 2 2x1 Multiplexer

b) FPM using Vedic multiplier with Proposed 4x2 Compressor Models:

Compressors are used in place of full adder to add partial products. In vedic multiplier, to add partial products modified 4x2 compressor models are used and which are explained using figure 5 and figure 6. From below figures, full adder operation is designed using two modified 4x2 compressors with XOR-Mux and XOR-XNOR-Mux logic models are used in vedic multiplier to improve the performance.

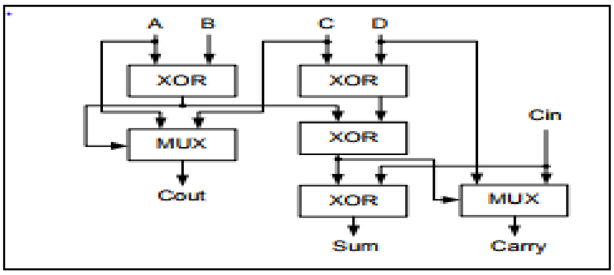

Fig. 5: 4:2 Compressor with XOR-MUX Logic.

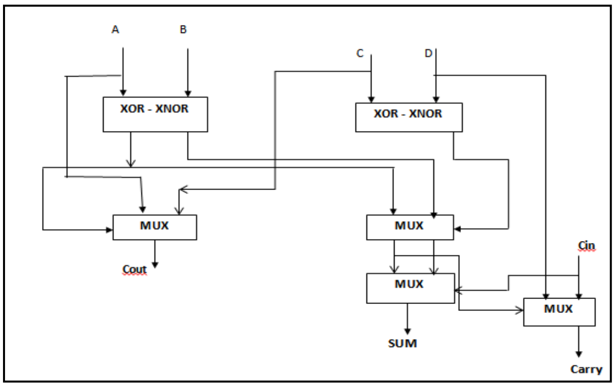

Fig. 6: 4:2 Compressor with XOR-XNOR-Mux Logic.

6. Simulation results

Performance analysis of floating point multiplication for single precision numbers with the help of Vedic multiplier with different techniques like multiplexers and compressors. The constrictions measured here are the power consumption.

a) Performance comparison analysis of SPFPM with Vedic using different techniques

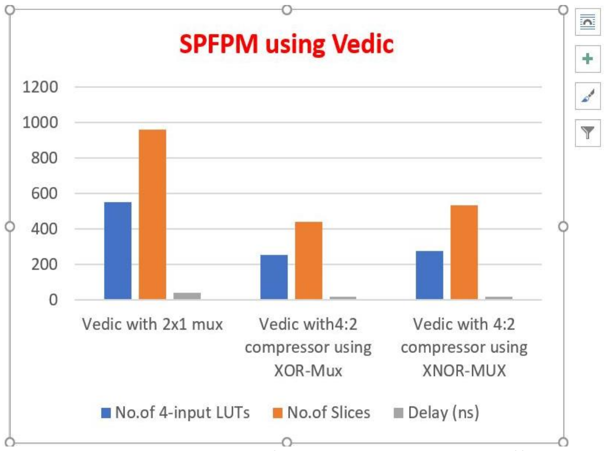

Fig. 7: Comparative Analysis of Vedic Multiplier with Different Techniques.

b) Performance Comparison Analysis

Table 1: Comparison of SPFM Using Vedic Multiplier

SPFPM using Vedic	Dynamic Power (mw)	Quiscent Power (mw)	Total Power (mw)
Vedic with 4x1 Mux (Existing)	0.002	0.081	0.083
Vedic with 2x1 Mux model1	0.003	0.081	0.084
Vedic with 2x1 Mux model2	0.024	0.081	0.105
Vedic with 3:2 compressor using XOR-Mux (Existing)	0.021	0.081	0.102
Vedic with 3:2 compressor using XNOR-XOR-Mux	0.033	0.081	0.114
Vedic with 4:2 compressor using XOR-Mux	0.002	0.081	0.083
Vedic with 4:2 compressor using XNOR-XOR-Mux	0.001	0.081	0.082

From the Table 1, It is proved through the simulation that single precision floating point multiplication using vedic multiplier provides the improved performance in respect of performance metrics. From the tabulated values, it is detected that single precision floating point multiplication with vedic using 4:2 compressor with XNOR-XOR-MUX has less power consumption compared to other techniques.

7. Summary and observations

Quiscent power is almost zero for all techniques.
Dynamic power is more for 2x1 multiplexer model1 (24mw) and 3:2 compressor using XNOR-XOR-Mux (33mw). Dynamic power is less in vedic with 4:2 compressor using XNOR-XOR-Mux
From the table I, it is observed that the total power dissipation is less in 4:2 compressors with XNOR-XOR-Mux and total power is high for 3:2 compressors with XNOR-XOR-Mux model.

8. Conclusion

In this paper, the optimized techniques are introduced to improve the performance of the single precision floating point multiplier block which plays an important role in Digital Signal Processing applications. The modified techniques such as 2x1 multiplexer, 3:2 and 4:2 compressors with XOR-MUX and XNOR-XOR-MUX logics for single precision floating-point multiplication to provides better solution in terms of power related issues. From the, simulated results, vedic multiplier with 4:2 compressor considering XNOR-XOR-Mux offers less power dissipation compared to other modified techniques.

References

[1] Mohan Shoba, Rangaswamy Nakkeeran, "Energy and area efficient hierarchy multiplier architecture based on Vedic mathematics and GDI logic", International Journal of Engineering Science and Technology, pp.1-11, June.2016.
[2] Irine Padma B.T and Suchitra. K, "Pipelined Floating-Point Multiplier Based on Vedic Multiplication Technique," International Journal of Innovative Research in Science, Engineering and Technology, Vol.3, pp.130-137, July 2014.
[3] Yashkumar. M. Warkari, Prof L.P.Thakare, Dr. A.Y. Deshmukh,"Design of Floating Point Multiplier for Fast Fourier Transform UsingVedic Sutra", International Journal of Engineering Research and General Science, Vol.2, pp.375-382, April 2014.
[4] C.Prema,C.S.Manikandababu,"Enhanced high speed modular multiplier using karatsuba algorithm" Proceedings of IEEE International Conference on Computer Communication and Informatics, Coimbatore, pp.375-382, Jan 2013.
[5] A.M. Mehta, C. Bidhul, S. Joseph, and P. Jayakrishnan, "Implementation of single precision floating point multiplier using karatsuba algorithm," Proceedings of International Conference on Green Computing, Communication and Conservation of Energy, pp.254–256, Tamilnadu, Dec 2013.
[6] Sushma R. Huddar and Sudhir Rao, Kalpana M , Surabhi Mohan" Novel High Speed Vedic Mathematics Multiplier using Compressors", Proceedings of International Conference on Communication and Signal Processing, pp.465-469, Melmaruvathur, Apr 2013.
[7] Daisuke Takahashi, "An algorithm for multiple-precision floating-point multiplication" International journal of Applied Mathematics and Computation, pp.291–298, 2005.
[8] K.Manolopoulos, D. Reisis, V.A. Chouliaras, "An efficient multiple precision floating-point Multiply-Add Fused unit", Microelectronics Journal, pp.10–18, 2016.
[9] Peter-Michael Seidel, Guy Even, Delay-optimized implementation of IEEE floating-point addition, IEEE Trans. Comput, 53(2), February 2004.
[10] Priyanka Koneru, Tinnanti Sreenivasu, Addanki Purna Ramesh. Asynchronous Single Precision Floating Point Multiplier using Verilog HDL, International journal of Advanced Research in Electronics and Communication Engineering, Nov 2013.
[11] Naresh Grover, MK Soni. Design of FPGA based 32-bit Floating Point Arithmetic Unit and Verification of its VHDL code using MATLAB, International Journal of Information Engineering and Electronics Business, MECS, Feb 2014.
[12] Gaurav Sharma, Arjun Singh Chauhan, Himanshu Joshi, Satish Kumar Alaria. Delay Comparison of 4 by 4-Vedic Multiplier based on Different Adder Architectures using VHDL, International journal of

Engineering & Applied Science Research, vol.3, pp.375-381, Jun 2013.

[13] M Pravallika, V VamsiMohana Krishna. Design and Verification of High Speed and Efficient Asynchronous Floating Point Multiplier, International journal of Engineering Research and Technology, Jul 2013.

[14] Anubhuti Mittal, Ashutosh Nandi, Disha Yadav. Comparative study of 16*order FIR filter design using different multiplication techniques, IET Circuits, Devices & Systems, Vol.11, issue 3,pp.196-200, 2017.

[15] Hemmert, K.S., Underwood, K.D. Fast, efficient floating-point adders and multipliers for FPGAs. ACM Transaction on Reconfigurable Technology and Systems. Vol.3, issue 3, pp. 1-11, 2010.