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Research paper

An unveiling FPGA based coding technique to detect and correct the faults by matrix algorithm

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Abstract

In this paper a new approach is implemented to increase the reliability of the memory by detecting and correcting the faults. In present technology the memory circuits are made up of low power technique. When high radiation falls on that circuit, Multiple Cell upsets (MCU) are generated due to this MCU the data will be corrupted. To trounce this, numerous error correction techniques are designed but the main issue is redundancy bits. The proposed technique describes about the reduction of redundancy bits. The information is arranged in the form of matrix (No of rows and no of columns) by adding certain number of rows and performing xor operation with certain no of column we can achieves less redundancy bits. The proposed work is coded using Verilog HDL, simulated using Isim and synthesized using Xilinx 14.2 ISE. The work is implemented on FPGA. No of slices used are 256 compared to previous work 300 and delay is reduced from 7.48ns to 7.2ns. Hence 14% improvement in area and 8.1% improvement in speed is observed.

Keywords: *Matrix Code; Error Correction Code (ECC); Multiple Cells Upset (MCUs).*

1. Introduction

In an Electronics device "glitch" is solitary type of soft error. These glitches are random in nature it is not catastrophic, and normally it will not destruction the device. Numerous systems have the capability to accept various level of soft errors, but these errors occurred when a charged particle strikes in a memory-type element or semiconductor memory. Mainly, the electron-hole pairs produced by the interaction between the semiconductor atoms with the active charged particle, corrupts the information stored in the memory [1]. High-energy solar particles and cosmic rays like X-rays, gamma rays react with the atmosphere generating high-energy protons and neutron that jumps to the ground. This cause varies with both altitude and latitude. One more common source of these errors is α particle, which are emitted by the radioactive isotopes present in the packaging materials of IC [2].

Error Correction can be done in two different ways one is Automatic Error Request other one Forward Error Correction codes. In Automatic Error Request technique error detection scheme is combined with request for retransmission of corrupted data, each block of data received and checked using the error detection if the check fails the data is requested for

Retransmission. [3] In Forward Error Correction the sender encodes the information taking an Error Correction Codes Prior to transmission extra data (redundancy) added to the code to get the original information. It is utilized for Reliable Storage reason CDS, DVDS, Hard plate and RAM.

2. Literature survey

Hamming code [4] is the oldest technique to detect and correct the errors. Implementation can be done by interfacing hamming code block and old weight code block. These two blocks is required to code the data which include extra bits in words that shows parity (encoding) and another blocks is required to decode the data. Encoder can be designed by using two input XOR gate and decoder can be designed by using 2 input XOR gate, with AND gate and with INVERTER gate. Decoder block is more difficult than encoder. The problem of this code is correction capability is less it will detect two errors and correct single errors only it can resolve single event upset.

Reed Solomon [5] code is used for correction of Burst and random errors because this error occurs in communication and storage medium. This coding technique can be designed by introducing parity check symbols. It is a non binary coding technique in that the code word is defined in terms of symbols rather than bits. It will corrects entire symbol, weather the error is caused by one bit being corrupted or all of the beings corrupted. If symbol is wrong all bit position will wrong result in burst noise. SEC-DED [6] Hamming Code has been designed to structure a particular class of codes known as Hsiao Codes to enhance the cost reliability and speed of the decoding logic. Later DEC-TED [7] triple error decoding codes can be implemented and it can correct maximum errors as surveyed. BICS code is proposed to detect and correct the errors. This can be done by placing the sensors in the column of the memory blocks they detect unexpected current variation of on each of the memory bit position it is used to control the current dissipation on the circuit. The combination of BICS and H tree gives low power simple encoding and decoding algorithm. It can be combined with either

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hamming or parity but combining parity bit is better than hamming. The problem of this technique it corrects only two errors. [8]
The existence DMC code is implemented by using decimal algorithm to detect the errors so that more error were detected and corrected. This DMC is designed by taking 8 symbols of 4 bit. The designed encoder and decoder is simple and having maximum correction capability but they require high redundancy bit because of redundancy bit it require more area, power, and delay. The maximum correction capability is up to 8 bits. [9]

3. Proposed technique

The Proposed architecture consists of Encoder and Decoder as shown in the figure 3.1. While the process of encoding the information bit B (input) is given to the encoder, and then the vertical redundant bits C and Horizontal redundant bits R are achieved. After the Encoding process the redundant bits and the information bit are stored in the memory. When high radiation falls on the stored memory than Multiple Cell Upsets occurs in the information these upsets can be fixed in the process of Decoder. By adopting Decimal Addition and Decimal Subtraction algorithm. The proposed DMC has highest fault tolerant capacity. In this coding scheme ERT method is introduced to reduce the area in the decoder.

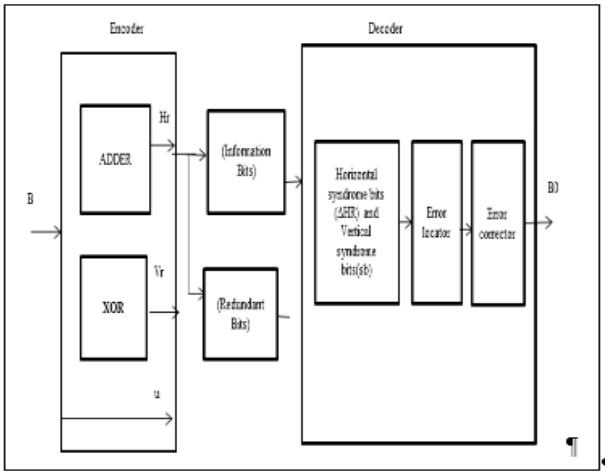


Fig. 3.1: Fault Tolarent Memory Block.

a) Process Flow:

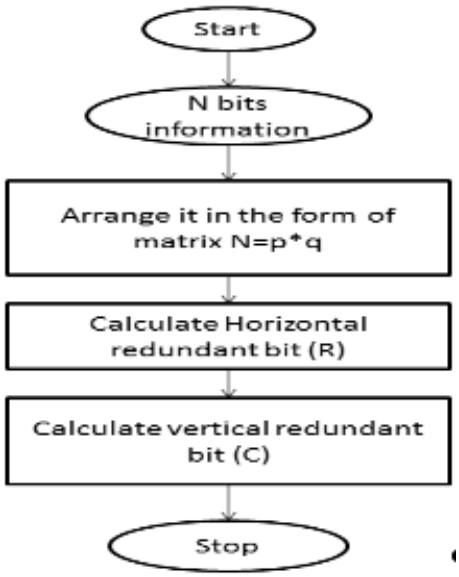


Fig. 3.2: Flow Chart of Encoder.

The flow chart describes Decimal matrix addition subtraction algorithm. Initially 64 bit data is divided in the form of symbols and arranging that symbols in matrix form. Calculate horizontal redundant bit by taking selected symbols and vertical redundant bit by doing xor operation with selected column these redundant bits are saved in memory.
Flow chart of Decoder:

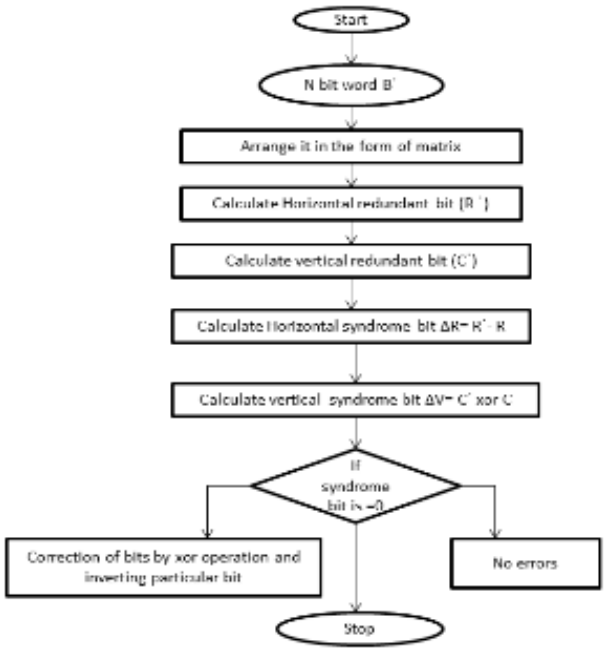


Fig. 3.3: Flowchart of Decoder.

The flow chart of decoder as shown in the figure 3.2 when high radiation falls on the memory as MCU occurs again encoder circuit is reused and calculates horizontal syndrome and vertical syndrome bits. If syndrome bits is equal to zero than no errors else correction of can be done by inverting particular bit.

b) Block Diagram of Encoder:

The encoder consists of adders and xor Circuits. In encoding process, the N bit information split into p bits and q symbols (N=p*q). These symbols can be sorted in matrix form that is q=q1*q2 where the value of q1 indicates number of rows and q2 indicates number of column. The Horizontal redundant bits R can be achieved by doing addition of preferred symbols per row. By performing XOR operation with respect to column vertical redundant bit C can be achieved.

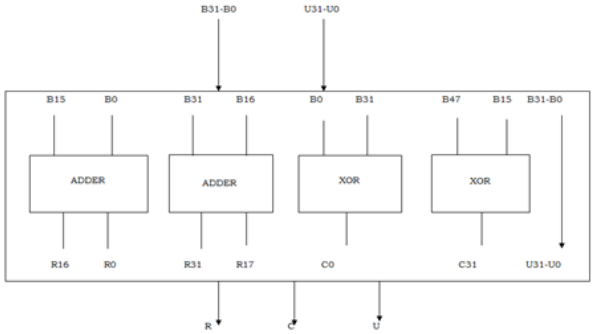


Fig. 3.4: Block Diagram of Encoder.

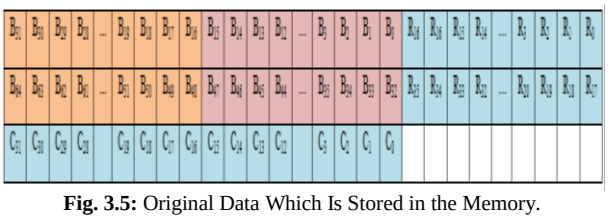


Fig. 3.5: Original Data Which Is Stored in the Memory.

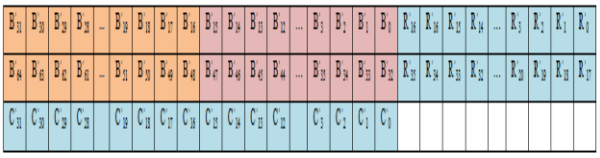


Fig. 3.6: Corrupted Data After MCU Occurs.

To examine encoder 64 bit data as shown in fig 2. These 64 bit data can be represents in the form of B0 to B64 and it is alienated into 4 symbols of 16 bit. The symbols represent in the form q1 and q2 (where q1 indicates no rows q2 indicates no of column) and it will be different for different technique. In encoder C0-C31 are vertical redundant bit and R0- R34 represents horizontal redundant bit. The number of redundant bit is depends upon the value of p and q value chosen. So the value of p and q should be sorted carefully to decline the redundant bits and increase correction capability. When the value of p=4, q1=2 and q2=8 the obtained redundant bit is seventy two. The correction capability is up to 16 bits.

When p=8 bits, q1=2 and q2= 8 than the redundant bits is around 68 the correction capability is also same as 16 bits similarly if p=16 bits, q1=2 and q2 is of 4 symbols than the redundant bits is of 66 bits and hence sorting of symbols is very important in matrix method. Dividing symbol and arranging matrix cannot be performed physically it perform Only logically hence the proposed coding technique is not have to change the memory's physical structure.

The Hr (Horizontal redundant) bits can be achieved by $R_{16}R_{15}R_{14}R_{13}\ldots R3R2R1R0=B_{15}B_{14}B_{13}B_{12}\ldots B3B2B1B0+$ B $B_{31}B_{30}B_{29}B_{28}\ldots B19B18B17B16$ (1)

$R_{33}R_{32}R_{31}R_{30}\ldots R_{20}R_{19}R_{18}R_{17}=B_{47}B_{46}B_{45}B_{44}\ldots B_{35}B_{34}B_{33}B_{32}+$ B $B_{63}B_{62}B_{61}B_{60}\ldots B51B50B49B48$ (2)

Vertical redundant bits are achieved by using

$C_0=B_0$ XOR B_{32} (3)

$C_1=B_1$ XOR B_{33} (4)

Similarly for respite of the redundancy bits is calculated by using equation (3) and (4). The encoder calculates (R33-R0) and vertical redundant bits C31-C0.and U31-U0 indicates the data bits in which copied directly from B31-B0 bits.

c) Block diagram of Decoder

The proposed decoder Fig 3.7 consists of syndrome calculator ,Error locator and Error corrector Retrieve the data from the Memory. Calculate Horizontal redundant bits R' and Vertical redundant bits C' from B'. Fault can be detected by calculating horizontal and vertical syndrome bits it can be represented by ΔR and Sy respectively. If ΔR and ΔV=0 than no error, else it can be corrected by performing Xor operation with syndrome bit inverting with particular bits obtained original bits.

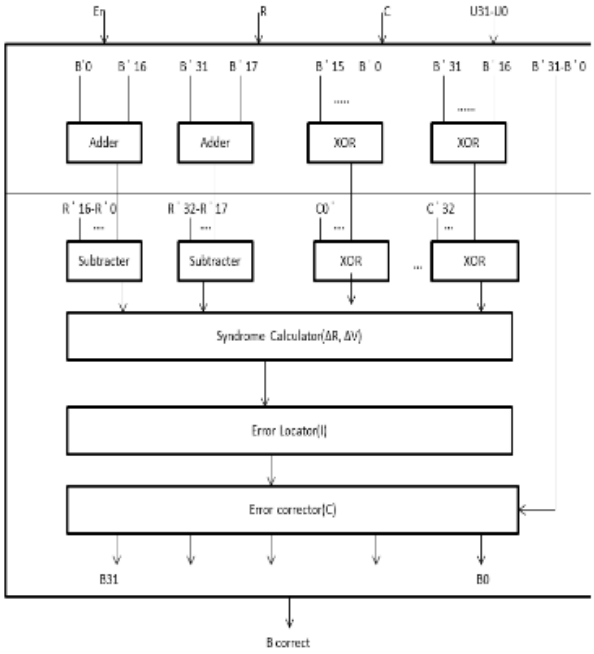


Fig. 3.7: Block Diagram of Decoder.

The received redundant bit R'_{16} to R'_0 and C'_{31} to C'_0 are achieved by the received data bits B' the horizontal syndrome bits $\Delta R'_{16}R'_{15}R'_{14}R'_{13}\ldots\ldots R'_3R'_2R'_1R'_0$ and vertical syndrome bit S_{y31}- S_{y0} can be calculated as follows

$\Delta R=R'_{16}R'_{15}R'_{14}R'_{13}\ldots R'3R'2R'1R'0\text{-}R_{16}R_{15}R_{14}R_{13}\ldots R_3R_2R_1R_0$ (5)

$\Delta R=R'_{33}R'_{32}R'_{31}R'_{30}\ldots R'20R'19R'18'R17$
$R_{16}R_{15}R_{14}R_{13}\ldots R3R2R1R0$ (6)

$\Delta V=c'$ xor c (7)

Similarly for respite of syndrome bits can be calculated from equation (6) and (7). Finally, in the error corrector the error can be corrected by inverting values of error bits. In the proposed technique the area of circuit is compacted by repeating its encoder and it is abbreviated as ERT. The ERT has capable to reduce the area without interrupting the complete the process of encoding technique and decoding technique. From the proposed technique we can identify and correct the errors like single, double, and multiple errors of each row irrespective of consecutive or inconsecutive error thus the proposed coding technique gives high tolerance, capacity of the memory compared to previous coding technique.

4. Result and analysis

The designed encoder and decoder are coded using Verilog HDL, simulated using Isim and synthesized using Xilinx 14.2 ISE. The work is implemented on FPGA.

Figure 4.1 indicates the output of the decoder by dividing 16 symbols. The 64 bit information corrupted due to radiation stored in the memory acts as input to the decoder D1. DE indicates the original data. HE1, HE2 are encoder horizontal redundant bits and VIN is encoder vertical redundant bit. After performing the decoding result R is obtained which is similar to the original data DE.

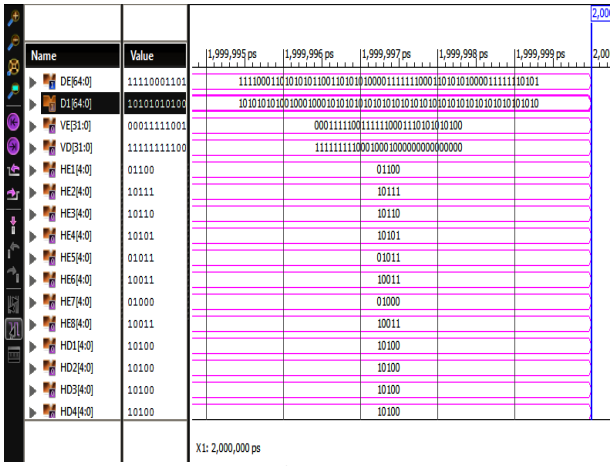


Fig. 4.1: Simulation Results of 64 Bit Data Split Into 16 Symbols.

The Figure 4.2 shows results of 8 symbols here the redundancy bits are decreased from 72 to 68 4 bit is reduced as compared Previous work.

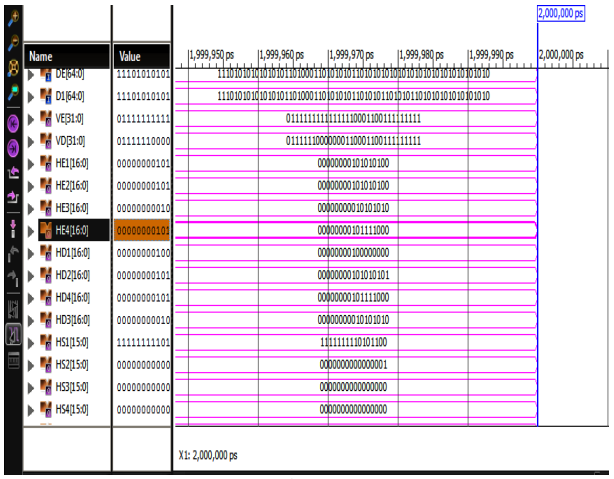


Fig. 4.2: Simulation Results of 64 Bit Data Split Into 8 Symbols.

The Figure 4.3 shows results of 4 symbols here the redundancy bits are decreased from 68 to 66 2 bit is reduced as compared 8 symbols

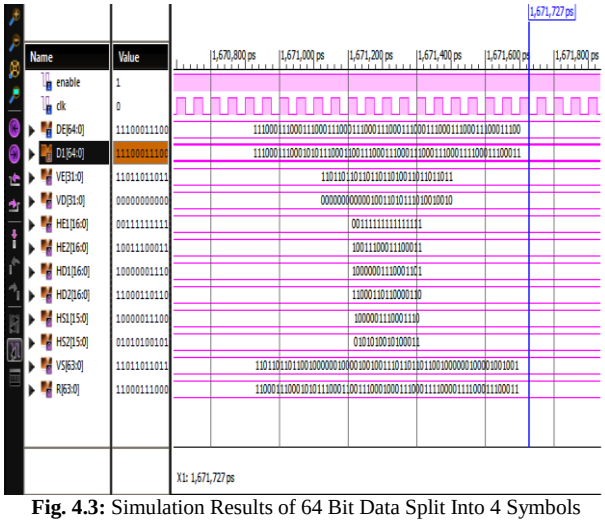


Fig. 4.3: Simulation Results of 64 Bit Data Split Into 4 Symbols

5. Comparision table

Table 5.1: Comparison of Existing and Present Technique

Parameters	symbols 16	8	4
Area in terms of slice	388 slices	300 slices	256 slices
Delay in ns	8.640 ns	7.48ns	7.20ns
Redundant bits	72	68	66

Table 5.1 shows the comparisons between 16,8, and 4 symbols Encoder and Decoder design . When this design is Simulated for considering 16 symbols the Area in terms of slice 388 , Delay in terms of ns is 8.60ns and Redundant bit is 72 bit when it is simulated for 8 symbols Area is 300 slices, Delay is 7.42 ns and Redundant bit is 64 bit, when it is simulated 4 symbols time Area is 256 slices, Delay is 7.40 ns and Redundant bit is 66 bit from the above it can be concluded that the data may be data either 32 bit or 64 bit or 128 bit if we divide in such a way to get to get 4 symbols than the result will be more efficient.

6. Conclusion

Here the novel method for Error correction Modified DMC is proposed to increase the correction capability of the system, their by reducing the redundant bits. From the above result is proved that by using modified DMC method the area, delay and Power is reduced as compare to the existing method therefore the proposed modified for Error correction is found to be novel than other method. By using less redundant bits.
The future work is to increase the reliability of the memory by reducing the redundant bit.

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