International Journal of Engineering & Technology, 7 (4) (2018) 4481-4488

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET
doi: 18995
Research paper

A new versatile active element and its application in design of minimum component all pass filters

Jahariah Sampe [1] *, Mohammad Faseehuddin [1], Shawal Hamid Md Ali [2]

[1] *Institute of Microengineering and Nanoelectronics (IMEN), University Kebangsaan Malaysia (UKM),43600 Bangi, Selangor, Malaysia*
[2] *Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia (UKM), Faculty of Engineering & Built Environment, UKM, 43600 Bangi, Selangor, Malaysia.*
**Corresponding author E-mail: jahariah@ukm.edu.my*

Abstract

In this paper a new active block namely Dual X current conveyor differential input transconductance amplifier (DXCCDITA) is discussed. A first order current mode (CM) Single Input Multi Output (SIMO) universal filter and four structures of all pass filters are developed using single DXCCDITA. Each of the proposed filters require only a single active element and minimum number of passive components one/three for implementation. The designed SIMO filter uses only one resistor and one capacitor both are grounded. Furthermore, one of the designed all pass filter uses only one grounded capacitor and enjoys cascadeability and independent tunability of pole frequency. The effect of non-idealities on the proposed filter topologies is also studied. The DXCCDITA is implemented in 0.35µm TSMC CMOS technology parameters and tested in Tanner EDA. Sufficient number of simulations are provided to establish the functionality of the proposed structures.

Keywords: *All Pass Filter; Current Mode; Current Conveyor; Cascadable; Tunable.*

1. Introduction

Last two decades have witnessed a shift in research focus towards current mode (CM) circuits. This can be attributed to their enhanced and exemplary performance capabilities even under low voltage environment where the conventional voltage mode circuits fail to perform. The CM devices exhibit high accuracy, wide bandwidth, consumes less chip area, enjoy simple architecture, exhibit enhanced slew rate and are less effected by the supply voltage scaling[1-4]. Due to the mentioned advantages the CM devices are used in the design of active filters and active all pass filter (APF) structures. Among the various filter structures APF is one of the most employed. The APF provides constant gain with variable phase shift this property is useful for employment in communications systems [5]. They are also used in phase compensation, as phase equalizers, phase shifters in multi-phase oscillators and signal generators etc. [5]-[7]. They are also utilized in synthesizing high-Q band pass filters [8-9]. The huge application range has provided much impetus to the development of newer topologies of APF with reduced number of both active and passive elements.

Some of the most utilized active blocks in APF design are the second generation current conveyor (CCII) [10], current controlled conveyor (CCCII) [11], current differencing transconductance amplifier (CDTA) [12], inverting Current conveyor (ICCII) [13], dual-X current conveyor (DXCCII) [14], fully differential current conveyor (FDCCII) [15] etc. The filters synthesized using the above mentioned active blocks can be readily found in the open literature. A literature of some of the exemplary APF is discussed below.

A two CDTA based resistors-less CM all pass implementation employing a single floating capacitor is presented in [12]. Eight topologies of CM all pass filters based on two CCII and four passive elements are presented in [16]. DOCCII based all pass filter given in [17] used two DOCCII and three passive elements. A CCCII based all pass filter implementation in [18] required two active elements and one passive component. The VM first order all pass filter proposed in [19] employed one DOCCII and three passive elements. Authors in [20] presented a negative CCII based all pass implementation utilizing three passive elements. The author in [21] presented a methodology of designing current conveyor based all pass filters from op-amp based designs. Two all pass filters were designed based on CCII but they required excessive passive elements. The VM all pass filter in [15] employed a complex element FDCCII and three passive components. The filter was cascadable but required a high supply voltage for proper functioning. The authors in [22] presented four structures of VM all pass filters, each structures required at least one CCII except the fourth which required two CCII and three passive elements. The DDCC base all pass implementation in [23] utilized single DDCC and two passive elements. The authors in [24] presented four all pass structures, each structure used one DXCCII and two or three passive elements. The DXCCII based all pass filters in [14] used three passive components and none of them were cascadable. A differential voltage CCII based CM all pass filter using three passive elements was reported in [25].The input impedance of the filter was dependent on passive elements. A minimum component CM all pass filter using a single DXCCII, two resistors and a capacitor is reported [26]. The filter require component matching to realize the response. A complete comparison of the above discussed AP filter implementations is provided in Table 1. Most of the above reported topologies of AP filters are characterized by one or more of the following weaknesses (i) use of more than one active element (ii) use of excessive number of passive elements (iii) no provision for tunability (iv) no Cascadeability.

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In this research a recently proposed new active block DXCCDITA [27] is employed in the design of minimum component first order universal CM SIMO filter and four topologies of minimum component first order APFs. The simulations are carried out using 0.35µm technology parameters from TSMC to validate the theoretical findings.

Table 1: Comparison of Proposed and Existing All Pass Filters

Ref.	Active Element (Number)	No. of Passive components		Mode of Operation	Input Impedance	Output Impedance	Tunable	Matching Condition	Technology
		R	C						
[12]	CDTA(2)	0	1	CM	High	High	Yes	No	BJT Model
[16]	CCII(2)	2	2	CM	High	High	No	Yes	-
[17]	DOCCII(2)	2	1	CM	Low	High	No	Yes	0.35µm
[18]	CCCII(2)	0	1	CM	Low	High	Yes	No	BJT Model
[19]	DOCCII(1)	2	1	VM	High	High	No	Yes	0.35µm
[20]	CCII-(1)	2	1	VM	High	High	No	Yes	0.35µm
[21]	CCII (1)	4	1	VM	High	Dependent on passive elements	No	Yes	-
[21]	CCII (1)	4	1	CM	Dependent on passive elements	High	No	Yes	-
[15]	FDCCII (1)	2	1	VM	High	Low	No	Yes	0.35µm
[22]	CCII (1)	2/1	1/2	VM	High	High	No	Yes	-
[23]	DDCC (1)	1	1	VM	High	High	No	No	0.5µm
[24]	DXCCII (1)			VM	High	Low	No	No	0.5µm
[14]	DXCCII (1)	2	1	VM	High	High	No	Yes	0.25µm
[25]	DVCCII(1)	2/1	1/2	CM	Dependent on passive elements	High	No	Yes	0.5µm
[26]	DXCCII (1)	2	1	CM	High	High	No	Yes	0.18µm
APF 1	DXCCDITA(1)	0	1	CM	Low	High	Yes	No	0.35µm
APF 2	DXCCDITA(1)	1	1	VM	High	High	No	Yes	0.35µm
APF 3	DXCCDITA(1)	1	2	VM	High	High	No	Yes	0.35µm
APF 4	DXCCDITA(1)	1	2	TAM*	High	High	Yes	Yes	0.35µm

*(TAM)-Trans-admittance Mode.

2. DXCCDITA a new active block

The Dual X current conveyor differential Input transconductance amplifier (DXCCDITA) [27-28] is functionally a connection of DXCCII and operational transconductance amplifier (OTA). The OTA provides output current proportional to the difference of input voltages multiplied by its transconductance. The transconductance of the OTA can be tuned by changing its bias current hence it provides tunability to the proposed structure. The new block carries features of ICCII, CCII, and tunable trans-conductor in one single architecture which is also simple to implement and develop in to integrated circuit. The Voltage current characteris tics of the developed DXCCDITA are given in matrix Equation 1 and the block diagram is presented in Fig. 1.

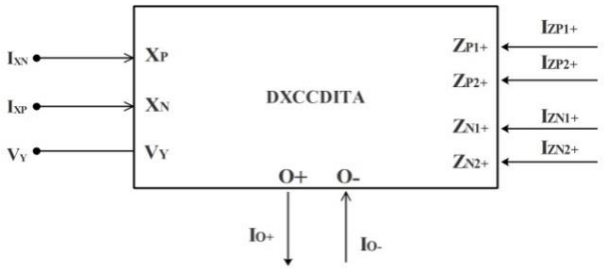


Fig. 1: Block Diagram of DXCCDITA.

$$\begin{bmatrix} I_Y \\ V_{XP} \\ V_{XN} \\ I_{ZP1} \\ I_{ZP2} \\ I_{ZN1} \\ I_{ZN2} \\ I_{0+} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & g_m & 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{XP} \\ I_{XN} \\ V_{ZP1} \\ V_{ZP2} \\ V_{ZN1} \\ V_{ZN2} \\ V_O \end{bmatrix} \quad (1)$$

The CMOS implementation of DXCCDITA is presented in Fig. 2. It is a nine terminal active element. The first stage consists of DXCCII, transistors (M1-M24). The voltage at Y appears at V_{XP} and in inverted format at V_{XN}. The current input at X_p node is transferred to nodes $Z_{P1}$and Z_{P2}. In the same way the current from X_N node is transferred to Z_{N1} and Z_{N2}.The second stage is composed of OTA. The transconductance is realized using transistors (M25-M36).The output current of the trans-conductor depends on the voltage difference between voltages at terminals $Z_{P1}$and Z_{N1}. Assuming saturation region operation for all transistors and equal W/L ratio for transistors M25 and M26 as given in Table 3 the output current $I_o$of the OTA is given by Equation 2.

$$I_O=g_{mi}(V_{ZP1}-V_{ZN1})=\left(\sqrt{2I_{Bias}K_i}\right)(V_{ZP1}-V_{ZN1}) \quad (2)$$

Where, the transconductance parameter $K_i=\mu C_{ox}\,{}^{W}/_{2L}$ (i=25, 26), W is the effective channel width, L is the effective length of the channel, C_{ox} is the gate oxide capacitance per unit area and µ is the-carrier mobility. It is evident from (2) that the transconductance can be tuned by the bias current thus imparting tunability to the structure.

3. Proposed filter structures

The proposed CM first order universal SIMO filter is shown in Fig. 3. The filter requires only single DXCCDITA, a single grounded capacitor and a grounded resistor for implementation. The filter has low input impedance. The low pass (LP) output is available at high impedance Z_{N1} terminal. The high pass (HP) output can be tapped from the O- terminal. The same structure also performs as first order inverting AP filter if the output is taken by summing the output current of O- and Z_{N1} terminals.

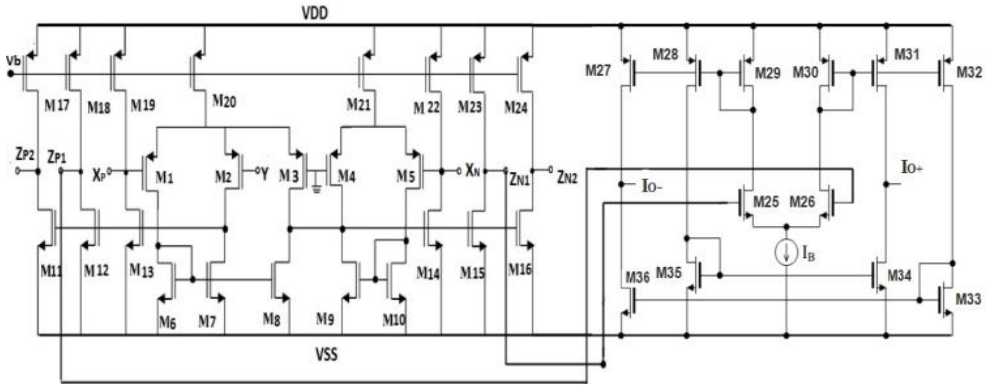


Fig. 2: CMOS Implementation of DXCCDITA.

The transfer function and the pole frequency of the filter is given in Equation 3-6. The transfer function is evaluated assuming a simple matching condition of $g_m R_1 = 1$.

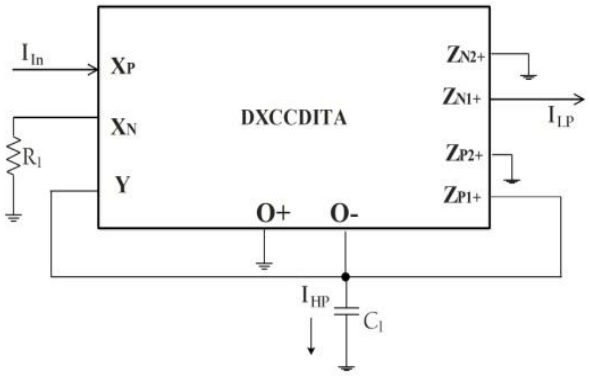


Fig. 3: First Order SIMO Universal Filter.

$$\frac{I_{HP}}{I_{in}} = -\frac{sC_1}{sC_1+g_m} \quad (3)$$

$$\frac{I_{LP}}{I_{in}} = \frac{g_m}{sC_1+g_m} \quad (4)$$

$$\frac{I_{AP}}{I_{in}} = \frac{1-{}^{sC_1}/_{g_m}}{1+{}^{sC_1}/_{g_m}} \quad (5)$$

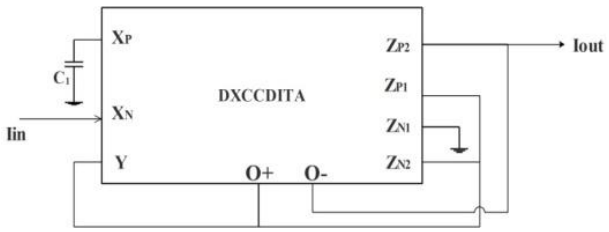
$$f_P = \frac{1}{2\pi}\frac{g_m}{C_1} \quad (6)$$

The structures of the proposed minimum component APF are presented in Figure 4 (a-c) along with their characteristic transfer function, components matching conditions and phase relations. The pole frequency of the APF1 to APF3 is given in Equation 7 and frequency of APF4 is given in Equation 8.

$$f_P = \frac{1}{2\pi}\frac{g_m}{C_1} \quad (7)$$

$$f_P = \frac{1}{2\pi}\frac{1}{C_1 R_1} \quad (8)$$

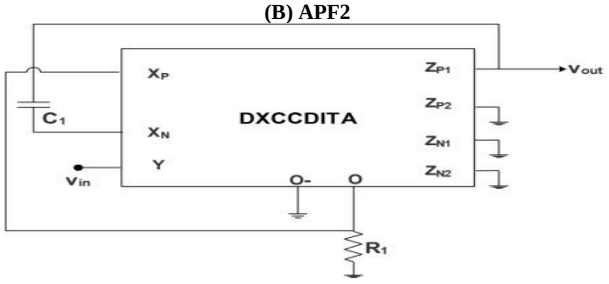
(A) APF1



$$\frac{I_{out}}{I_{in}} = -\frac{1-{}^{sC_1}/_{g_m}}{1+{}^{sC_1}/_{g_m}}$$

Phase: $\Phi(\omega) = 180 - 2\tan^{-1}(\omega C_1/g_m)$

(B) APF2

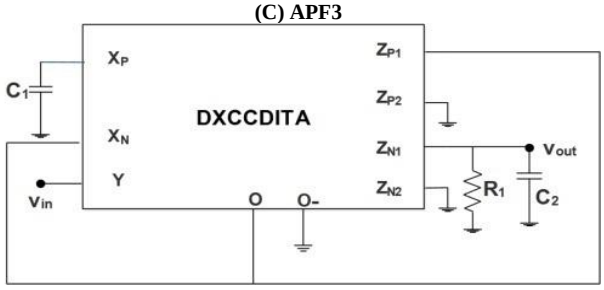


$$\frac{V_{out}}{V_{in}} = \frac{1-{}^{sC_1}/_{g_m}}{1+{}^{sC_1}/_{g_m}}$$

Matching Condition: $g_m R_1 = 1$

Phase: $\Phi(\omega) = -2\tan^{-1}(\omega C_1/g_m)$

(C) APF3



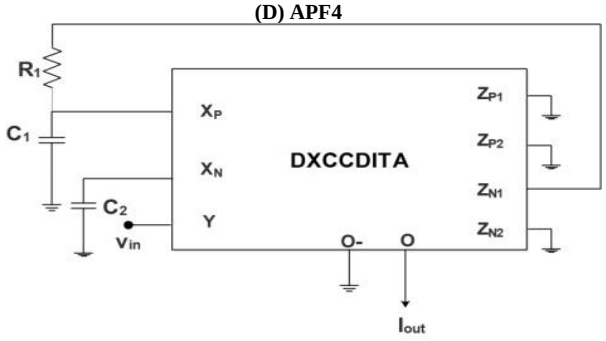
$$\frac{V_{out}}{V_{in}} = -\frac{1-{}^{sC_1}/_{g_m}}{1+{}^{sC_1}/_{g_m}}$$

Matching Condition: $g_m R_1 = \frac{1}{2}$, $C_1 = C_2$

Phase: $\Phi(\omega) = -2\tan^{-1}(\omega C_1/g_m)$

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(D) APF4



$$\frac{I_{out}}{V_{in}}=g_m\frac{1-\frac{1}{sC_1R_1}}{1+\frac{1}{sC_1R_1}}$$

Matching Condition: $C_1=C_2$

Phase: $\Phi(\omega) = 180 - 2\tan^{-1}(\omega C_1 R_1)$

Fig. 4: Proposed All Pass Filters.

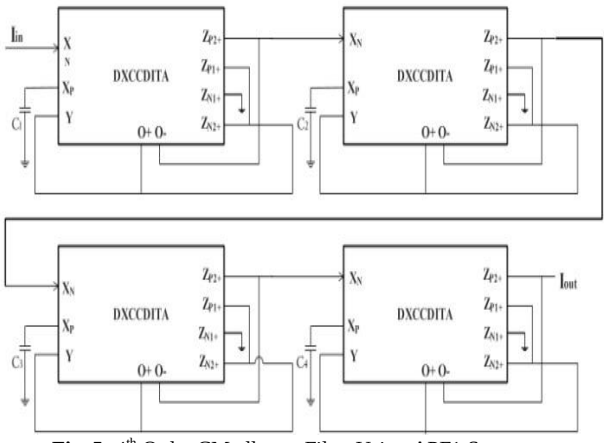


Fig. 5: 4th Order CM all pass Filter Using APF1 Structure.

The APF 1 all pass structure is a minimum component resistor less implementation utilizing only a single DXCCDITA and a grounded capacitor for the design. The APF1 is ideal for fabrication thanks to the use of grounded capacitor. The use of grounded capacitor is advantageous in mitigating noise and parasitic effects. Furthermore, the design requires least number of both active and passive elements and enjoys independent tunability of the pole frequency. The design is also fully cascadable which is further established by developing a 4th order filter by directly connecting four APF 1 as shown in Fig. 5. The second VM structure APF 2 employs a single capacitor and a grounded resistor. In this structure also the input node is high impedance which is essential for cascading point of view. The third implementation APF 3 has high input impedance and requires two grounded capacitors and a grounded resistor. The topology requires passive elements matching to realize all pass response. The fourth all pass design APF 4 is a trans-admittance mode (TAM) realization. The filter employs two grounded capacitors and a resistor. The input voltage is applied at the high impedance Y node and output current is available at high impedance Z node leading to cascadeability.

4. Non-ideal analysis

In this section the Non-idealities of the DXCCDITA are considered and their influence on the proposed all pass filter circuits is analyzed. A simplified non-ideal model of DXCCDITA is presented in Fig. 6 for analysis. The most important aspects contributing to the deviations in frequency performance are the non-ideal frequency dependent current and voltage transfer gains $\alpha_i(s)$ and $\beta_i(s)$, where $\alpha_{(N,P)}(s) = \alpha_{0(N,P)}/(1 + s/\omega_{\alpha(N,P)})$ and $\beta_{(N,P)}(s) = \beta_{0(N,P)}/(1 + s/\omega_{\beta(N,P)})$. Ideally, $\alpha_{0i} = \beta_{0i} = 1$ and $\omega_{\alpha(N,P)} = \omega_{\beta(N,P)} = \infty$. Another important performance parameter is the associated parasitic at different nodes of the DXCCDITA. The X nodes parasitics can be quantified as $Z_{XP} = Z_{XN} = R_{X(N,P)} + sL_{X(N,P)}$. The parasitic resistance and capacitance associated with the Y and Z nodes are R_{ZP}, R_{ZN} and R_Y. While the associated capacitances are C_{ZP}, C_{ZN} and C_Y. There ideal values being equal to zero. The R_o and C_o are the parasitics at the OTA output. Considering the effect of the non-ideal gains the transfer function of the four all pass filters will be modified as presented in Equations 9-12.

$$\frac{I_{out}}{I_{in}}=\frac{(s\alpha_P\beta_P C_1-g_m)}{(s\alpha_P\beta_P C_1+g_m)} \quad (9)$$

$$\frac{V_{out}}{V_{in}}=-\frac{(\frac{s\beta_N C_1}{\alpha_P}-\beta_P g_m)}{(\frac{sC_1}{\alpha_P}+g_m)} \quad (10)$$

$$\frac{V_{out}}{V_{in}}=-\frac{(s\alpha_P\beta_P C_2-\beta_N g_m)}{(\frac{sC_1}{\alpha_P}+\frac{2g_m-\alpha_N g_m}{\alpha_N})} \quad (11)$$

$$\frac{I_{out}}{V_{in}}=g_m\frac{(s\beta_N C_1-\frac{\beta_P}{R_1})}{(sC_1+\frac{1}{R_1})} \quad (12)$$

As a result of component tolerance and non-idealities in DXCCDITA the response of the practical filter deviates from the ideal one. To get a measure of the deviation, the concept of sensitivity is employed [29-30]. Mathematically sensitivity is defined as given in Equation 13.

$$S_x^y = \lim_{\Delta X-\infty}\left\{\frac{\Delta y/y}{\Delta x/x}\right\} = \frac{x}{y}\frac{\partial y}{\partial x} \quad (13)$$

Where X is the component that is varied and Y is the filter frequency ω_P in our case. The sensitivities calculated using the above procedure for the pole frequency for APF1 to APF3 are as given below.

$S_{g_m}^{\omega_P}=-S_{C_1}^{\omega_P}=1$

And for APF 4 the sensitivity is $-S_{R_1}^{\omega_P}=-S_{C_1}^{\omega_P}=1$, which are not greater than unity as desired.

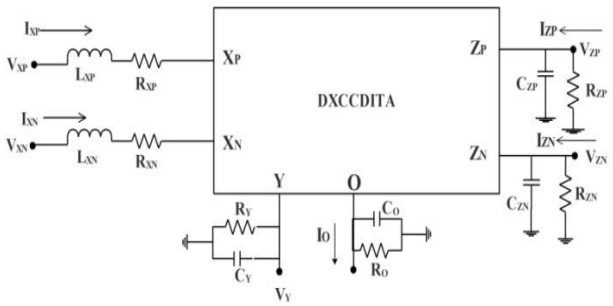


Fig. 6: Non-Ideal Model of DXCCDITA.

5. Simulation results

In order to establish the workability of the proposed dual X current conveyor differential input transconductance amplifier (DXCCDITA). It was designed in 0.35µm parameters from TSMC. The circuit was simulated in Tanner EDA to measure the important design metrics. The aspect ratios of the transistors are given in Table 3. The supply voltages are kept at $V_{DD} = -V_{SS} = 1.5V$. The bias voltage was fixed at V_{bias}=0.55V. The choice of V_{bias} sets the bias current of the DXCCII. If the bias current is increased the dynamic range of the circuit will increase but at the same time the power dissipation will also increase. There is a trade off between power dissipation, dynamic range and frequency performance which must be selected depending on the application. The bias current of OTA

was set at 50μA which resulted in a transconductance of $g_m = 0.1mS$. The proposed active element is characterized using the method stated in [31]. First, the voltage following characteristic between Y and X_P and X_n nodes is tested as shown in Fig. 7. Next, the DC Current transfer between (X_P and Z_P) and (X_N and Z_N) is measured as shown in Fig.8. The AC analysis was performed to evaluate the current, voltage and transconductance transfer bandwidths of the DXCCDITA. The associated plots are given in Fig.9-11. The transconductance characteristic of the OTA is examined by applying a DC sweep at its input and noting the output current. The transconductance characteristic is presented in Fig. 12 for a bias current of 50μA. The important performance parameters are summarized in Table 4.

Table 3: Aspect Ratios of the Transistors

Transistor	Width (W μm)	Length(L μm)
M1- M2	1.4	0.7
M3- M5	2.8	0.7
M6- M7	2.4	0.7
M8- M10	4.8	0.7
M11-M24	9.6	0.7
M25-M36	2	1

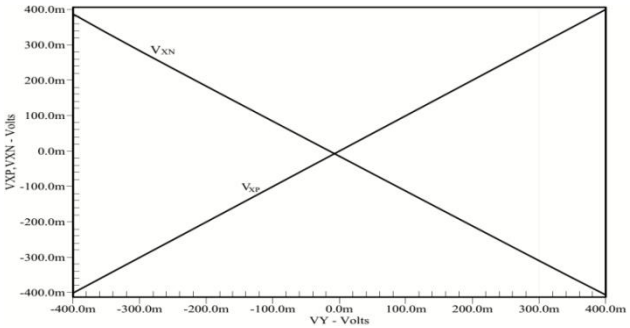


Fig. 7: DC Voltage Transfer Characteristics of X_P and X_N Nodes.

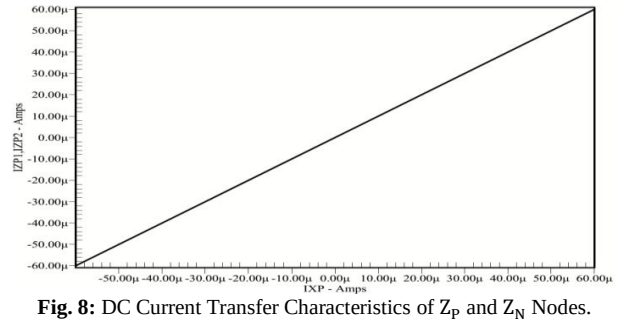


Fig. 8: DC Current Transfer Characteristics of Z_P and Z_N Nodes.

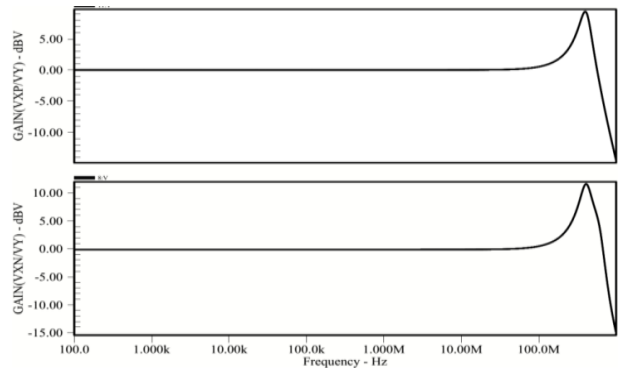


Fig. 9: (A) Voltage Transfer Bandwidth (V_{XP}/V_Y) (B) Voltage Transfer Bandwidth (V_{XN}/V_Y).

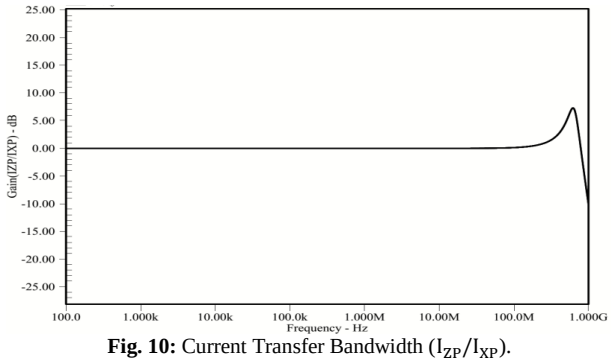


Fig. 10: Current Transfer Bandwidth (I_{ZP}/I_{XP}).

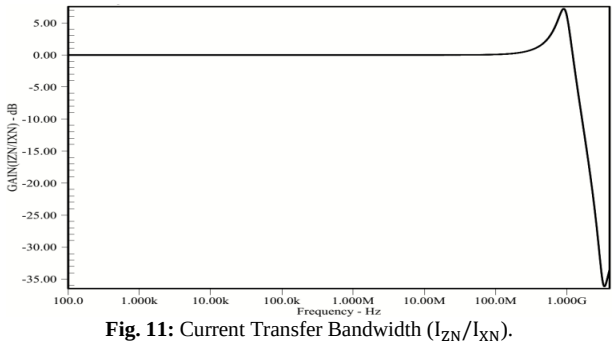


Fig. 11: Current Transfer Bandwidth (I_{ZN}/I_{XN}).

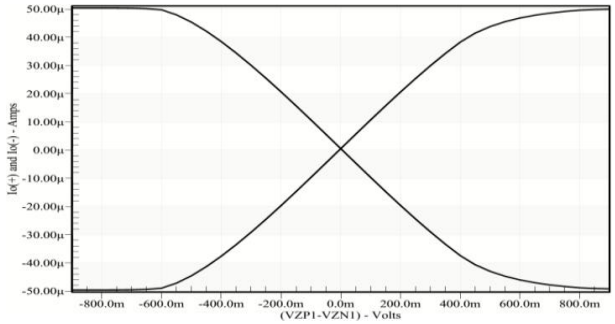


Fig. 12: Transconductance Transfer Characteristics $I_O = g_m(V_{ZP1} - V_{ZN1})$.

Table 4: Performance Parameters of the Proposed DXCCDITA

Voltage Gain (V_{XP}/V_Y)	0.98
Voltage Gain (V_{XN}/V_Y)	0.95
Current Gain (I_{ZP}/I_{XP})	1.05
Current Gain (I_{ZP}/I_{XP})	1.05
DC Voltage transfer range	±400mV
DC Current Transfer range (I_{ZP})	±60μA
DC Current Transfer range (I_{ZN})	±60μA
Voltage Transfer B.W. (V_{XP}/V_Y)	632MHz
Voltage Transfer B.W. (V_{XN}/V_Y)	728MHz
Current Transfer B.W. (I_{ZP}/I_{XP})	932MHz
Current Transfer B.W. (I_{ZP}/I_{XN})	1.32GHz
Parasitic Resistance at $X_P$node R_{XP}	71.1Ω
Parasitic Resistance at $X_N$node R_{XN}	38.2 Ω
Resistance at Z_N node R_{ZN}	305K Ω
Resistance at Z_P node R_{ZP}	305 K Ω
Resistance at O node Z_O	1.05M Ω

Now the proposed SIMO first order universal filter is tested. The filter is designed for a pole frequency of 1.59154MHz by selecting C_1=10p and R_1=10k. The LP and HP responses are presented in Fig. 13-14, by adding the high pass and low pass currents the inverting AP response is also obtained as shown in Fig. 15. The simulated pole frequency of the all pass filter was found to be 1.6138MHz which results in 1.4% error. The error occurred due to non-ideal voltage and current transfer gains and parasitic elements present in the DXCCDITA as discussed in detail in section 4. To establish the linearity of the filter transient analysis is performed for LP and AP responses. The results are given in Fig. 16-17.

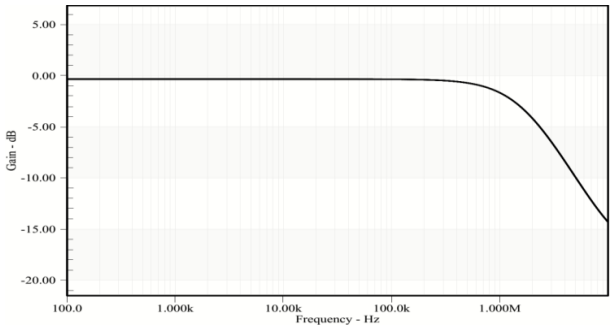


Fig. 13: Low Pass Response of the SIMO Filter.

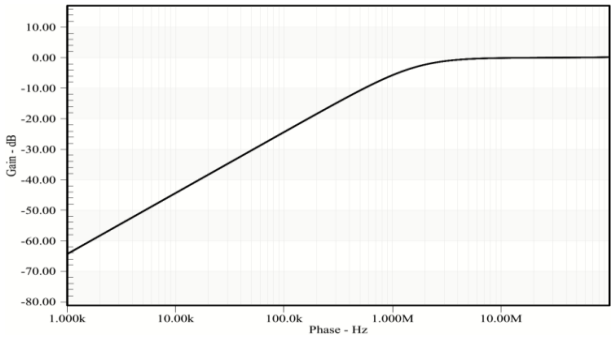


Fig. 14: High Pass Response of the SIMO Filter.

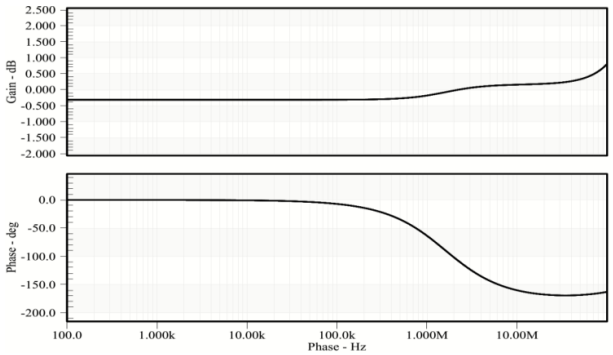


Fig. 15: Inverting All Pass Response of the SIMO Filter.

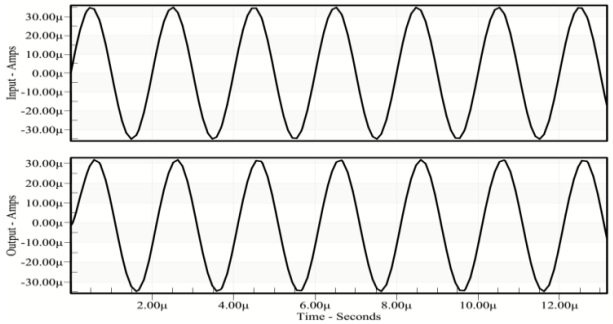


Fig. 16: Transient Response of the Low Pass SIMO Filter.

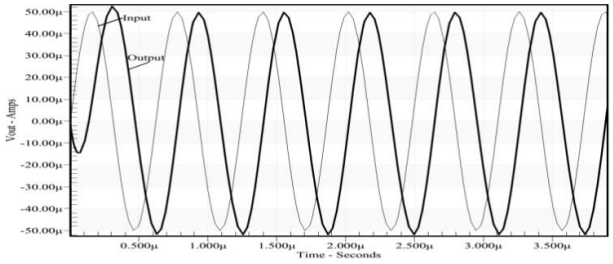


Fig. 17: Transient Response of the Inverting All Pass SIMO Filter.

Next, the second proposed resistor-less APF1 structure is examined. The filter is designed for a frequency of 1.59MHz by selecting C_1=10pF and bias current of 50μA (g_m = 0.1mS). The gain and phase characteristics of the filter are given in Fig. 18. Transient analysis is also performed as shown in Fig. 19 to analyse the phase difference between input and output signals. It can be seen that the phase difference is almost 90^0. The phase shift is further validated by the X-Y plot as shown in Fig. 20. A 4th order filter is developed by directly cascading the APF1. The phase plot of the 4th order filter for bias currents of 10μ, 50μ, 100μ and 150μ is given in Fig. 21. This verifies the cascadeability and tunability of the APF1.

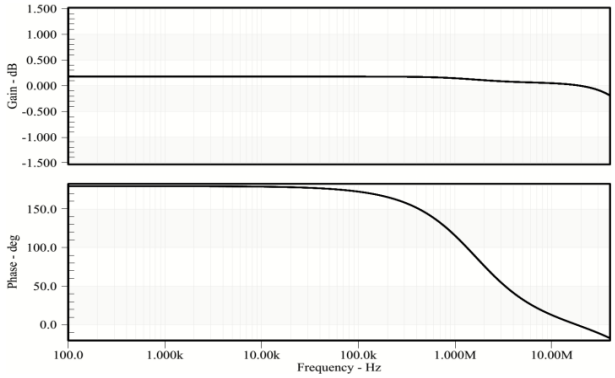


Fig. 18: Gain and Phase Response of the APF 1.

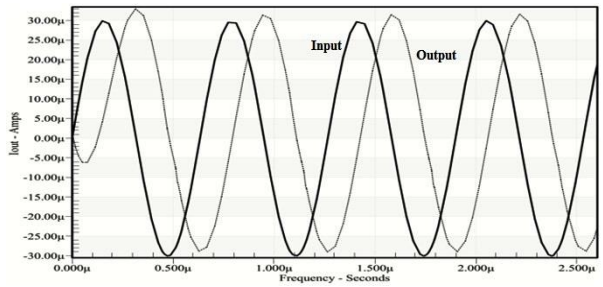


Fig. 19: Transient Response of the APF 1.

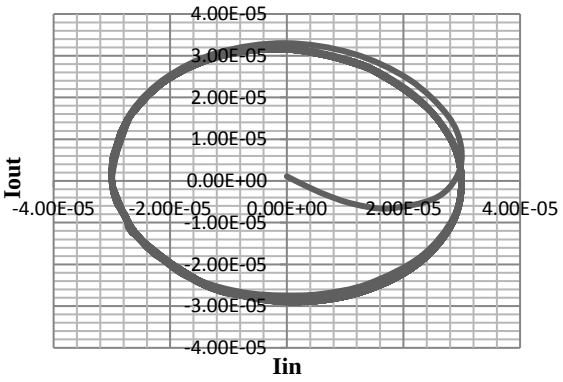


Fig. 20: X-Y Plot of the Input and Output of the All Pass Filter APF 1.

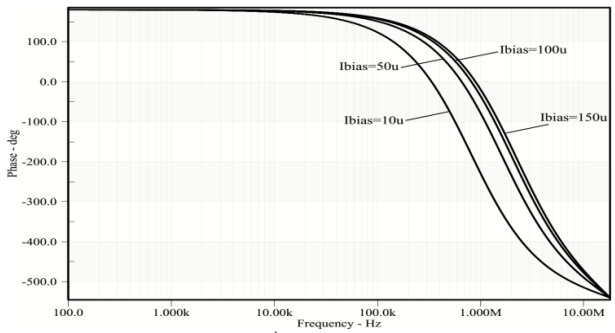


Fig. 21: Phase Response of the 4th Order Filter for Different Bias Currents.

The effect of capacitance variability on the APF 1 filter transfer function is examined by performing the Monte Carlo analysis for 10% variation in the capacitor value. The Gaussian distribution is chosen for the analysis. The plot is given in Fig. 22. It can be inferred from the plot that the filter performs well and shift in the frequency is within acceptable limits. Moreover, the shift in the frequency can be nullified by adjusting the bias current of the OTA.

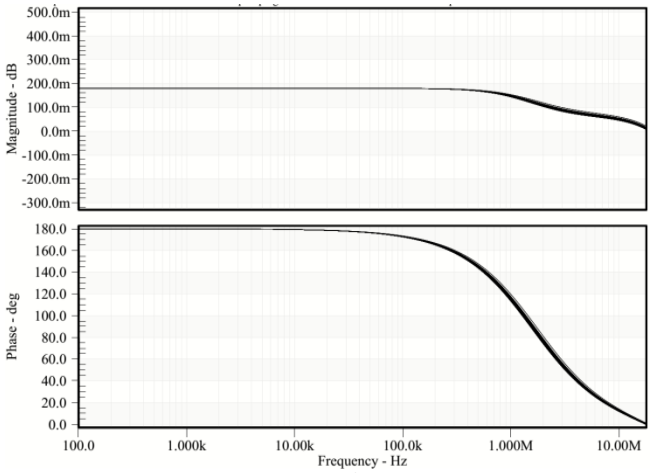


Fig. 22: Monte Carlo Analysis Result for 10% Variation in Capacitance Value.

The APF 2 is designed and simulated for a pole frequency of 1.59MHz with passive components values set as C_1=10pF and R_1=10KΩ. The resulting plots are presented below Fig. 23.

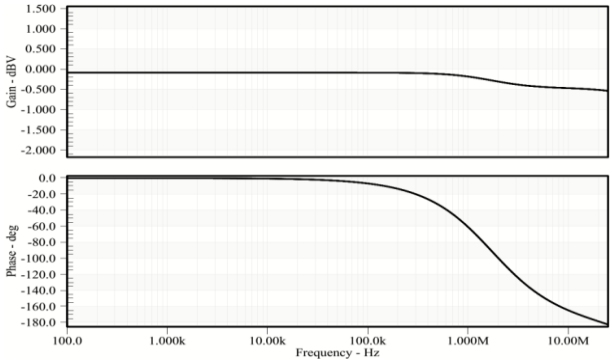


Fig. 23: Gain and Phase Response of the APF 2.

The VM APF 3 is tested with C_1=C_2=10pF and R_1=5K to achieve the pole frequency of 1.59MHz. The discrepancy between simulated and theoretical results was around 1% which is small. The error occurred due to non-ideal voltage and current transfer gains and parasitic elements present in the DXCCDITA as discussed in detail in section 4.The associated plots are given in Fig. 24.

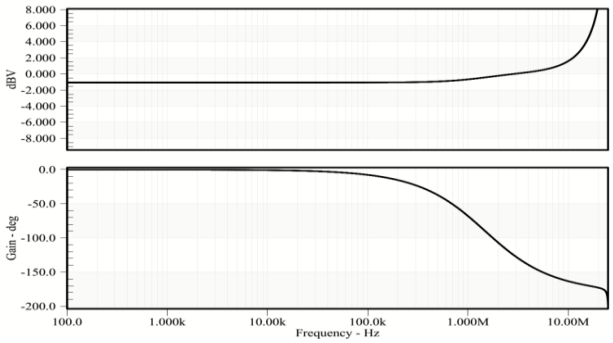


Fig. 24: Gain and Phase Response of the APF 3.

6. Conclusion

The new active block Dual X current conveyor differential input transconductance amplifier (DXCCDITA) is presented in this study. A thorough analysis of the proposed active element is carried out to establish its workability. Next, a minimum passive element CM first order SIMO universal filter and four structures of minimum component all pass filters are proposed. All the developed filters requires one active element and one/three passive components for implementation. Some of the filters require simple component matching to realize all pass response. One of the designed all pass filter requires only one grounded capacitor, enjoys independent tunability of pole frequency and is cascadable as well. A scheme for realizing nth order CM all pass filter is also suggested and a 4th order filter is developed from it. The effect of non-idealities which influences the performance of the filter structures is also studied. Enough number of simulation results are provided to validate the theory. The simulations are performed using the 0.35μm parameters using Tanner EDA. The results are in good agreement with the proposed theoretical analysis.

Acknowledgement

This work is funded by Minister of Education Malaysia under grant FRGS/1/2018/TK04/UKM/02/1 and UKM internal grant KRA-2018-058.

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