International Journal of Engineering & Technology, 7 (3.29) (2018) 180-184

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper



Low power driver receiver topology with delay optimization for on-chip bus interconnects

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Abstract

Demands on reducing the delay and power on integrated circuits is increasing with the development of more and more low power devices. The technology scaling and the device design manage static power dissipation. However, the dynamic power dissipation and the delays associated with the bus interconnects have to be addressed separately. A low swing driver-receiver circuit for driving and receiving the signals on the global bus interconnects is presented. Also the capacitively driven interconnects are used for the signal transmission and a series coupling capacitor is introduced at an optimized location along the bus. A substantial improvement of 55% in the delay performance is obtained with the driver-receiver and capacitively driven interconnect topology combine for the data transmission bus

Keywords: *Static Power; Dynamic Power; Global Bus Interconnect, Driver-Receiver; Capacitive Driven Bus Interconnect.*

1. Introduction

The complexity of VLSI circuits is continuously increasing and at the same time, the demand for reducing the power consumption of the chips is increasing. The usage of more and more portable and hand held, battery operated devices is fuelling this demand [1]. The major component of the power dissipation in integrated circuits is the dynamic power dissipation caused due to charging and discharging of the output load capacitances. The interconnects are primary capacitive loads and dissipate up to 50% of total power [2]. Interconnects also have a major contribution to the chip performance and robustness [2], [3]. In many high performance gate arrays the component of power dissipation due to interconnects is around 40% of total dissipation. Indeed, the data bus, address bus, control line running across the length of the chips invariably increase the capacitance. The number of data bus lines increases with more and more demand higher throughput. The buses are indispensable even with scaling calling for new circuits and low capacitance interconnect technology.

Various architectures for the interconnect buses proposed for reducing the power consumption primarily work on either reduced voltage swing on the load [4-7] or by implementing charge-recycling procedure [8], [9]. Reducing voltage swing is an effective way to reduce power dissipation and to increase the efficiency on interconnects. However, voltage swing reduction increases the complexity of the on-chip circuitry and has an effect on the reliability and performance. Cross talk, substrate coupling, interconnect delay, transmission line effects, power supply integrity are the effects due to signal reliability and integrity [3]. Nakagome et.al. used the dual bus line architecture and the receiver dissipated static power. Circuit topologies using devices with different threshold Nekili and Savaria [7] presented voltages. Yamauchi et al [8] used the BiCMOS technology to allow high speed operation and at the same time reduce the dynamic power dissipation.

With large scale integration of devices on chip, the contribution of interconnects in the overall performance is ever increasing. Two types of interconnects are used in the VLSI chips. The local interconnects connect the logic gates in function blocks and decrease in length with the improved scaling. The Global interconnects which connect blocks or units span large distances in SoCs. Global interconnects are hence a bottleneck for modern day state of the art chips.

Solutions to address speed and power issues for on chip interconnects are proposed which include repeater insertion, low swing circuits, current mode signaling [10-11], amplitude pre-emphasis techniques [12-13] and capacitively driven interconnects [14-15]. These techniques achieve low power and delay in signal transmission.

In this paper, the design topology for low power, low swing driver-receiver pair for bus interconnects is presented. In addition to the low swing driver receiver design, bus interconnect modeling is presented. Capacitively driven bus is modeled and simulated along with a low power driver-receiver pair to obtain lesser delays in the signal transmission. This paper is organized as follows. Section II presents the concept of capacitively driven bus interconnects and the delay optimization. Section III presents the driver receiver circuit topologies for low power and low delay implementation. The simulation setup and the test architecture is presented in Section IV. The results, analysis are summarized in Section V and conclusions in Section VI.

2. Modeling of capacitive driven bus interconnect

Capacitively driven bus interconnects are a promising solution for on chip global bus as they do not need a secondary power supply to achieve low swing signalling and reduced wire delays. A capacitively driven interconnect utilizes a series capacitor on the driver end before the interconnect. The concept is illustrated in Fig 1 for single bit. The interconnect can be modelled as a passive series of

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RC networks as in the conventional transmission line model. As there is no DC path to ground, all the intermediate nodes in the circuit are floating. The intermediate node voltages are given by Equation 1.

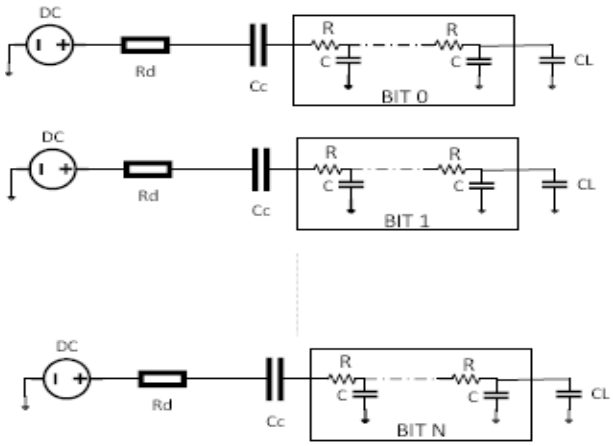


Fig. 1: Capacitive Driven Bus Interconnect Schematic.

$$V_n = \frac{C_w C_c \left[\left((R_d + R_w)\frac{C_c}{C_w} + \frac{R_w}{2}\right) C_L + R_d C_c + \frac{R_w C_w}{6} + \frac{R_w C_c}{2}\right]}{(C_L + C_c + C_w)^2} \quad (1)$$

Where,

CW Interconnect wire capacitance
Cc Coupling capacitance
CL Load Capacitance
Rd Driver series resistance
RW Interconnect wire resistance
Equation 2 gives the approximate value of first order delay

$$T_{dc} \approx \frac{R_w C_w}{6} \quad (2)$$

The RC characteristics of a global interconnect make it behave as a low pass filter, hence making the interconnect bandwidth limited. During the transmission, different frequency components travel with different velocities, which in time domain results in intersymbol interference. The series coupling capacitor, in frequency domain acts as a high pass filter. By using the series coupling capacitor, the intersymbol interference can be reduced. With a high pass filter, some of the low frequency components may increase intersymbol interference if the frequencies are too high to be used and hence a band pass filter is recommended. A low pass filter followed by high pass filter is preferred for implementing the BPF. The RC characteristics of interconnect makes it a natural low pass filter. Hence, the requirement of having a band pass filter can be designed by properly placing the high pass filter along the interconnect. The placement of high pass filter section of the BPF opens up the scope for optimization. In case of a capacitively driven interconnect, the series element which is nothing but acting as a high pass filter, the location of same needs to be finalized.
To finalize the coupling capacitor location along the interconnect, the capacitively driven wire is modelled as two sections of interconnects connected by the series coupling capacitor. The first order delay in this case is approximated by Equation 3.

$$T_{dco} \approx \frac{R_1 C_1}{6} + \frac{R_2 C_2}{2} \quad (3)$$

Where R1, C1 and R2, C2 are the resistance and capacitance of the two sections of the transmission line. The optimized location of series capacitor is obtained as k=1/4. Hence, in the capacitively driven interconnect, the bandwidth or in that sense, the delay optimized location of the capacitor is approximately 25% from the driver.

3. Driver receiver topologies

The scheme mainly works on the idea of limiting the voltage swing along interconnect to improve performance. The necessity of external power supply of reference voltage is avoided by using this limitation. The voltage swing limit is given by Equation 4

$$\sim V_{tn} \le V_s \le \left(V_{dd} - \left|\sim V_{tp}\right|\right) \quad (4)$$

The energy saving ratio is given by Equation 5.

$$\frac{E_{low}}{E_{tot}} = \frac{V_s}{V_{dd}} \cong \frac{V_{dd} - \left|\sim V_{tp}\right| - V_{tn}}{V_{dd}} \quad (5)$$

The schematic diagram of driver-receiver configuration is shown in Figure 4. The driver and receiver end circuits are detailed in Figure 5 and Figure 6

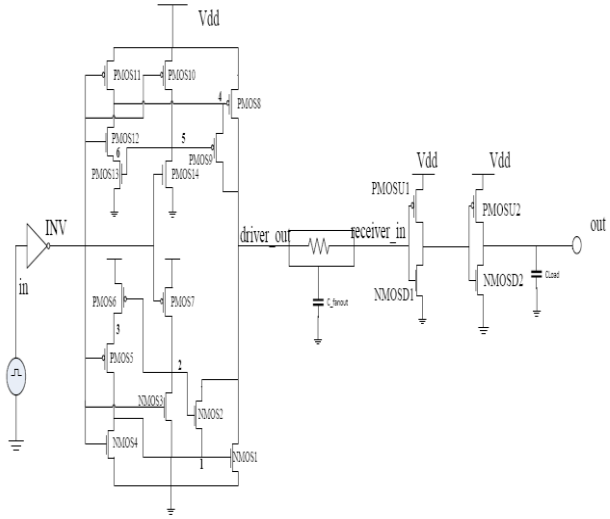


Fig. 2: Low Swing Driver-Receiver Architecture.

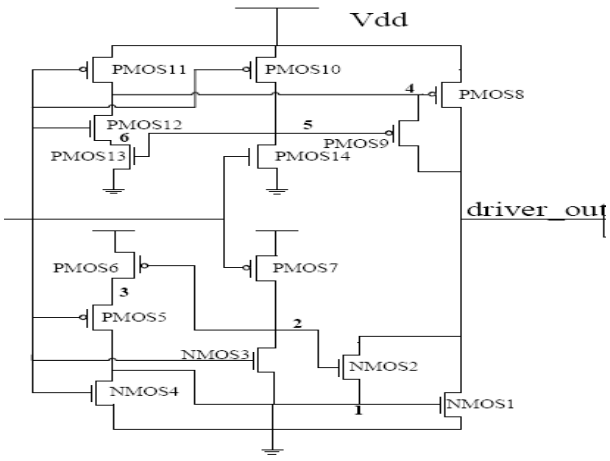


Fig. 3: Driver End Schematic.

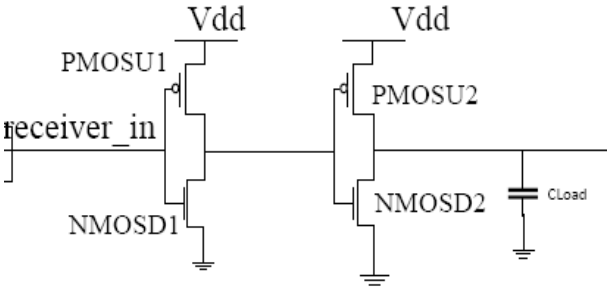


Fig. 4: Receiver End Schematic.

The driver section of the proposed scheme operates in three different modes: Active, Diode connected and Source follower. In the fully active mode, the driver provides full drive capability to charge/ discharge the interconnect line. The voltage swing is limited by diode connected mode of driver also offering lower impedance. Finally the source follower mode provides better noise immunity. When the interconnect is driven to opposite direction, transistor finally turns off.

The overdrive beyond the switching limits improves the propagation delay and can be controlled by proper transistor sizing. The scheme gives higher drive strength for the same area as it has only one series transistor. In case the line is inactive for long periods, voltage level guards can be incorporated.

When input is HIGH, transistors NMOS3, NMOS4 and PMOS6 are ON and NMOS1 (N driver), NMOS2, PMOS5and PMOS7 are OFF. When the input transits from HIGH-LOW, NMOS4, NMOS3 and PMOS8 (P driver) are turned OFF, while the gate of NMOS1 is charged, through PMOS5-PMOS6, fully activating the output transistor (mode 1). As the interconnect line discharges towards ground, PMOS7 which is active, turns PMOS6 OFF and turns NMOS2 ON. Gate of NMOS1 "holds" the charge while the line is discharging till it is not low enough to activate NMOS2.When NMOS2 is active, gate of NMOS1 is driven to match the line (mode 2). Upon LOW-HIGH transition of input, the same events occur on the upper half of the circuit (PMOS8 side).

The receiver section is a simple inverter with an Enable signal. A balanced inverter is selected because of its simplicity and faster performance for conditions when the driven line crosses Vdd/2 at every transition. Long interconnect lines can lead to transistor mismatch in driver and receiver transistors. The enable signal in receiver then turns off the receiver avoiding any bias current when the line is not used.

On the other end of the transmission line (driver end), a simple inverter with enable signal is used as in Fig. 6. The enable signal can be used to turn-off the inverter when the interconnect line is not used.

4. Test architecture and simulation setup

The test structure for testing the driver-receiver topologies is shown in Figure 5. The capacitively driven interconnect is modelled as two sections of interconnects each modelled as lumped RC circuit. Both the interconnect portions are connected by the coupling capacitor. The driver-receiver pair is simulated with an output load capacitance of 25fF. The metal interconnects are implemented in METAL3 (M3) layer and are modelled with a per unit resistance Rw=120Ω/mm and per unit capacitance, Cw=150fF/mm. To model the fan-out, an extra capacitive load of 60fF/mm length of wire is added as distributed load along the interconnect length.

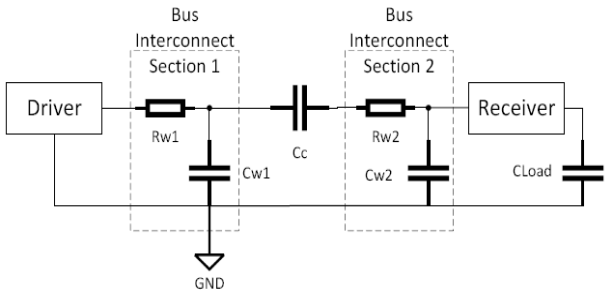


Fig. 5: Test Architecture for Simulations With Capacitive Driven Bus Interconnect.

The test conditions are listed in Table 1.

Table 1: Test Conditions

Parameter	Symbol	Value
Power Supply	V_{ddh}	1.0V
Gate Source Voltage	V_{gs}	0.54V
Loading Condition	C_L	60fF/mm
Output Capacitive Load	C_{Lout}	100fF

The circuit test setup as shown in Figure---is used to study the delay performance of the driver-receiver circuit and also to study the effect of having the series capacitor element in the interconnect.

The simulations are carried out with the parameters as mentioned in Table 1. The delay in signal propagation from driver to receiver is simulated for different interconnect lengths and also for different coupling capacitor values. An optimum value of the coupling capacitor is selected and the results are presented in Section V. To see the effect of coupling capacitor on the delay, one simulation is carried out without the coupling capacitor. A comparison between the values gives an understanding the benefit of capacitor driven interconnect line against the normal one.

5. Results and discussion

Performance analysis results for delay in the signal transmission through the interconnect are presented in this section.

a) Simulation Results

Fig 6 shows a typical transient response of the input and output waveforms for a test case with coupling capacitor of 5pF and interconnects length of 10mm. The top plot is the input waveform, middle plot is the waveform at the end of the interconnect and receiver input, the bottom plot is the final output of the receiver circuit.

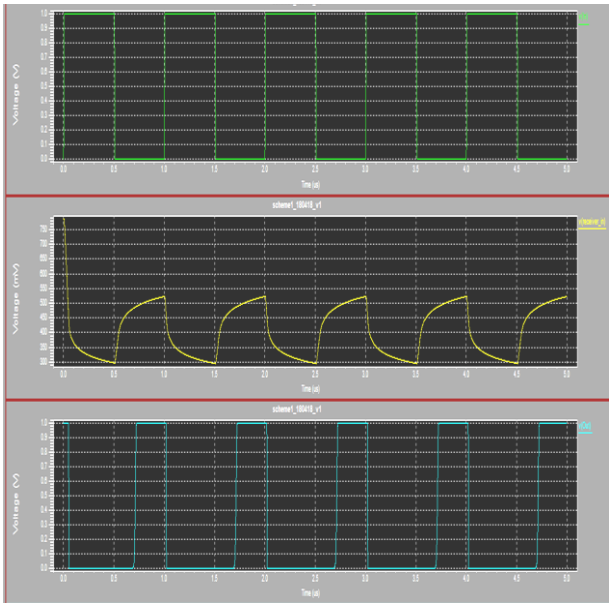


Fig. 6: Transient Analysis for Coupling Capacitor of 5pf and Interconnect Length 10mm.

Fig 7 and 8 shows the similar plot for interconnect length of 1mm with coupling capacitor of 5pF and 0.5pF respectively. Fig 9 tries to present the effect of varying coupling capacitor values on the delay for a fixed length of bus interconnect wire.

b) Discussion

As shown in Fig 6, the input signal is reproduced at the receiver output (logically inverted). Also important to note here is the middle plot which shows the output waveform at the receiver input or at the end of the interconnect. As was mentioned in the beginning, the driver-receiver pair design employs low swing topology which is evident from the peak to peak voltage swing in the middle waveform. The low swing signal is then reproduced by the receiver to match the input signal waveform. Similar transient results are shown in Fig 7 and 8 for other values of coupling capacitor.

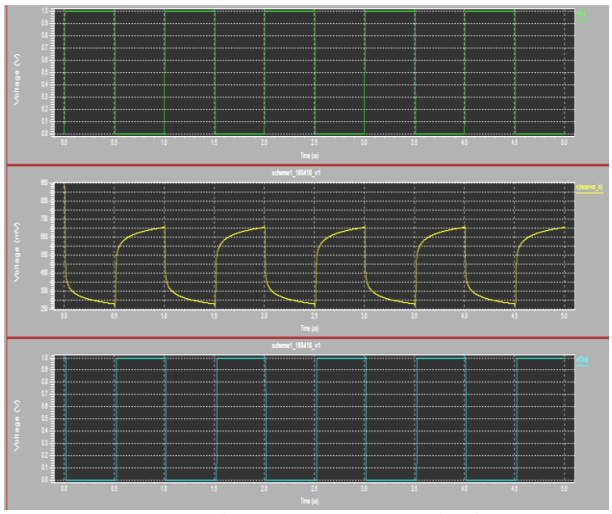


Fig. 7: Transient Analysis for Coupling Capacitor of 5pf and Interconnect Length 1mm.

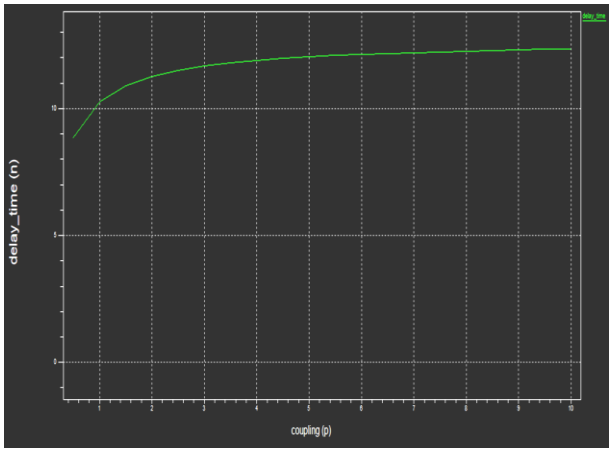


Fig. 8: Transmission Delay for Varying Coupling Capacitor Values with 1mm Interconnect.

Fig 9 summarizes the effect of coupling capacitor value on the delay introduced in the circuit. It is trivial to observe that as the capacitor value increases, delay is also increasing. Hence, the coupling capacitor value has to be kept small.

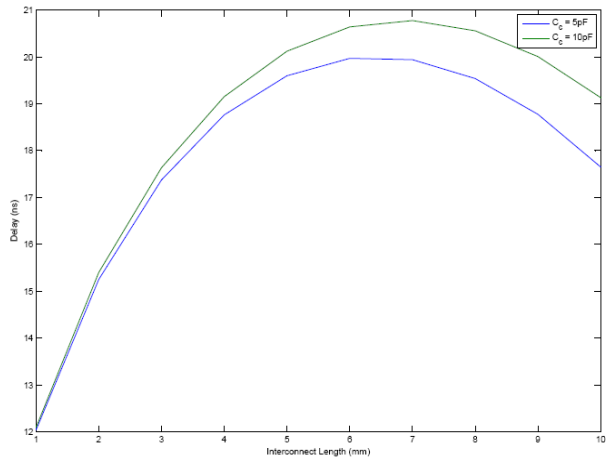


Fig. 9: Transmission Delay for Varying Interconnect Length and Different Coupling Capacitor Values.

The other aspect of dependence on delay is observed from the plot in Fig 10. This plot shows the delay variation with the change in interconnect length from 1mm to 10mm (which is of the order of present day global interconnect lengths for complex SoCs). The delay increases as the length of interconnect increases peaks at 7mm and then starts decreasing. The delay is also more for the higher coupling capacitor as compared to the circuit with lower coupling capacitor which is in line with the results of Fig 8. The plot in Fig 10 shows that for higher interconnect lengths the difference in delays for two coupling capacitor values is higher. The difference is not so prominent for lower interconnect lengths. This strengthens the claim that a capacitively driven interconnect is more effective for higher interconnect lengths or the global interconnects.

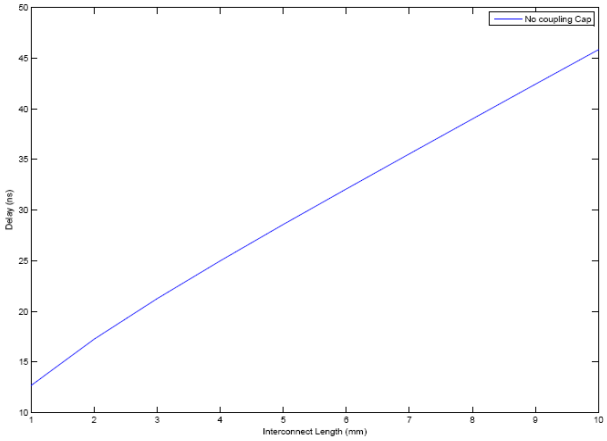


Fig. 10: Transmission Delay for Varying Interconnect Length without Coupling Capacitor.

Fig 11 shows the plot of delay v/s interconnect length for interconnects without coupling capacitor. It is clearly evident that the capacitively driven interconnect gives a better delay performance as against the normal interconnect. However, the advantages of capacitively driven v/s normal interconnect are not prominent for shorter interconnects but as the interconnect length increases, the performance improves many fold and hence the claim of improved performance for global wires with capacitively driven interconnects is established.

6. Conclusion

This paper has attempted to improve the delay performance of driver-receiver circuits for driving longer bus interconnect lengths. The capacitively driven bus topology was used for improvement in delay performance. A driver-receiver topology for driving interconnects is first presented. Subsequently, the capacitively driven interconnect model is developed and introduced for simulations and the delay performance is studied. The paper presents the variations in delay for different design cases and establishes that the capacitively driven bus interconnect topology has contrasting advantages as compared to the normal interconnect for global wires.
The capacitively driven bus interconnect topology offers a 55% improvement in the delay performance, which is a substantial improvement in the global interconnect scenario.

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