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Research paper



Low voltage high speed 8T SRAM cell for ultra-low power applications

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Abstract

The usage of portable devices increasing rapidly in the modern life has led us to focus our attention to increase the performance of the SRAM circuits, especially for low power applications. Basically in six-Transistor (6T) SRAM cell either read or write operation can be performed at a time whereas, in 7T SRAM cell using single ended write operation and single ended read operation both write and read operations will be accomplished simultaneously at a time respectively. When it comes to operate in sub threshold region, single ended read operation will be degraded severely and single ended write operation will be severely degraded in terms of write-ability at lower voltages. To encounter these complications, an eight transistor SRAM cell is proposed. It performs single ended read operation and single ended write operation together even at sub threshold region down to 0.1V with improved read-ability using read assist and improved dynamic write-ability which helps in reducing the consumption of power by attaining a lower data retention voltage point. To reduce the total power consumption in the circuits, two extra access transistors are used in 8T SRAM cell which also helps in reducing the overall delay.

Keywords: *SRAM; Read-Ability; Write-Ability; Low Power; Read Assist; Pass Transistors and Delay.*

1. Introduction

Portable mobile electronic devices are mostly used in day to day lives which are equipped with batteries [1]. Power consumption is one of the main design metric in such devices. As power consumption increases, size of the battery and cost also increases, which in turn effects the compactness of the device. So, low power is the major requirement for portable systems. On the other side, Memory is the very important element in the embedded electronic systems which consume major part of system operation in terms of power. If the power consumption of memory is reduced, total power consumption [2] of system also reduced and hence size, cost, life and maintenance of the battery will be reduced and also system becomes more compact. Most of the researchers concentrated on low power memories for ultra-low power applications.

In CMOS technology, SRAM circuit plays a vital role in digital systems. The semiconductor type memory, which has bi stable latching circuitry is said to be Static Random Access Memory (SRAM). It can retain the data for one bit. SRAM cells are used for micro controllers and microprocessors. It mainly consists of two CMOS inverters with back to back connection, these inverters act as a memory cell whereas the remaining transistors act as access transistors. Bit and bit bar lines act as inputs and outputs. Every SRAM cell performs three basic operations, such as read, standby and write operations. In order to hold the data and to preserve the circuit in idle position, standby operation is performed. With the help of read-ability and write-ability, both read and write operations are performed in SRAM to read and write the data. In this paper, the power and delay are reduced in 8T SRAM cells when compared to standard 6T SRAM cell and conventional 8T SRAM. Delay is reduced by using read assist technique and Power is condensed by using two extra pass transistors. Here, the length and width of PMOS with 0.13µm and 0.52µm are used and the length and width of NMOS with 0.13µm and 0.26µm are used respectively.

2. Literature review

Gupta et al, [3] was proposed a scheme to increase the performance of seven transistor SRAM cell by performing read operation efficiently. But there is a delay during the read operation and the power dissipation is also very high. Budhaditya et al,[4] implemented a single bit line 6T SRAM cell, where there is high delay due to which the performance of read and write operations are severely degraded. Yang et al,[5] implemented 7T SRAM cell in Fin FET technology, but the power consumption is high. For low power applications Ansari et al, [6] designed a 7T SRAM cell, but didn't calculate power and overall delay. For low power applications, an 8T SRAM cell is implemented in this paper by using Read assist 8T and two extra access transistors of 8T SRAM. We calculated and compared SRAM's total power dissipation, read time, overall delay, write time and achieved low power consumption and lower delay comparing to the earlier works.

3. Low power design requirements

For portable devices, power is an important design consideration which plays a major role while designing VLSI circuits. There are different considerations that one would like to optimize about power. They are area, speed, testability, power dissipation, cost, risk and shielding. The power consideration is taken as an aspect along with the other two parameters: speed and chip design.

a) Area

Coming to the design considerations, area is directly proportional to the power. If the power consumption is reduced then the size of

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the battery in portable devices gets reduced. Which is in turns the area of chip also gets reduced.

b) Speed

If the power consumption is high in the circuit then the maintenance of the system should be done more times. As the maintenance increases, it yields to degradence of the speed.

c) Testability

A device is to be tested before being used. The device can be easily testable when it comes to be operated at lower voltages.

d) Power dissipation

If the circuit dissipates too much power then it becomes too hot or stops working. So, power minimization is the primary importance for portable devices equipped with batteries.

e) Cost

It is the main factor that should be in mind while designing the circuit. If the utilization of the power is increased then automatically the cost factor also increases.

f) Risk

The device which consumes high power is more risky when compared to the lower power electronic devices.

g) Shielding

For high voltage devices, the shielding for the circuit is compulsory to avoid power fluctuations whereas for low voltage devices high level shielding is not necessary.

4. Basic SRAM cell

In general, every SRAM cell consists of several MOSFET's. It has two cross coupled inverters and access pass transistors. These two inverters acts as a memory cell which is further transmitted or received to single bit of information. The memory cell will be operated by using access pass transistors; else it is in hold state. Whenever the access pass transistors are enabled by using word line, the memory cells operates both read and write operations. Bit line (BL) and bit line bar (BLB) are the inputs of the standard 6T SRAM cell, which are passing through the access pass transistors and to get the two outputs Q and QB (Q bar) of SRAM cell as shown in Fig 1.

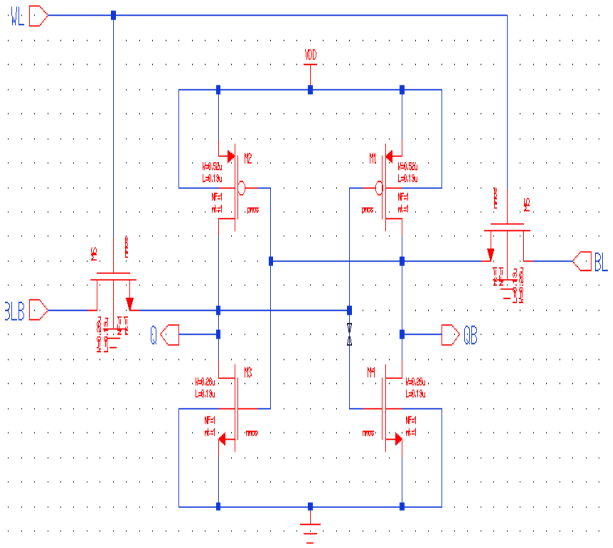


Fig. 1: Standard 6T SRAM Cell.

a) 6T SRAM cell working

In standard 6T SRAM cell, the two inverters are connected in back to back connection. The output of the first inverter is connected to the input of the second inverter and vice versa. Basically, SRAM performs three operations which are Hold, Read and Write operations. Whenever the two access pass transistors of the word line (WL) are in OFF state, then the bit line and bit line bar (BL & BLB) are also in OFF condition, hence the memory cell is in hold state .If both the bit and bit bar lines act as inputs then write operation can be performed. If both the bit and bit bar lines act as outputs then the read operation can be performed.

b) Read operation

In this circuit, if Q="1" and QB="0" then the word line gets enabled. Now bit and bit bar lines act as outputs and they are precharged [10] to VDD then Q="0" and bit bar voltage is VDD. The difference between bit bar voltage and Q voltage has some alteration in voltage which results in the decrease of bit bar voltage. Bit and bit bar lines act as a comparator when the bit bar value decreases then the output becomes "1".

c) Write operation

If Q="0" and QB="1" then the word line gets enabled. Now bit and bit bar lines act as inputs and bit bar line is connected to the ground. Now the voltage difference of the QB and bit bar will be less than threshold voltage M3 which results M3 in OFF state and M1 in ON state then the output Q="1".

5. Implementation of proposed 8T SRAM cells

An 8T SRAM cell contains two inverters, one inverter (M1-M3) and another one (M2-M4), which are linked mutually. Single-ended write operation is performed with the help of Access transistors (M5, M6) [11] and Single-ended read operation is performed by using two NMOS transistors (M7, M8). The write bit line bar, write bit line and write word line (WBLB, WBL, WWL) are used for accomplishing write operation. For achieving the read operation, a read word line (RWL) and a read bit line (RBL) are used. In this cell both read and write operations can be performed at sub-threshold region to an operating voltage at 0.1V.The structure of the proposed 8T SRAM cell is shown in Fig 2.

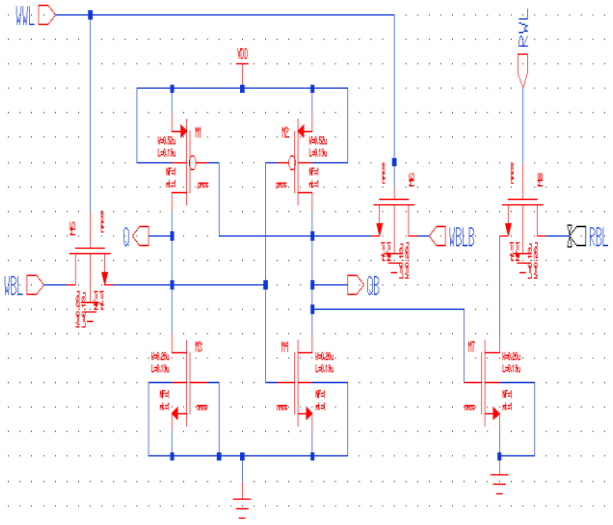


Fig. 2: Conventional 8T SRAM Cell.

a) 8T SRAM cell with Read assist

Read assist [12] 8T SRAM cell improves the readability by using read port (M7&M8).and gate terminal of the first inverter. If NMOS is connected to the ground then the node value of NMOS becomes "zero". As the Read Word Line (RWL) is enabled, the Read Bit Line (RBL) increases to high and by storing in Q node, the M7 NMOS is either turned ON or OFF. If the cell stores "1", then M7 is turned OFF and the bit line remained to be high. If we observe Fig 3, for bit line discharging through M7 and M8 in SRAM cell stores "0".

The two ends of operations in 8T SRAM cell are single ended read operation and single ended write operation respectively. For single ended write operation, Write Word Line (WWL) and the Write Bit Lines (WBL) are used. For single ended read operation, Read Word Line (RWL) and Read Bit Lines (RBL) are used.

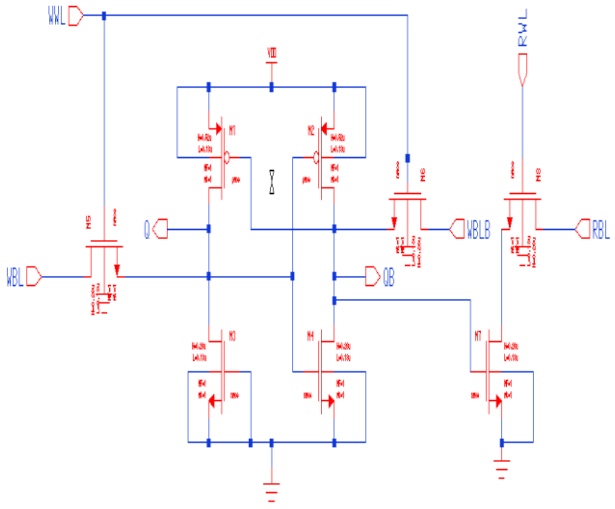


Fig. 3: Proposed 8T SRAM with Read Assist.

b) Proposed 8T SRAM using two extra pass transistors

In this technique, two extra pass transistors are merged at the two ends of the 8T SRAM cell to disrupt any short circuitry in the cell itself. If we observe Fig 4, In between VDD [13] and the cell, one PMOS is inserted with logic"0" [14] at the gate terminal. Likewise, an NMOS is inserted between the ground and the cell having logic "1" at the gate terminal. The total power [15] can be reduced in the 8T SRAM cell by using inserted two pass transistors.

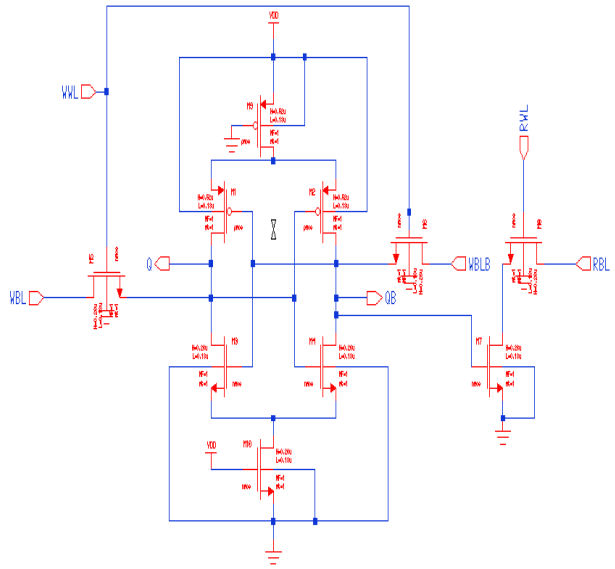


Fig. 4: Proposed 8T SRAM Using [2] Extra Pass Transistors.

6. Simulation results and discussions

The simulation results of Standard 6T SRAM cell, Conventional 8T SRAM, 8T SRAM with Read Assist and 8T SRAM using two Extra Pass Transistors are figured below. The waveforms and Fig 5, Fig 6, Fig 7, Fig 8 represents write and read abilities respectively.

Fig 5 represents the timing waveforms of Standard 6T SRAM cell and it consists of three inputs as word line (WL), bit line (BL) and bit line bar (BLB) and also two outputs as Q and Q bar (QB). Bit line (BL) and bit line bar (BLB) are act as inputs. Q and Q bar (QB) are act as outputs.

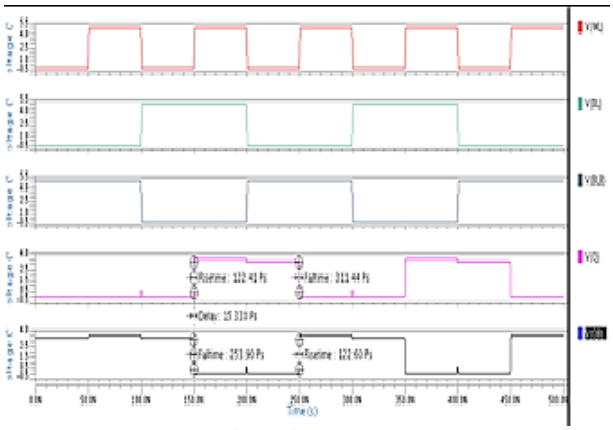


Fig. 5: A Waveform of Standard 6T SRAM Cell.

The write delay is measured between bit line bar (BLB) and Q whereas, the read delay is measured between bit line (BL) and Q bar (QB) as shown in Fig 5.

Fig 6, Fig 7, Fig 8 represent waveforms of Standard 6T SRAM cell, Conventional 8T SRAM, 8T SRAM with Read Assist and 8T SRAM using two Extra Pass Transistors. These SRAM cells consists of six inputs as write word line (WWL), write word line bar (WWLB), write bit line (WBL) and write bit line bar (WBLB), read word line (RWL) and read bit line (RBL) and also two outputs Q and Q bar (QB).

The write delay is measured between write bit line (WBL) and Q bar (QB). The read delay is measured between read bit line (RBL) and Q as shown in Fig 4,5,6,7 respectively.

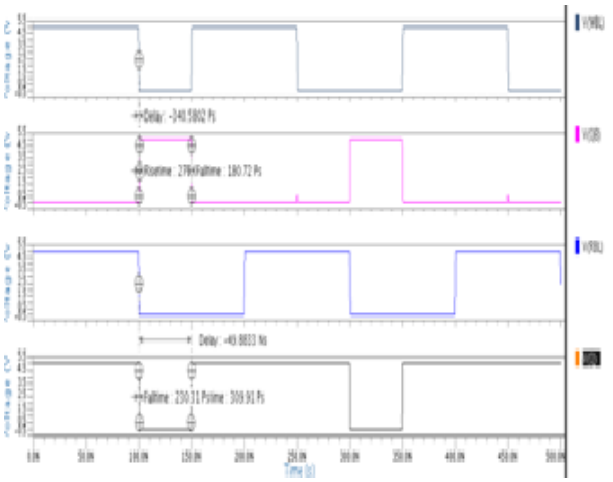


Fig. 6: Waveform of Conventional 8T SRAM Cell.

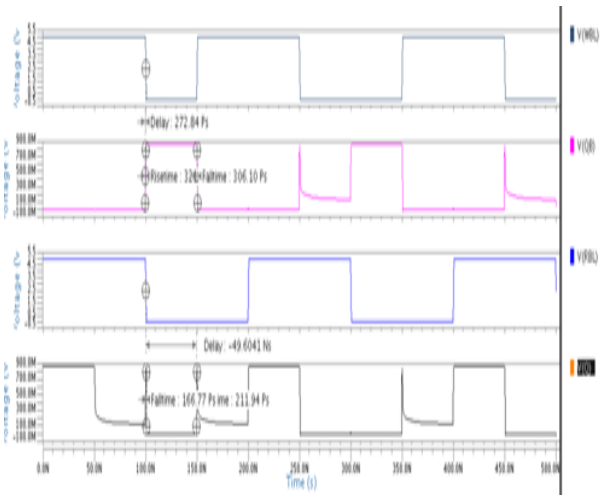


Fig. 7: Waveform for Proposed 8T SARM with Read Assist.

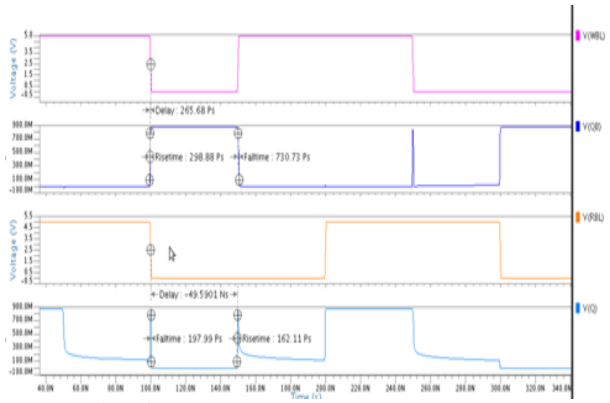


Fig. 8: Waveform for Proposed 8T SRAM Using [2] Extra Pass Transistors.

i) Delay Analysis

Table I: Represents the Overall Delay Between Input and Output of SRAM Cells. the Proposed SRAM Cell Designs Have Lesser Delay Compared to Existing SRAM Cell

Applied Voltage	Standard 6T SRAM cell	Conventional 8T SRAM	Proposed 8T SRAM with Read assist	Proposed 8T SRAM using 2 Extra Pass Transistors
0.1V	273.78 PS	172.84 PS	49.591 PS	155.68 PS

ii) Power Analysis

Table 2: Depicts the Total Power Consumption of the SRAM Cells. The Proposed SRAM Cell Designs Have Less Power Compared to Existing SRAM Cells

Applied Voltage	Standard 6T SRAM cell	Conventional 8T SRAM	Proposed 8T SRAM with Read assist	Proposed 8T SRAM using 2 Extra Pass Transistors
0.1V	5.6280 µW	5.3201 µW	3.6867 µW	3.1286µW

If we observe

iii) Write and Read Time Analysis

Table 3: It Represents Write and Read Delay Time Analysis at Lower Operating Voltage 0.1V. The Proposed SRAM Cell Design Have Less Write and Read Delays Compared with the Existing SRAM Cells

Applied Voltage		Standard 6T SRAM cell	Conventional 8T SRAM	Proposed 8T SRAM with Read assist	Proposed 8T SRAM using 2 Extra Pass Transistors
0.1V	Write delay	273.78 PS	172.84 PS	49.591 PS	155.68 PS
	Read delay	402.35 PS	250.61 PS	142.63 PS	185.15 PS

Fig 9, Fig 10, Fig 11 and Fig 12 are the layouts of standard 6T SRAM cell, conventional 8T SRAM, proposed 8T SRAM with read assist and proposed 8T SRAM using two Extra Pass Transistors respectively. The layouts are physically validated by calibre tool of mentor graphics which contains DRC, LVS and PEX simulation and it can be used for manufacturing VLSI chips.

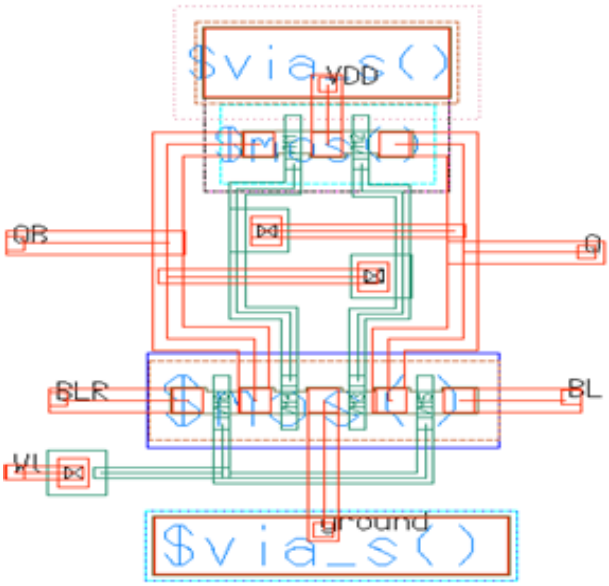


Fig. 9: Layout for Standard 6T SRAM Cell.

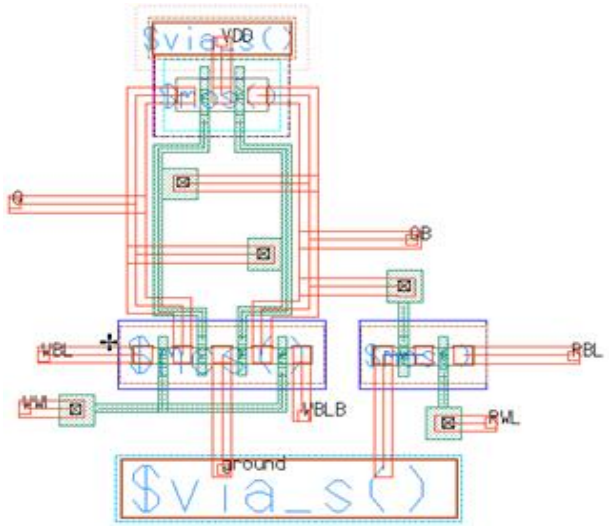


Fig. 10: Layout for Conventional 8T SRAM Cell.

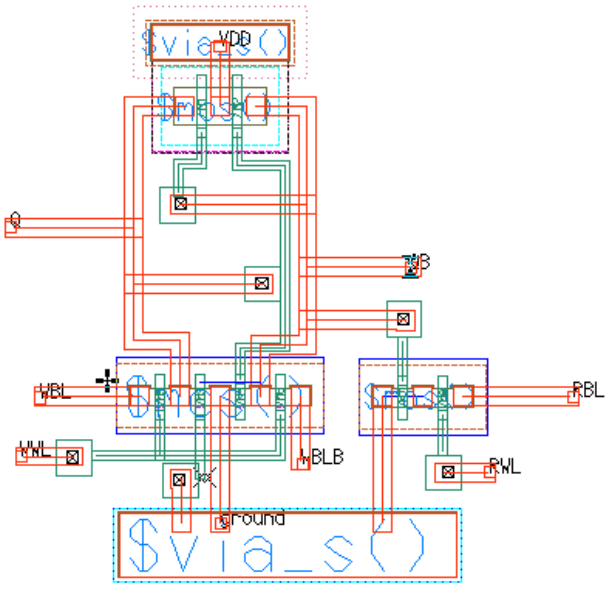


Fig. 11: Layout for Proposed 8T SRAM with Read Assist.

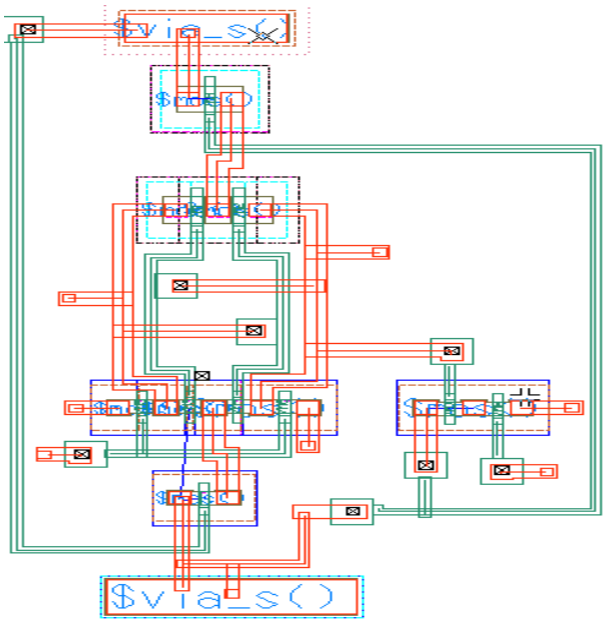


Fig. 12: Layout for 8T SRAM Using Two Extra Pass Transistors.

7. Conclusion

The proposed 8T SRAM cell can be very useful for ultra-low power applications operating voltage of 0.1V with reduced delay. The conventional 8T SRAM cell is modified in two ways to optimize power and delay. First, 8T with Read assist technique and second, 8T SRAM using two Extra pass transistors. These results are compared with Standard 6T SRAM and Conventional 8T SRAM cells. The delay of the proposed 8T SRAM with Read assist is reduced by 81.89% compared to 6T SRAM cell and reduced by 71.36% compared to Conventional 8T SRAM cell. The delay of the proposed 8T SRAM using two Extra pass transistors is reduced by 43.14% compared to 6T SRAM cell and reduced by 9.93% compared to Conventional 8T SRAM cell. The power of the proposed 8T SRAM with Read assist is reduced by 34.5% compared to 6T SRAM cell and reduced by 30.71% compared to Conventional 8T SRAM cell. The power of the proposed 8T SRAM using two Extra pass transistors is reduced by 44.42% compared to 6T SRAM cell and reduced by 41.20% compared to Conventional 8T SRAM cell. The ELDO simulation tool is used to verify these circuits. The schematic circuits and layouts are designed with the help of Mentor Graphics– a laboratory software tool.

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