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Research paper



Hardware realization of DVR with 27 level multi carrier PWM based MLI

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Abstract

The quality of the electrical power delivered to consumers is heavily affected by the power electronics based controllers, introduced in both domestic and industrial sectors, which in turn results in malfunctioning of equipment or eventual damage. Series compensators, Shunt compensators and series-shunt compensators are some of the strategies applied to address the power quality issues effectively. In this work a series compensating device, viz. 27 level-cascaded multilevel inverter based Dynamic Voltage Restorer (DVR) with multicarrier SPWM technique is proposed to mitigate voltage swells and voltage sags. The PWM technique used in this work is Alternate Phase Opposition PWM (APODPWM), which is one of the vertical arrangement multicarrier sinusoidal pulse width modulation techniques, to control the cascaded H-bridge inverter. The single-phase version of the proposed system is simulated to verify the effectiveness in addressing voltage issues and it is found that the obtained simulation results are satisfactory. The THD is found to be 3.40%, which is well below IEEE standards apart from considerable improvement in response time. The prototype of the proposed model is developed and the pic-micro-controller PIC16F887 is employed to implement the APODPWM. The experimental results obtained from the prototype are compared with the respective simulation results and they match with reasonable accuracy.

Keywords: *Multi Level Inverter (MLI); Alternate Phase Opposition Disposition Pulse Width Modulation (APODPWM); Dynamic Voltage Restorer (DVR); Sinusoidal Pulse Width Modulation (SPWM).*

1. Introduction

The quality of power depends mainly on the quality of voltage supplied to the customer and therefore, a reasonable maintenance of voltage quality assures power quality. However, the normal operations in industries such as starting/stopping of induction motors, energizing large capacitor banks and symmetrical/unsymmetrical line faults in power system cause voltage sags and swells, resulting the deterioration of voltage quality at the respective Point of Common Coupling (PCC). The sensitive loads connected to that PCC are heavily affected by the voltage degradation. Tripping of adjustable speed drives (ASD) and faulty operation of PLCs in automated industries are certain unwanted consequences of voltage sag and swell, resulting adverse monetary impact [1] [2] [3] [4].

DVR is one of the cost-effective solution to mitigate voltage issues such as voltage sags, swells and outages. A DVR system comprises of a PWM voltage source inverter (VSI), a series injecting transformer, a control circuitry and a DC source. Among all the components, VSI is the major component of a DVR [8] [9] [10] [11] [12]. The closeness of the output of the DVR towards the pure sine wave and the THD are decided by the number of levels in the VSI [5] [6] [7]. In this proposed work, a cascaded H-bridge multi-level inverter (MLI) configuration with 27 level is used as VSI in DVR with 13 full bridge configurations. The selection of proper modulation technique, modulation index and frequency ratio are key aspects for better performance of the VSI. Fundamental frequency modulation method is preferred in this work along with multi-carrier SPWM technique to reduce the switching losses and to improve THD [13] [14] [15].

Simulation of Single Phase DVR

Figure 1 shows the simulation model of the proposed single phase DVR in MATLAB-Simulink. The single-phase voltage source block acts as the generating station and transmission line is represented by a RLC series branch. The load is simulated by a series RL circuit. A series connected two winding transformer block with 1:1 ratio acts as injection transformer. A comparator module is used to compare the line voltage with reference voltage and to generate the error signal. This error signal is fed to the PI controller and the output of the PI controller is the modulating or reference signal for all the 26 comparators of the PWM generator. The repeating sequence block is used to generate the required 26 triangular carrier signals and their levels are shifted vertically by setting the corresponding block parameters and the phase difference between any two adjacent signals are 180°. Further, the carrier signals are so arranged that the peak magnitude of the lower signal is the lower level of its immediate upper signal. The output of any of the 26 comparators goes high once the magnitude of the reference signal is greater than that of the corresponding carrier signal. The 26 carrier signals are divided into two groups, separated by the reference line, such that the upper 13 signals fall in first group and the lower 13 signals in the second group and the reference line align with the x axis of the modulating signal. The outputs of the comparators serve as the triggering signals for all the 13 bridges of the MLI block. If the pair S_i^1 and S_i^4 of i^(th)bridge is excited by i^th carrier of first group the same i^th carrier from second group is used to trigger S_i^2 and S_i^3 pair of the same bridge. The output of the MLI Block, which is in fact the compensating voltage, is fed to the power line through the injection transformer.

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To introduce the voltage sag in the power line, an inductor of larger value is connected through a switch such that the closing of the switch at any time results in a voltage sag in the power line. The swell is introduced through a suitably programmed three phase programmable voltage source by tapping the output of any one of the three phases. Voltage measurement blocks and scopes are added at required points to capture the dynamics of the parameters such as line voltage, load voltage, injected voltage etc. The values assigned to various block parameters are given in Table 1.

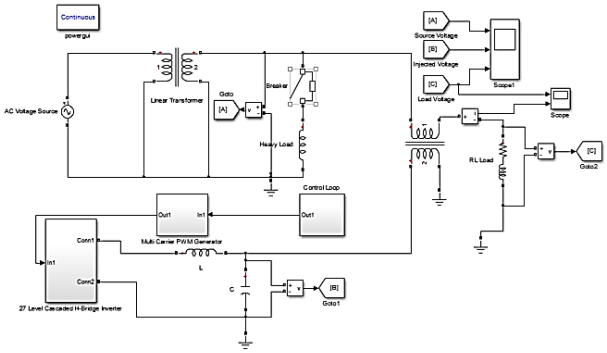


Fig. 1: Simulation Block Diagram of Single Phase DVR.

Table 1: Simulation Parameters of Various Block

S. No.	Name of the Block	Parameter	Value
1	Single Phase Voltage Source	V_{rms}	230 Volts
		Frequency	50 Hz
2	Transmission Line	Resistance	1.6 Ω
		Inductance	1.08 mH
3	Load	Resistor	100Ω
		Inductor	20mH
4	PI Controller	K_P	1.2
		K_I	0.5
5	Switching Device in MLI	Internal Resistance	1 mΩ
		Snubber Resistance	100 kΩ
		Snubber Capacitance	∞
6	Injection Transformer	Ratio	1:1
		Power	1.5 kVA
		Frequency	50 Hz
7	Triangular Carrier Signals	Frequency	12 kHz
		Peak Amplitude	5 Volts
8	Inductance for voltage sag	--	5 H
9	Three phase programmable voltage source to introduce swell	Phase Voltage	230 Volts
		Frequency	50 Hz

2. Simulation results and analysis

The total simulation period is assumed to be one second. The voltage sag is introduced at 0.3 second by switching on the heavy inductor. This pulls down the line voltage to 184 Volts, resulting a sag of 46 volts i.e. 20% sag, for a period of 0.2 seconds. Voltage swell is introduced at 0.7 second by suitably programming the programmable voltage source and it is made to last for 0.2 seconds, i.e. 20% swell for 0.2 seconds. Figure 2 shows the voltage captured at source side which clearly displays the sag and swell introduced at 0.3 second and 0.7 second respectively.

The output of the DVR, designed to mitigate the voltage issues, is shown in Figure 3. DVR maintains zero output as long as the line voltage is equal to its nominal value and once the deviation in the line voltage is sensed it injects the voltage to bring the line voltage back to its nominal value. From 0.3 second to 0.5 second it injects 46 volts in phase with line voltage so as to alleviate the voltage fall and maintains 230 volts at load side. Similarly, between 0.7 second and 0.9 second it injects same 46 volts, but 〖180〗^∘ out of phase so as oppose the line voltage to bring it down to its nominal 230 Volts. Figure 4 shows the voltage captured at load side and it is evident that the voltage applied to the load is maintained at its nominal value during the occurrence of faults and also irrespective of the nature of the faults.

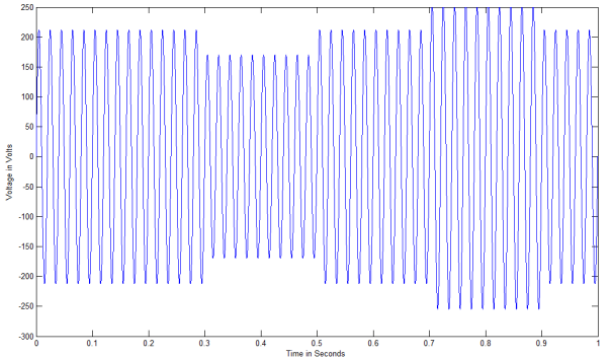


Fig. 2: Line Voltage with Sag and Swell.

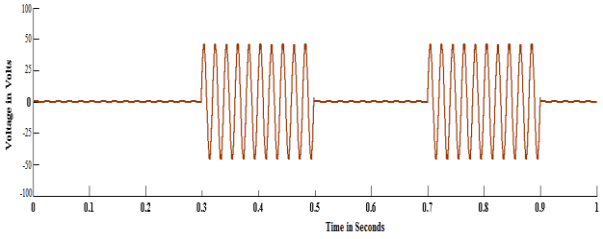


Fig. 3: Voltage Injected by DVR during Sag and Swell.

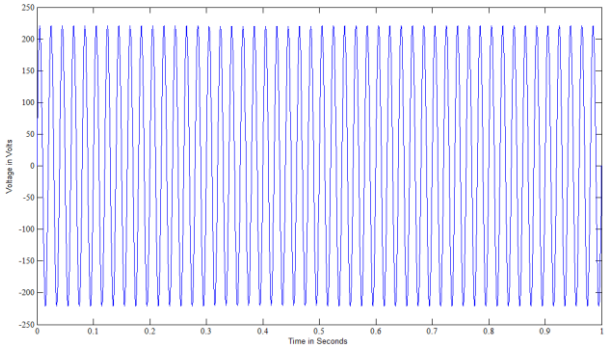


Fig. 4: Load Voltage after Compensation.

The switching transient observed during switching on and off the bridges is 50 Volts. It is also noticed that during the occurrence of the fault, that leads to either swell or sag in the line voltage, the time taken to restitute the voltage is only [2] milliseconds, a reasonably better value. From the Fourier series analysis of the load voltage shown in Figure 5, THD, the index that reflects the quality of the AC quantity injected, is observed as 3.40%, which is well below the IEEE stipulated standards. As the simulation of single phase, DVR gives satisfactory results it is decided to fabricate a low power prototype model of it to evaluate its effectiveness practically.

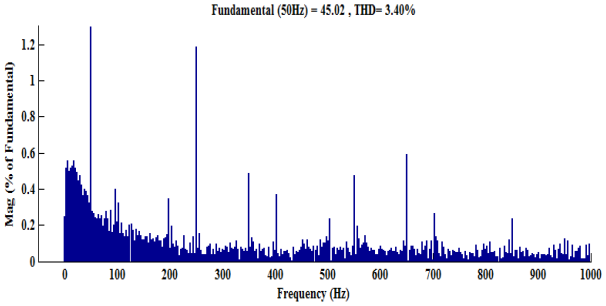


Fig. 5: Total Harmonic Distortion of Load Voltage.

3. Overview of hardware

The practical realization of the proposed DVR comprises of both hardware and software sections. In hardware part there are two major segments viz. Power Circuitry and Control Circuitry. Power Circuitry consists of hardware components such as switching devices, power transformers, load where as the control circuitry consists of soft mechanisms to generate the required PWM signals through PIC 16F887. MOSFET IRF840 is the power switching device selected and 13 H–Bridges are realized through 52 MOSFETs as shown in Figure 6. PIC Micro-Controller 16F887 forms the core of the control circuitry and PI control and PWM generation are realized through software. Proper isolation has been provided wherever required to protect the components and also for a better overall performance of the DVR.



Fig. 6: Hardware Setup of the Proposed System.

Hardware Description
A DVR for a capacity of 750 Watts is designed and fabricated to estimate the practical performance of the proposed version. The power line is realized through an autotransformer and the value of the connected load is Z_L=100+j62.8. By switching on an induction motor, voltage sag is introduced in the power line and it is observed the amount of sag is about 20% and lasted for 0.2 second without DVR. On the other hand, the swell is produced by increasing the line voltage using the autotransformer. The autotransformer is so adjusted that the amount of swell is 12% and being manual operation the swell lasts for considerable duration. Appropriate precaution measures are followed along with the isolation for the proper functioning of DVR during swell. The opto- isolator MCT 2E is used to provide isolation between the power circuit and PIC microcontroller based control circuit. The sag and swell in the realized power line are introduced separately one after another to assess the ability of prototype DVR.

4. Control strategy

PIC16F887 microcontroller performs all the control activities, such as analog to digital conversion, generation of reference voltage V_ref and comparison of the reference voltage with line voltage equivalent, PI processing and PWM operation to generate the gating pulses for the H-Bridges. The line voltage, reduced to 5 Volts through a transformer, is fed as the input for the analog to digital converter of the PIC microcontroller through channel 0. The digital equivalent of the reference voltage is stored in the internal register and the output of the analog to digital converter is compared with this reference. Then the error signal undergoes PI control algorithm and the output of the PI process is sent to PORT A which serves as the reference signal for PWM generation algorithm. PWM1, one of the two PWM generation modules of the PIC microcontroller is used to generate the required gating pulses for the 13 H-Bridges. Timer1 is used to generate the required carrier signal at 12 MHz frequency and the Timer output is compared with the contents of PORT A to generate the gating pulse for the first H-Bridge. The magnitude of the Timer output is then properly updated to get the second level of the carrier signal before comparing it with the contents of PORT A and this process is repeated for all the 13 levels, before next sample of the line voltage is taken. As the speed of the microcontroller is much higher than that of the power system being controlled, proper generation of the gating pulses is assured. The hardware arrangement of driver circuit and Inverter circuit is shown in Figure 7.

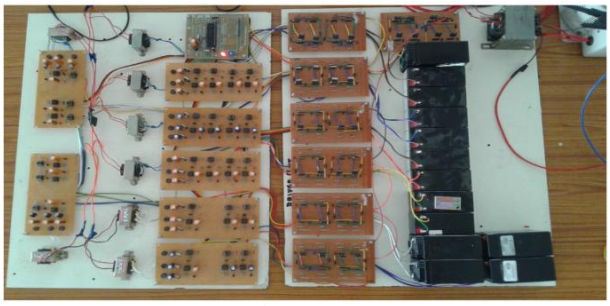


Fig. 7: Hardware Setup of Driver Circuit and Inverter Circuit.

5. Performance analysis

As discussed the voltage sag is introduced by switching on the induction motor whereas the swell is by adjusting auto transformer and both are depicted in Figure 8 and Figure 9 respectively. It is easily seen that the line voltage falls to 184 Volts i.e., 20% during sag. Similarly, the swell is observed as 12% i.e. the line voltage is raised to 258 Volts.

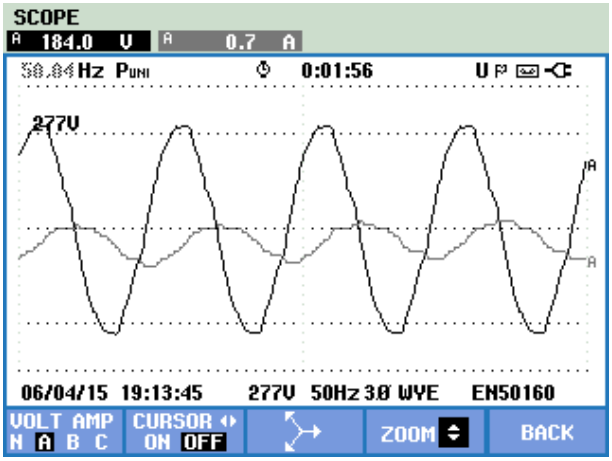


Fig. 8: Line Voltage with Sag.

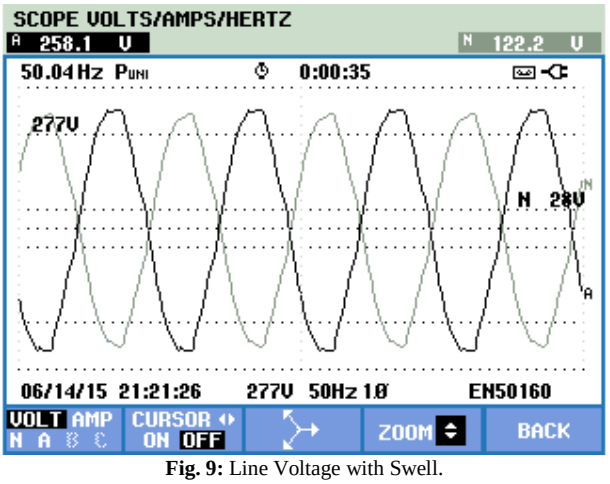


Fig. 9: Line Voltage with Swell.

To mitigate the voltage issues discussed, the DVR is introduced and the line voltages, observed with the DVR, are shown in Figure 10 and Figure 11. The line voltages observed from these figures are 230V each, which prove the effectiveness of the proposed DVR in

alleviating the sag and swell successfully. During sag, the magnitude of the voltage injected by the DVR is 46V and that of the swell is 28 V which may be estimated from the peak values of the respective compensating voltages shown in Figure 10 and 11.

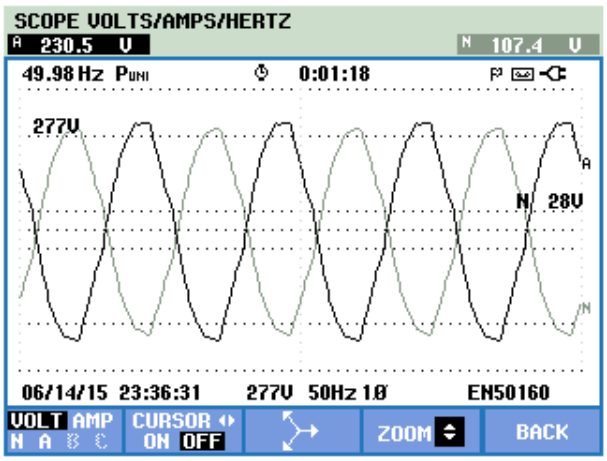


Fig. 10: Load Voltage after Voltage Sag Compensation.

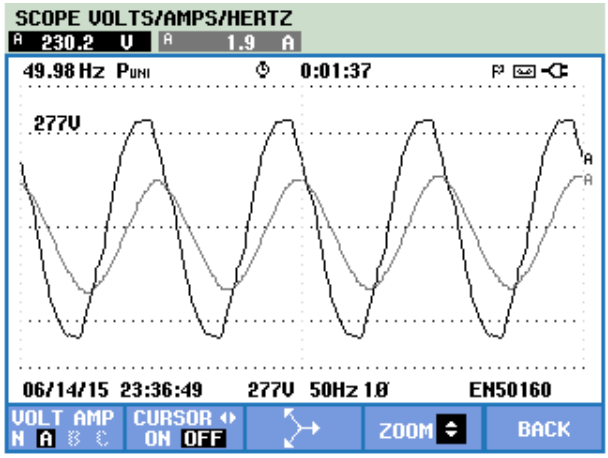


Fig. 11: Load Voltage after Voltage swell Compensation.



Fig. 12: Voltage Injected by DVR during Sag.

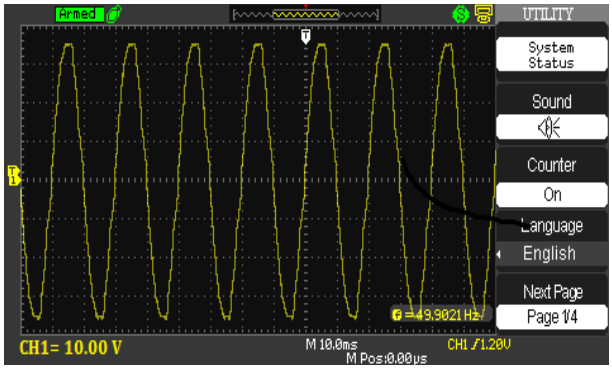


Fig. 13: Voltage Injected by DVR during Swell.

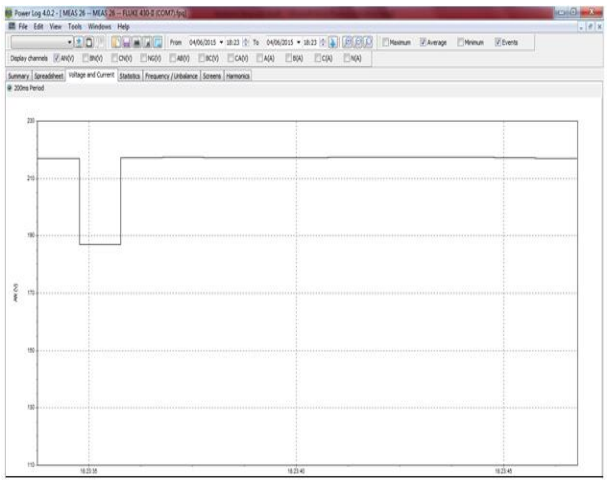


Fig. 14: Response Time of DVR.

It is also observed from Figure 14, that the time taken to restore the voltage by the DVR is only [2] milliseconds, an appreciable response time.

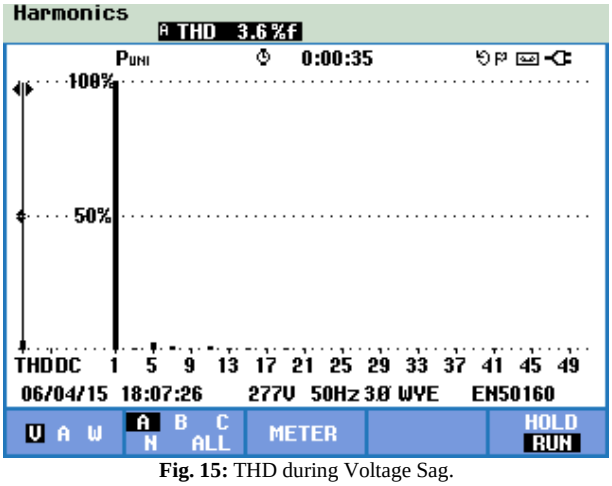


Fig. 15: THD during Voltage Sag.

The THDs measured during compensation of sag and swell are respectively 3.6% and 3.8% as shown in Figure 15 and Figure 16 and these values are well below IEEE standards.

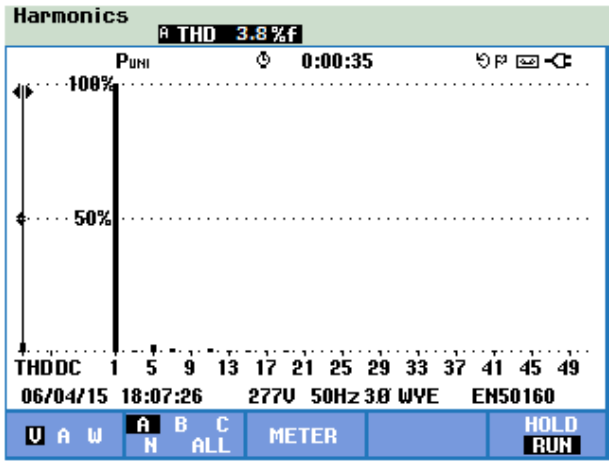


Fig. 16: THD during Voltage Swell.

6. Conclusion

The inevitable voltage sags and swells in power line are to be mitigated to protect the sensitive equipment connected to the power line and a 27-level cascaded H-bridge MLI based DVR is proposed in this paper for the same. The single-phase version of the proposed

DVR was simulated in MATLAB-Simulink and the performance observed was satisfactory. Hence, a prototype, with power MOSFET IRF840 to realize the VSI of the DVR, was fabricated with APODPWM as the modulation technique. The firing angles for the MOSFETS of the DVR were software controlled with the PIC Microcontroller PIC16F887. The voltage swell and sag were introduced manually and the effectiveness of the DVR in mitigating the same was observed. It was noticed that the proposed DVR was effectively functioning during both sag and swell conditions in bringing back the line voltage to its nominal value with an appreciable response time. The THD in both the cases were also well below the IEEE standards. It was also confirmed that the simulation results match with the experimental results, with negligible variations, as shown in

Table 2: This Configuration May be scaled for a Three- Phased System Also

S.No.	Fault	Simulation Results				Hardware Results			
		Line Voltage (V)		Injected Voltage (V)	% THD	Line Voltage (V)		Injected Voltage (V)	% THD
		Without DVR	With DVR			Without DVR	With DVR		
1.	Sag	184	230	46	3.4	184	230.5	46	3.6
2.	Swell	276	230	46	3.4	258	230.2	28	3.8

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