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Research paper



Design and Analysis of Heterojunction Tunneling Transistor (HETT) based Standard 6T SRAM Cell

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Abstract

Subthreshold Swing (SS) of MOSFETs, which determines the low voltage operation of portable mobile devices, cannot reduce below 60mV/dec that restricts MOSFETs for ultra-low power applications. This work presents design and implementation of high ON current, improved Miller capacitance and reduced subthreshold swing heterojunction tunneling transistors (HETTs) for portable electronic systems. The performance of HETT with MOSFET has been compared. In this work, the overlapping of gate oxide onto source can increase the band to band tunneling (BTBT) and improves the ON current of the transistor. Miller capacitance effect can be reduced by the use of low band offset materials and low energy states of materials like Ge or SiGe. This, in turn, results in better performance characteristics for the transistor.

The Proposed design and implementation of HETT include both N-type HETT (NHETT) and P-type HETT (PHETT) fabrications and the performance characteristics analysis of both NHETT and PHETT are provided. The advantages and limitations of both NHETT and PHETT for beyond CMOS technologies, in addition to the basic and structural differences between HETTs and conventional MOSFETs to facilitate the use of HETT in place of MOSFET have been elaborated in detail. The construction process of HETT is not at all completely different which is suitable to MOS Design process and is applicable for portable mobile applications. The power analysis of HETT based standard 6T SRAM cell is provided and the performance is verified with the conventional MOSFET based 6T SRAM cell.

Keywords: *Heterojunction Tunneling Transistor (HETT); 6T SRAM Cell; Band to Band Tunneling; Miller Capacitance; Subthreshold Swing; Low Power.*

1. Introduction

As the number of transistors placed on the silicon-die increase according to Moore's law [1], the power consumption of the IC also increases due to more chip activity. This, in turn, raises the temperature of the chip and restricts the chip activity. Therefore new power optimization techniques are required to maintain the chip activity and to limit the heat generated [2]. Voltage scaling is one of the best techniques to obtain required power efficiency, but it leads to high leakage current and low speed of operation [3]. On the other side, the limit on the subthreshold swing of MOS transistor cannot allow further scaling of threshold voltage [4] which results reduced ON-state current and limits ON to OFF state current ratio [5].

The best way to avoid above limitations is to use a TFET [6] in place of MOSFET to increase the performance of the chip. The TFET structure provides low leakage current, reduced subthreshold swing i.e. less than 60mV/dec and lower power consumption and it is operated at low supply voltage because of low band gap materials like Ge, SiGe or InAs [7]. The researchers are paying more interest towards TFETs as it is dominant in future IC technologies. But, the TFETs have low drive current in ON-state [8]. A heterojunction tunnel field effect transistor (HETT) [9] is used to overcome this limitation of TFET.

In HETT, BTBT [10-11] is high and hence ON-state drive current increases [12]. On the other side, lower power consumption, reduced subthreshold swing, and less leakage current can be more easily obtained. Further scaling of the transistor [13] is also possible and hence more compact size can be obtained. In this, the gate oxide is overlapped on to the source to increase the BTBT and to improve the Miller capacitance [14-15]. Therefore the performance of the chip can be improved and hence HETT is one the best alternatives of MOSFET for beyond-CMOS technologies.

In this paper, the design and implementation of n-type HETT (NHETT) and p-type HETT (PHETT) has been provided in detail. The volt-ampere characteristics and transfer characteristics of MOSFET are discussed. The timing performance and power analysis of NHETT and PHETT are verified by using Standard 6T SRAM cell.

2. HETT structure design and implementation

In HETT, instead of Si, if low band gap materials such as Ge or SiGe are used, then ON to OFF state current also improved. The epitaxial technique is used for the manufacturing of HETT. The SiGe and the surface Si layers are formed by using CVD (Chemical Vapor Deposition). The top Si and surface Si layers thicknesses are in the range of 20nm to 30nm and that of SiGe layer is 20nm to 50nm. The SiGe layer consists of Ge content which is in the range of 10% to 25%. SiGe or Ge layer thickness is in the range of 5nm to 20nm. The thickness of the film is well under control from 5nm to 20nm. Oxygen and Nitrogen are used in the process of oxidizing and annealing respectively. 1005° C to 1100° C of temperature is required for both these processes for the first stage of oxidizing and annealing whereas for the second stage is 900° C to 950° C and the time required for both the cases is about 0.5 hours to 1 hour. Thermal phosphoric acid etching is used to

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remove the Si3N4 layer and Hydrogen Fluoride (HF) etching is used to remove the SiO2 layers.

HETT consists of Silicon on Insulator (SOI) substrate with top Si surface layer and BOX layer and a back substrate, a gate which is deposited on the top surface of Si, an active region which is below the gate in which the active areas composed of a SiGe or Ge region for source and Si region for drain and in between two active regions a Ge/Si heterojunction is formed. The gate consists of the SiO2 insulating layer on the surface of Si layer and the gate electrode is deposited on the SiO2 insulating layer.

There are two possibilities of transistors: one with source as P-type and drain as N-type regions and another one with source as N-type and drain as P-type regions. For both these transistors, boron (B) and boron difluoride (BF2) is used as the doping element for the P-type region and whereas phosphorus (P), arsenic (AS), or antimony (Sb) for N-type region. Ion implantation and thermal or laser annealing are performed for the N-type and P-type doping processes.

Increased ON-OFF state current is obtained since the source is formed in SiGe or Ge region and drain is formed in Si region. The device fabrication process is simple and is well suitable for present CMOS fabrication process without changing the technology and hence it can be used in industrial applications for the mass production of ICs with reduced cost. Fig. 1 and fig. 2 shows the schematic structures of N-HETT and P-HETT.

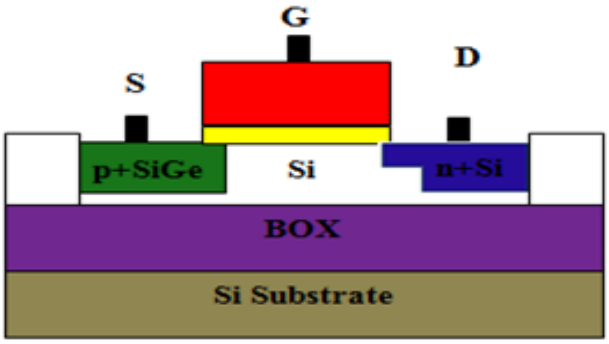


Fig. 1: Structure of N-HETT.

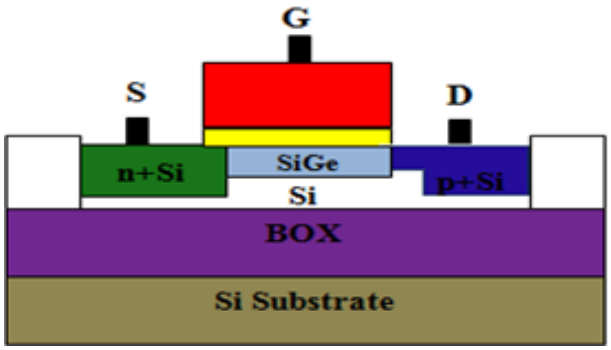


Fig. 2: Structure of P-HETT.

In VLSI design, circuit logic and memory elements are the main components. HETT based SRAM is proposed for the memory design of low power systems because of low leakage and high drive current with improved Miller capacitance. Standard 6T SRAM cell consists of two crossed coupled inverters with two access pass transistors. Conventional MOSFETs in this structure are replaced by HETTs for improving the performance of SRAM by reducing the leakage power.

The schematic circuits and layouts of both standard and HETTs based 6T SRAM cells are shown in fig.3, fig.4, fig.5 and fig.6. The physical verification of the layout design can be done using Calibre tool of mentor graphics that includes DRC, XRC, and LVS. These layouts are used by the manufacturer in the physical fabrication of low power VLSI chips. The layouts and schematic circuits are designed and implemented using 130 nm Technology - a mentor graphics tool.

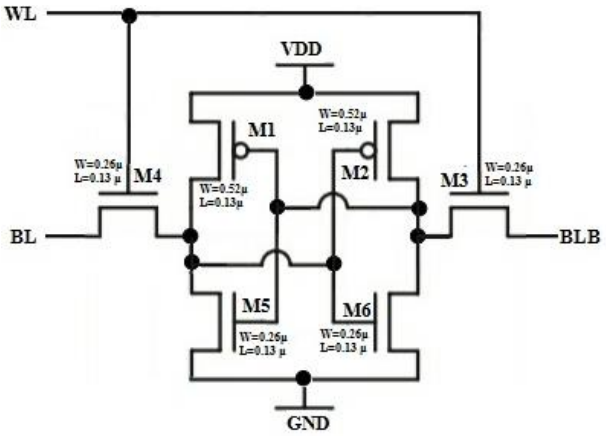


Fig. 3: Standard 6T SRAM Cell Schematic Circuit.

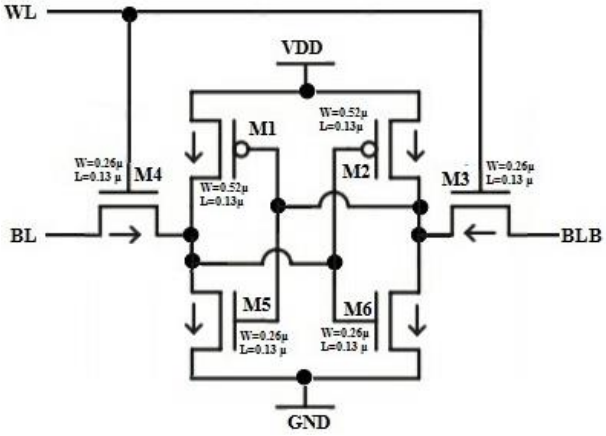


Fig. 4: HETT Based 6T SRAM Cell Schematic Circuit.

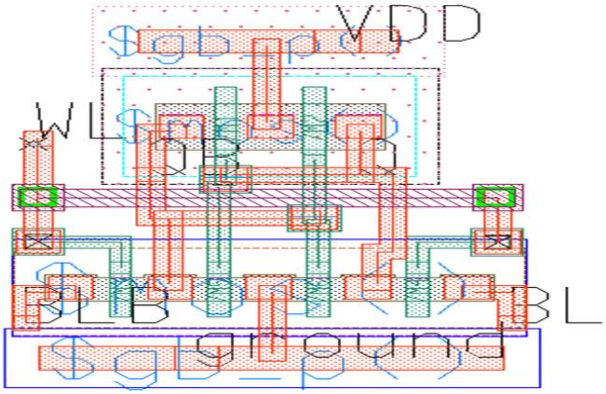


Fig.5: Standard 6T SRAM Cell Layout.

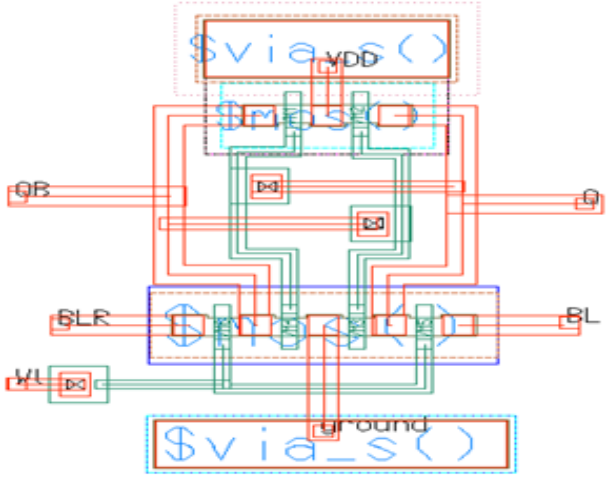


Fig.6: HETT Based 6T SRAM Cell Layout.

3. Results and discussion

NHETT and PHETT with gate oxide overlapped onto source are designed and the performances of these devices are verified by implementing HETT based 6T SRAM; the results are validated with standard 6T SRAM cell. The table 1 exhibits the standard 6T SRAM cell topology power analysis i.e. average power consumed, maximum power and minimum power at different temperatures.

Table 1: Standard 6T SRAM Cell Power Analysis

Temperature	Average power consumed (watts)	Maximum power (watts)	Minimum power (watts)
0°C	0.804770e-6	38.71789e-6	0.0081687e-6
10°C	0.861380e-6	40.12487e-6	0.0672551e-6
25°C	1.092882e-6	51.22267e-6	0.1277842e-6
40°C	1.696481e-6	54.14799e-6	0.0356692e-6
50°C	1.887441e-6	55.78707e-6	0.2186169e-6
60°C	1.945122e-6	41.24576e-6	0.2451220e-6

Table 2 exhibits the proposed HETT based 6T SRAM cell topology power analysis at different temperatures.

Table 2: Proposed HETT Based 6T SRAM Cell Power Analysis

Temperature	Average power consumed (watts)	Maximum power (watts)	Minimum power (watts)
0°C	0.717221e-6	38.7303e-6	0.0082822e-6
10°C	0.808901e-6	40.9591e-6	0.0642465e-6
25°C	0.933907e-6	48.4637e-6	0.0132411e-6
40°C	1.047729e-6	48.0325e-6	0.0268350e-6
50°C	1.132893e-6	48.0325e-6	0.0268350e-6
60°C	1.302309e-6	35.3850e-6	0.0409720e-6

The average power consumed of the proposed HETT based 6T SRAM cell is reduced at different temperatures compared to standard 6T SRAM cell and is shown in table 3 and comparison of average power consumed is shown in fig.7.

Table 3: Average Power Consumed of Standard and HETT based 6T SRAM Cells

Temperature	Average power consumed of Standard 6T SRAM cell (watts)	Average power consumed of HETT based 6T SRAM cell (watts)
0°C	0.804770e-6	0.717221e-6
10°C	0.861380e-6	0.808901e-6
25°C	1.092882e-6	0.933907e-6
40°C	1.696481e-6	1.047729e-6
50°C	1.887441e-6	1.132893e-6
60°C	1.945122e-6	1.302309e-6

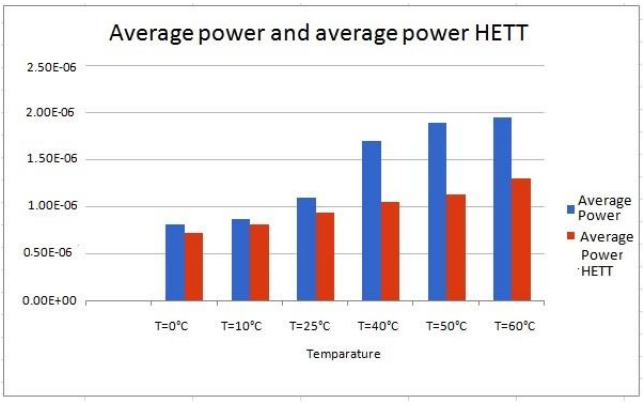


Fig.7: Average Power Consumed Comparison of Standard and HETT based 6T SRAM Cells.

The maximum and minimum powers of the design plays an important role in the low power VLSI design and are described as follows

The maximum power of the proposed HETT based 6T SRAM cell is reduced at different temperatures compared to standard 6T SRAM cell and is shown in table 4 and comparison of maximum power is shown in fig.8.

Table 4: Maximum Power of Standard and HETT Based 6T SRAM Cells

Temperature	Maximum power of Standard 6T SRAM cell (watts)	Maximum power of HETT based 6T SRAM cell (watts)
0°C	38.71789e-6	38.7303e-6
10°C	40.12487e-6	40.9591e-6
25°C	51.22267e-6	48.4637e-6
40°C	54.14799e-6	48.0325e-6
50°C	55.78707e-6	48.0325e-6
60°C	41.24576e-6	35.3850e-6

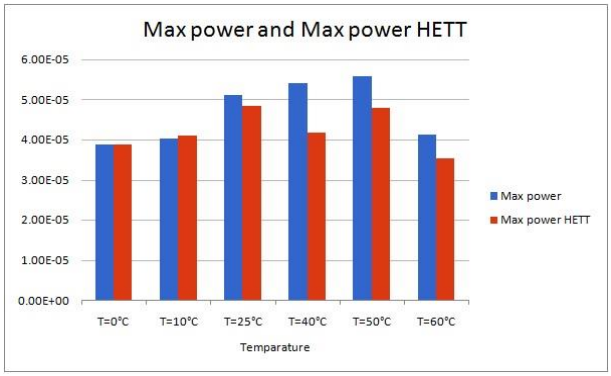


Fig.8: Maximum Power Comparison of Standard and HETT Based 6T SRAM Cells.

The minimum power of the proposed HETT based 6T SRAM cell is reduced at different temperatures compared to standard 6T SRAM cell and is shown in table 5 and comparison of minimum power is shown in fig.9.

Table 5: Minimum Power of Standard and HETT Based 6T SRAM Cells

Temperature	Minimum power of Standard 6T SRAM cell (watts)	Minimum power of HETT based 6T SRAM cell (watts)
0°C	0.0081687e-6	0.0082822e-6
10°C	0.0672551e-6	0.0642465e-6
25°C	0.1277842e-6	0.0132411e-6
40°C	0.0356692e-6	0.0268350e-6
50°C	0.2186169e-6	0.0268350e-6
60°C	0.2451220e-6	0.0409720e-6

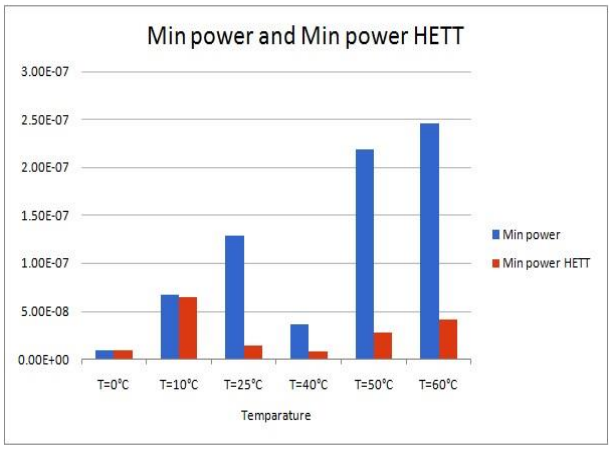


Fig.9: Minimum Power Comparison of Standard and HETT Based 6T SRAM Cells.

From figure 7, figure 8 and figure 9, it is observed that average power consumed, maximum power and minimum power of HETT based 6T SRAM cell is reduced compared to standard 6T SRAM cell above 40°C temperature and hence these HETT based SRAM cells can be more useful at high temperature low power industrial applications like nuclear reactors, welding, melting, boiling etc. Since HETT provides high ON current, low leakage and improved Miller capacitance with reduced subthreshold; it is useful for ultra low power applications.

4. Conclusions

A Heterojunction Tunneling Transistor (HETT) with gate oxide overlapped onto source to increase ON-state current and to decrease leakage power with improved Miller capacitance was proposed. To overcome the circuit limitations of MOSFET for beyond-CMOS technologies, HETT becomes the best alternative. HETT based 6T SRAM cell for ultra-low power applications was presented in this paper. The power analysis of HETT based SRAM cell is provided at different temperatures and the performance is validated with conventional Standard 6T SRAM cell. The design is fully CMOS-compatible and preferable for low power memory implementations because of low leakage power. Combination of both CMOS and HETT technologies are suitable for portable digital logic systems, preferably HETTs for low leakage power and CMOS for performance.

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