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Research paper

An Evaluation of Bidirectional Converter Topologies for Ups Applications

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Abstract

This paper emphases on different four topologies of Non-Isolated Bidirectional converter which are being equated for its suitability in the application of UPS. The evaluation is based on efficiency, number of switches and voltage gain used in the converter. The working philosophies and design equations of topologies are discuss in detail. The comparative studies and simulation results are deliberated for Boost mode. All the topologies of the low voltage side and high voltage side are connected with 24V battery and 260V DC bus with switching frequency 30 kHz.

Keywords: *DC- DC Converter, Non-isolated Bidirectional converter, Uninterruptible Power Supply, Topology Comparison*

1. Introduction

The A DC-DC converter have lately established a lot of devotion due to the growing need to the system with the capability of energy transfer which delivers the functionality of two unidirectional converters in a single converter unit that name as bidirectional converter. The non-conventional energy cannot afford stable power to the load; the batteries are used for satisfactory power. The complete power of the energy cannot be used totally by the load some number of power can be used to control the battery [5]. In order to discharge and charge the battery, a bidirectional converter is required which transfer the energy between two supplies in both directions [6].The bidirectional converters can be categorized into non-isolated and isolated categories. In isolated types, the chief anxieties are current stresses, high switching losses, conduction losses and excessive voltage [11]. To overcome these troubles non isolated Bidirectional DC Converter topology advanced which are adequate due to high efficiency enhancement, highly cost effective, volume of the system and reduction in weight [8]. DC converters are broadly used in numerous industrial users such as aerospace, electric vehicles, UPS, PV and several other appliances [3], [7], [9]. The main block diagram of converter system is presented in Figure 1. In standard mode the power flows between sources to load and also duties the battery, if any faults happen the source gets disconnected then the battery discharges and delivers power to the load. Between several topologies applied for different applications, four topologies are nominated and matched to provide the comparative estimation of the systems.

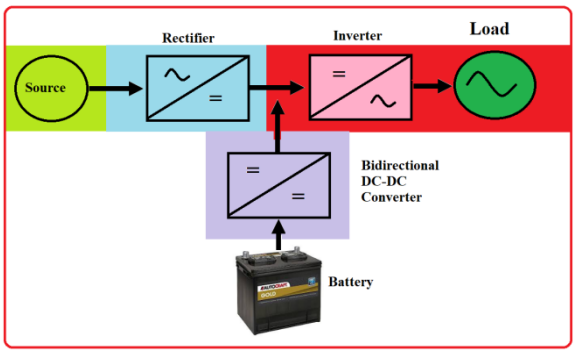

Figure 1: Block diagram of UPS

In this paper, segment 2 labels the analysis of different bidirectional dc converter topologies and working principle. In segment 3, discuss about design specifications data and in segment 4, simulations of the different bidirectional dc converter topologies are supported using MATLAB and the Final segment compared both Mode.

2. Operating Principles of the Topologies

The operation and analysis of the four topologies are explained for both Boost and Buck mode.

2.1. Topology 1

A non-isolated converter with ripple free inductor and fixed switching frequency a is displayed in Figure 3.It operates with

auxillary circuit path that involves of an additional winding to the main and an auxillary inductor of systems. The ripple free inductor reduces its voltage ripple [2].

The Boost mode initiates with turn of S. Time intervel of this mode is very short because of the value of C1 and C2 are very small. The swtiching voltage of converter is vary linearly that same time current should be constant. Now the swtich ON. Voltage of switch VS2 is sustained as zero at the instant of the switched -ON S2., turn on of S2 is ZVS achieved. Then the magnetising current im and inductance LM is VLO increases linearly. Now voltage reach zero is moment the switched ON in Swtich S1. In this mode the magnetising current im decreases linearly.

The voltage gain is $$\frac{V_{HI}}{V_{LO}} = \frac{1}{(1-D)} \quad (5)$$

From the indutor current modes of operation can be obatined, using those inductor current equations Ls can be modified as [2]

$$L_S < \eta(1-n)V_{L0}\frac{DT}{2P} \quad (6)$$

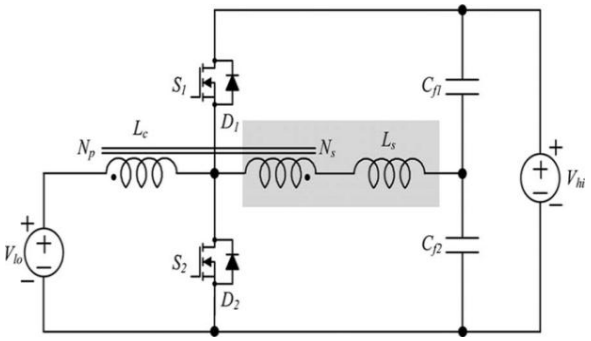

Figure 2: Topology 1

2.2. Topology 2

The topology 1as displayed in Figure 2 is a mixture of boost converters that are charity to improve the voltage gain. It covers four semiconductor switches and their diodes, capacitors and two inductors used to split the input current which is reasons the improving efficiency. Two of the switches are power semiconductor switches and the lasting acts as synchronous rectifiers [1].

In Boost mode, the switches are S3, S4 are switch off and the switches are S1 ,S2 are switch on. The DC source VL is voltage is transfer into inductor L2, Inductor L1 is magnetized by the DC voltage source and the charge is stored in capacitor. At same time Capacitor CH on load side is also discharged to the load.

The voltage gain is $$\frac{V_H}{V_L} = \frac{1}{(1-D)^2} \quad (1)$$

In buck mode, the S1, S2 are switch off and switches S3 ,S4 are switch on condition. The DC source VH is transmitted to inductors L1.at same time Capacitors C is discharged to inductors L2 and capacitors CL on battery side.

The voltage gain is $$\frac{V_L}{V_H} = D^2 \quad (2)$$

The inductors can be found from the current ripples of the inductors L1 and L2by using form of integral current equation [1].

$$L_1 \geq \frac{(1-D^2)R_L}{2D^2 fs} \quad (3)$$

$$L_1 \geq \frac{R_L}{2fs} \quad (4)$$

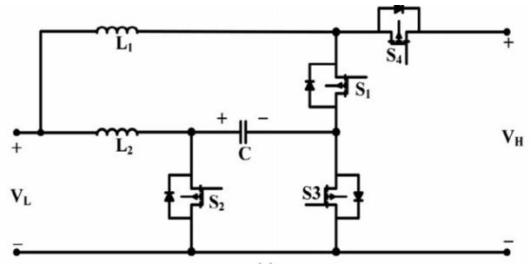

Figure 3: Topology 2

2.4. Topology 3

Topology for discharging and charging the battery over single circuit in applications of UPS and modern electric vehicles is given in Figure 5. This zero-voltage switching condition converter operate both mode provides large voltage diversity. This enables boosting the low voltage of battery to high voltage dc, and it's achieved by the only three switches, additional voltage clamped and coupled inductor [10].

In Boost mode, switch S1,diode DS3 are switched on. The power stored in the leakage inductor LK2 is unrestricted to C2, and iLK2 and (iS3) are steadily reduced. The voltage of battery VL issues energy into the inductor leakage LK1. Thus, the leakage inductor current iLK1 quickly rises. The magnetizing-inductor current iLM and the leakage-inductor current iLK1 are linearly increased. S1 is switched off, and DS2 and DS3 are switched on. The power of Lm is unconfined into CH via the coupled-inductor and DS3. ILM linearly reductions, and the energy stored in capacitor C2 is transferred to CH and RH.

The voltage gain is, $$\frac{V_H}{V_L} = \frac{2+nD}{1-D} \quad (11)$$

In Buck mode, switches S2 ,S3 are switched on, D4 is switched off. The voltage source VH charges through the inductor LM. The voltage across the primary winding linearly increase because of primary voltage is equal to VP. The DC bus voltage releases its power to capacitor C2, CL, and resistor RL. If S2 and S3 are switched off, and DS1 is switched on. Inductor LM not only releases its power into capacitor CL and RL but also transfers power to capacitor C2 via NS and D4 so its linearly decreases.

The voltage gain is, $$\frac{V_L}{V_H} = \frac{D(1-D)}{2n(1-D)^2+1} \quad (12)$$

The inductor should be premeditated as high adequate to minimize the ripples with low losses. The inductor ripple current is obtained from minimum critical inductance can be, output inductor current, average input [12].

$$L_M = \frac{D(1-D)2}{2n^2}T_S \quad (13)$$

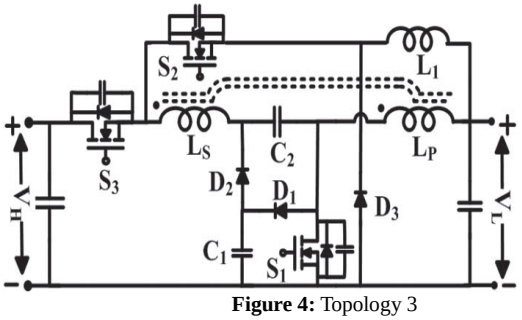

Figure 4: Topology 3

2.3. Topology 4

The converter displayed in Figure 4 uses the coupled inductor performance to succeed simple control with high conversion ratio. In discharging of the converter entertainments as two setup

converter by regulatory one semiconductor switch to attain high boost voltage conversion. The charging mode the system performances as two stepdown converters that control two semicondutor switches instantaneously to reach high step down voltage conversion. In predictable buck-boost dc dc converter the adaptation ratio is pointedly summary by parasitic features. Coupled inductor reasons high power switches because of energy stored on the leakage inductor [12].

During Boost mode the dc dc converter operate steps up the low battery voltage to high dc lvoltage. Switch S2 off conditon during this mode. Switch S3is OFF and S1 is ON and the low voltage battery is operate on the low voltage circuit. If S1 is switched off, the primary iLP charges the freeloading capacitances across switch S1, the secondary current iLS discharges the paracitic capacitances across switch S3. The starting current to reductions while the secondary side current rises because of leakage inductance. Energy transfer to high voltage side circuits from L,C2 are now connected in series circuit,

The voltage gain is $$\frac{V_H}{V_L} = \frac{n}{(1-D)} \quad (7)$$

During Buck operatig mode switch S3 remains ON but the switches off both S1 and S2. The current flows complete the C2 and both fixed inductor winding from high voltage to the low voltage side. Now low voltage side is D3 is conducting with continous inductor current iL1 into the low voltage side. The attached inductor is reversed,because of S3 turns off, the polarities reversed. The S2 turn on with body diode of to possess the current iLS flowing S1 diode also switch on. While the primary current iLP remains same, then the secondary current iLS decreases. The low voltage side of the circuit through switch S2 and inductor L1, When S1 and S2 turns on C2 starts discharging across. Thus, discharging capacitor C2. Clamp capacitor C1 also discharges concluded D2 by adding minimum current i3 into the the low voltage.

3. Design Data Specifications

The Table 1 lists the design constraints of all the topologies. The switching frequency, high side and low side of the voltage , the same values for all the selected topologies. The device values are designed with benefit of above declared analysis.

Table 1: Design data specification

Parameters	Topology structure 1	Topology structure 2	Topology structure 3	Topology structure 4
VL / VH	24V / 260 V	24V / 260 V	24V / 260 V	24V / 260 V
P0	500 W			
FS	30 KHZ			
L	LS = 1.3Mh	L1 ≥ 900mH L2 ≥ 9.5µH	L2 ≥ 80µH	L1 = L2 = 1 µH
C	C1 ≥ C2 ≥3.3 µF	C1 ≥64µF CH=CL ≥ 96µF	C2 ≥ C1 ≥4.4 µF	CL ≥ 220 µF C2 ≥ CH ≥330 µF

4. Simulation and Results

The simulation results is supported out using MATLAB software. In topology 1 the input Gate pulse to switch 2 which are being exact during Boost operation with a duty cycle of 0.6 is given in Figure 10 and its equivalent input and output waveforms are listed below in Figures 11-13 .

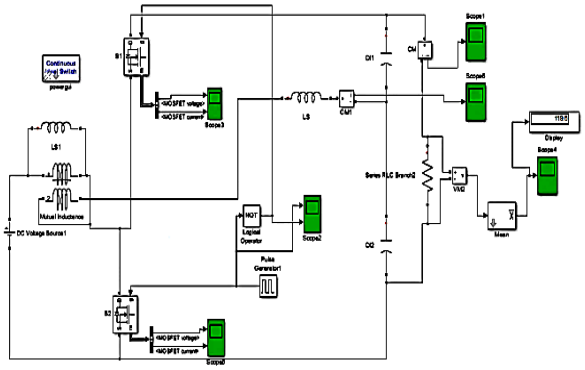

Figure 10:. Simulation model of Boost mode for topology 2

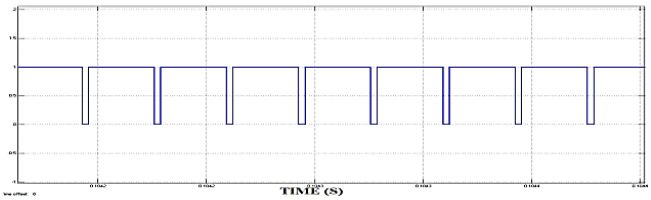

Figure 11: Gating signal for Boost mode of topology2

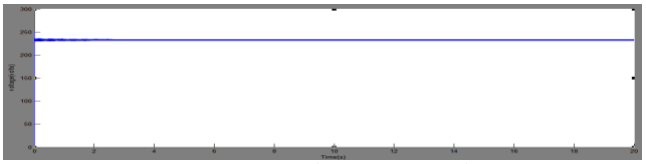

Figure 12:.Output voltage for Boost mode of topology2

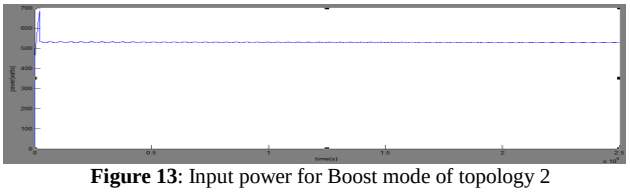

Figure 13: Input power for Boost mode of topology 2

From the above waveforms, for a given the output voltage obtained as 240 V, input voltage of 24 V which is shown in figure 12. The input power is 547 W in figure 13 due to the large amount of current drawn at the input side for a given output of 500W.

In Topology 2 the input pulse to switches 1 and 2 which are being exact during Boost mode of operation with a duty cycle of 0.69 is given in Figure 6 and its equivalent input and output waveforms are listed below in Figures 7-9.

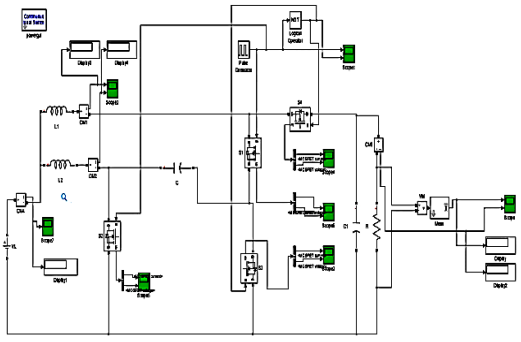

Figure 6: Simulation of Boost mode for topology 1

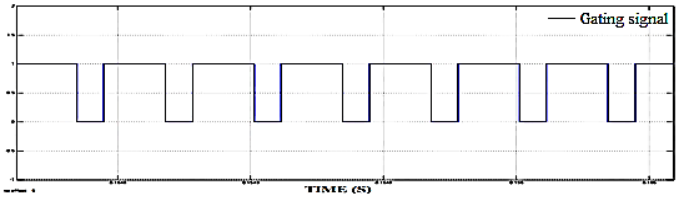

Figure 7. Pulse signal for Boost mode of topology1

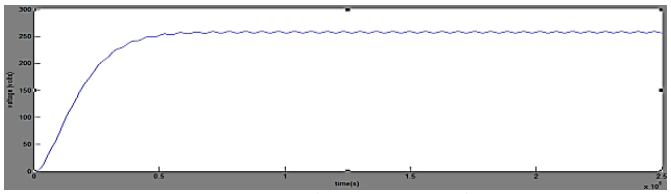

Figure 8: Output voltage for Boost mode of topology1

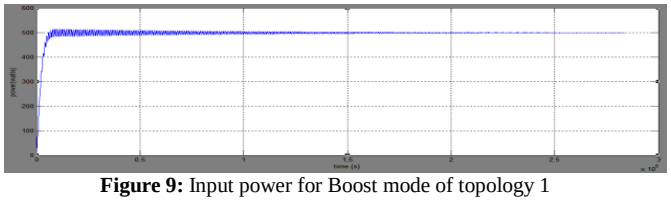

Figure 9: Input power for Boost mode of topology 1

From the above waveforms, for a given the output voltage obtained as 250 V from the input voltage of 24 V which is shown in figure 8. Once the converter is switched on, there is large amount of current flows at the input side. For a given the input power is drawn to 550 W output power of 500W.

In topology 3 the input pulse to switch 2 which are being exact during Boost operation with a duty cycle of 0.58 is given in Figure 18 and its equivalent input and output waveforms are listed below in Figures 19-21.

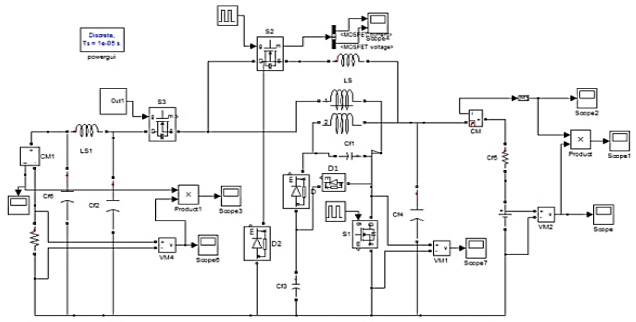

Figure 18: Simulation model of Boost mode for topology 4

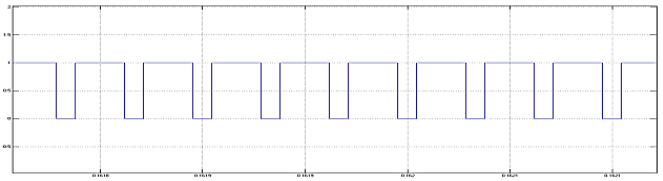

Figure 19: Gating signal for Boost mode of topology 4

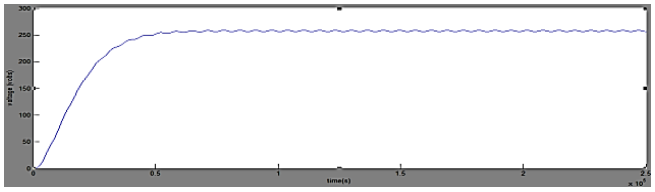

Figure 20: Output voltage for Boost mode of topology 4

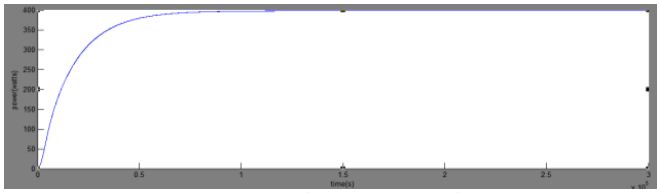

Figure 21: Input power for Boost mode of topology 4

From the above waveforms, for a given the output voltage obtained as 240 V, input voltage of 24 V which is shown in figure 20. The input power is 566 W in figure 21 due to the large current drawn at the input side for a given output power of 500 W.

In topology 3 the input pulse to switch 1 which are being exact during Boost with a duty cycle of 0.72 is given in Figure 14 and its equivalent input and output waveforms are listed below in Figures 15-17.

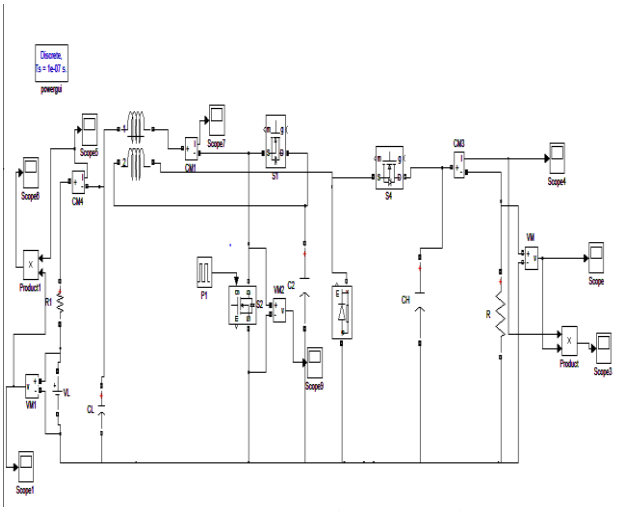

Figure 14: Simulation model of Boost mode for topology 3

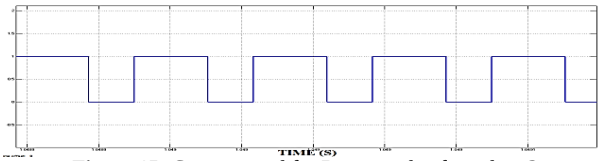

Figure 15: Gating signal for Boost mode of topology3

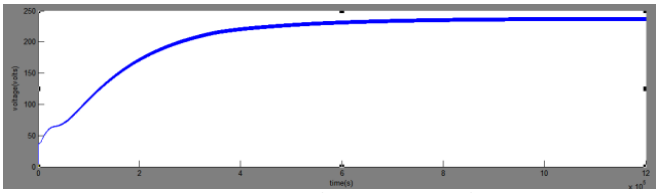

Figure 16: Output voltage for Boost mode of topology3

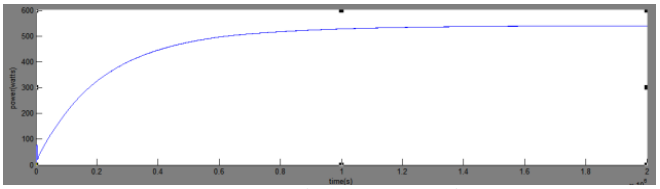

Figure 17: Input power for Boost mode of topology 3

From the above waveforms, for a given the output voltage obtained as 250 V, input voltage of 24 V which is shown in figure 16. The input power is 542 W in figure 17 due to the large inrush of current at the input side.

4.5. Efficiency Calculation of All the Topologies.

The efficiency can be designed either by using the Simulink equivalent model or analytical equations, since the parameters of MOSFET from its datasheet.

4.5.1 Measured Efficiency:

From Simulink equivalent model, input and output powers are stately and the efficiency is designed using equation 14.

$$\eta = \left[\left(\frac{\text{output power}}{\text{input power}}\right)\right] \times 100 \qquad (14)$$

The table 2 offers the comparison of all selected topologies in Boost mode operation. The efficiency, number of switches used, duty cycle, voltage gain are taken into consideration. For 24V / 260 V conversion, the calculated efficiency of topology 4 is 92% which is higher than the other topologies.

Table 2: Comparison of Boost mode

Features	I	II	III	IV
No of switches	2	4	3	3
Voltage gain	$\frac{V_H}{V_L} = \frac{1}{(1-D)}$	$\frac{V_H}{V_L} = \frac{1}{(1-D)^2}$	$\frac{V_H}{V_L} = \frac{2+nD}{1-D}$	$\frac{V_H}{V_L} = \frac{n}{(1-D)}$
Duty cycle	0.60	0.69	0.58	0.72
Efficiency of converter	91%	90%	88%	92%

4.5.2. Theoretic Efficiency:

Also, the efficiency for topology 4 is calculated using analytical equations. Using the data sheet parameters the power loss of MOSFET is calculated. The values which are taken from the data sheet are tr= 30ns, tf= 100ns, Rds(on)= 0.045Ω,

fsw= 30KHZ.

Total power loss (Ptot) = switching Power loss (Psw) +conduction loss (Pcond) (15)

Switching power loss of MOSFET,

$$P_{SW} = \frac{1}{2} V_{DS} \times I_D (t_r + t_f) \times f_{sw} \quad (16)$$

P_{SW} = 4.77W

Conducting power loss of MOSFET,

$$P_{cond} = (I_D)^2 \times R_{ds(on)} \quad (17)$$

P_{cond} = 16.9 W

Total power loss of MOSFET = P_{SW} + P_{cond}

Diode loss, PCD = VD ID × δ

= 0.8 W

Total power loss = P_{SM} + P_{CM} + PCD

Efficiency,

$$\eta = \left[\left(\frac{\text{input power} - \text{total power loss}}{\text{input power}}\right)\right] \times 100 \quad (18)$$

$\eta = 95\%$

Thus, efficiency using analytical equations considering power loss in MOSFET switches and other losses in diode and inductor is found to be 95%

5. Conclusion

Different topologies of Non-Isolated Bidirectional DC-DC Converter are selected based on their comparison in act and appropriateness for UPS application. The circuit operating mode principle of both step up and step down adaptation are clarified in detail. The high voltage side is connected with 260V and low voltage side is connected to 24V source for four topologies. The simulation is finished in Matlab environment. The operative topology for the above identified application is designated based on efficiency, voltage gain, the number of switches used. The efficiency of the topology three is 92% which is slightly higher than the others.

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