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Research paper

Microprocessor Based Firing Circuit for Static Slip Energy Recovery Controlled Slip Ring Induction Motor Drive

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Abstract

Microprocessor based firing control scheme of static slip energy recovery (SER) controlled slip ring induction motor drive is described. In the scheme the microprocessor generates firing pulses and also decides the pair of thyristors of the controlled converter to be gated. It uses less number of hardware components. The oscillograms at different points of the firing circuit and at the output of the controlled converter are presented. These oscillograms resemble with the theoretical wave forms.

1. Introduction

The slip ring induction motor is being used in industrial applications, such as, crane, hoist, pump, and fan [1]. The frequently used control technique is the static Kramer/Scherbius system in which a diode bridge rectifier connected with the rotor of the slip ring induction motor returns slip energy through a line commutated inverter to the ac supply mains [2]. This configuration was first proposed by A. Lavi and R. J. Polge [3]. By regulating the rotor voltage through variation of firing angle of line commutated inverter [4], the speed control is achieved. When the firing angle is decreased, smaller dc voltage of the inverter permits the flow of higher rotor current, resulting higher generation of torque, thereby, higher speed of drive. On the other hand, if the firing angle is increased, higher dc voltage of the inverter prohibits the flow of rotor current, resulting lower torque and lower speed. In recent years, the microprocessor technique has been applied to control the speed of ac and dc drives for obtaining high performance of the drive due to their fast, accurate, versatile, and diagnostic characteristics instead of traditional control scheme [5]. The applications of the microprocessor for the speed control of the drives are shown in papers [6-10].

The drive under investigation shown in fig.1 consists of a slip ring 3-phase induction motor, a 3- phase uncontrolled converter, a smoothing inductor, a 3- phase controlled converter and a 3- phase step up transformer.

In the present paper, Intel-8085 microprocessor is employed to control the firing angle of the controlled converter. It generates the firing pulses of 120^0 duration and also selects the pair of thyristors to be gated in response to three phase zero crossing signals and digitized signals in phase with line voltage applied at the thyristors.

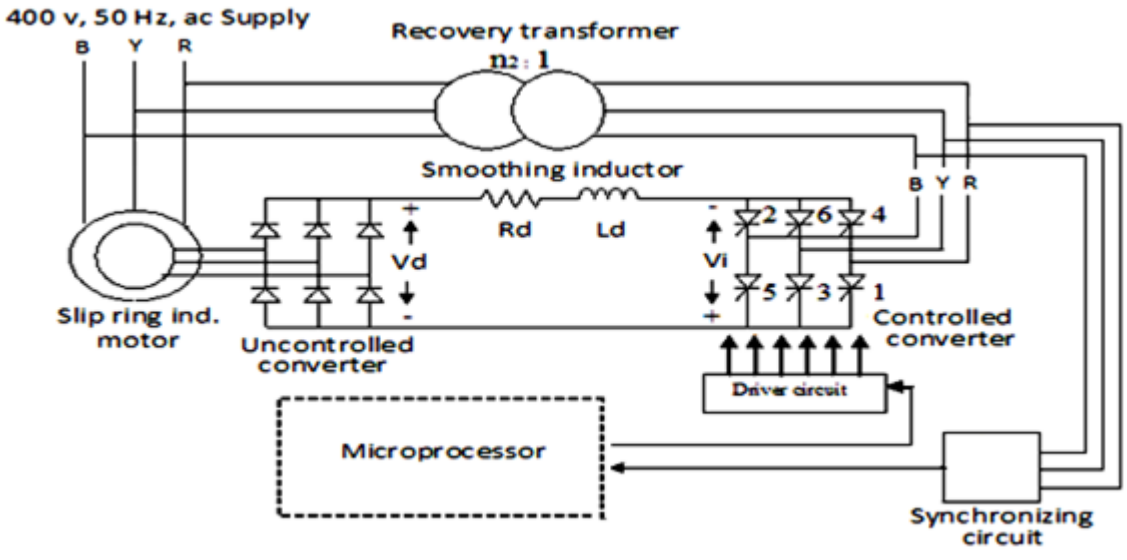

Fig. 1: Schematic diagram of an open loop microprocessor based static SER controlled slip ring induction motor drive

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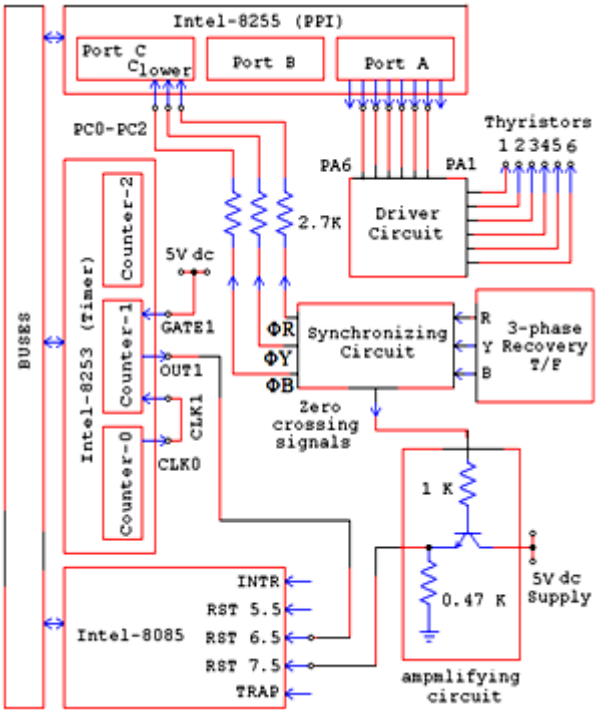

Fig. 2: Block diagram of a microprocessor based firing control scheme

2. Description of Firing Control Scheme

The block diagram of a microprocessor based firing control scheme is shown in fig.2. The three phase zero crossing signals provided by synchronizing circuit after amplification are applied to the microprocessor through RST 7.5 to interrupt the microprocessor at every 60^0 interval of the line frequency. The synchronizing circuit also generates digitized signals ΦR, ΦY and ΦB. These signals are applied to the microprocessor through pins PC0, PC1 and PC2 of port C_{lower} to inform microprocessor that which one pair of thyristor of the controlled converter is forward biased. In response to these two signals, the microprocessor generates firing pulses at the assigned value of the firing angle. The firing angle is measured using Intel-8253, a timer. The firing pulses are provided at pins PA1 to PA6 of port A of Intel-8255, a programmable peripheral interface. For proper firing of thyristors of the control converter, these firing pulses are amplified and shaped properly using driver circuits. The description of three main sections of the block diagram is as follows:

1. Synchronizing circuit:
The synchronizing circuit is shown in fig. 3. The secondary voltage of three phase delta/star step- down transformer lags the primary voltage by 30^0. The comparator connected with the secondary winding converts sine wave into alternating square wave. The zener diode passes positive half of square wave and blocks its negative half and provides digitized signals ΦR, ΦY and ΦB which are in phase with line voltage V_{ry}, V_{yb} and V_{br}. After inverting these, inverted digitized signals $\overline{\Phi R}$, $\overline{\Phi Y}$ and $\overline{\Phi B}$ are obtained. All these digitized signals are differentiated using RC circuits and the outputs of the differentiators are fed to dual monostable multivibrators which generate pulses of 0.088 millisecond width required by the microprocessor to be interrupted through RST 7.5. Three phase zero crossing signals are obtained after performing NAND-gate operation of signals $\overline{Q1}$, $\overline{Q2}$ & $\overline{Q3}$ and $\overline{Q4}$, $\overline{Q5}$ & $\overline{Q6}$ and then OR-gate operation.

2. Generation of firing pulses:
The counter-1 of Intel-8253 is used to provide the delay corresponding to the firing angle of the controlled converter from the instant of zero crossing signal. The time daily is counted using the clock signal of 1.536 MHz which is available at CLK0 pin of the counter-0. The port C_{lower} is assigned as input port for inputting digitized signals ΦR, ΦY and ΦB, whereas, port A is assigned as output port for outputting firing pulses for the thyristors of the controlled converter. For inverter operation of the controlled converter the firing angle should be greater than 90^0. Two thyristors one from upper half and other from lower half conduct at a time. Each thyristor conducts for 120^0 interval in every cycle. After each 60^0 interval, one thyristor in sequence is fired and one thyristor turns off. To meet these requirements six firing pulses at each 60^0 interval are generated at predetermined firing angle. Each firing pulse is made of 120^0 duration to ensure reliable operation of thyristors in the presence of source inductance..The system software consisting of one main program and two numbers of subroutine programs one for RST 6.5 and another for RST 7.5 is developed for the control of firing angle.

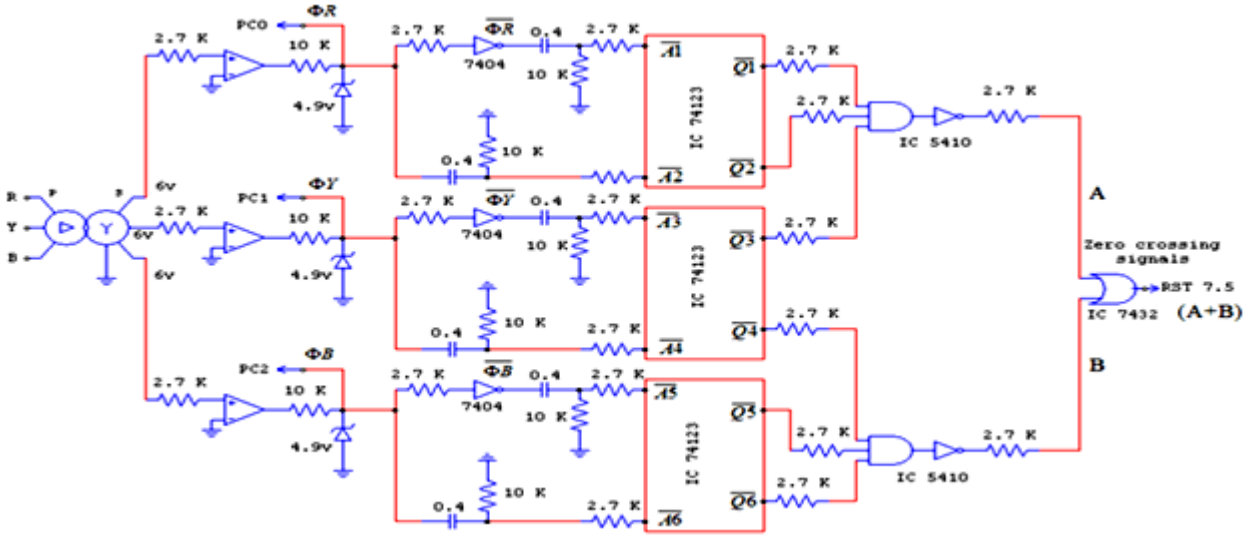

Fig. 3: Synchronizing Circuit of Three Phase Controlled Converter

(a) Main program:

The figure fig.4.shows the flow chart of the main program. Firstly, the main program initializes ports of intel-8255, counters of 8253 and stack pointer. For the initialization of Intel-8255 and 8253, their control words made as per the requirements and assignments, are loaded in the accumulator. Secondly, the control of interrupts and facilitation of operation of RST 6.5 and RST 7.5 subroutines are also taken care by the main program. The command word of interrupts unmasks RST 7.5 and masks RST 6.5 and RST 5.5. After initialization the microprocessor waits for zero crossing signals through RST 7.5. On interruption, service subroutine RST 7.5 starts execution and waits for interruption through RST 6.5 which is unmasked at the end of RST 7.5 service subroutine. RST 6.5 gets interrupt signal through OUT1 at the terminal count. After interruption the service subroutine of RST 6.5 starts execution and after performing its function returns to the main program to initialize Intel-8253 once again.

(b) RST 7.5 service subroutine:

The flowchart of RST 7.5 service subroutine is given in fig.5. Initially the firing angle 'α' is read and pointer 'P' is set to zero. First function of this subroutine is to calculate the reduced control angle and corresponding LSB address of the count value which is double of the reduced control angle. The reduced control angle is the angle which indicates how much firing angle is higher than 60^0 or 120^0. The pointer 'P' is modified by adding either 06 H or 0C H depending on whether the firing angle is greater than 60^0 or 120^0.

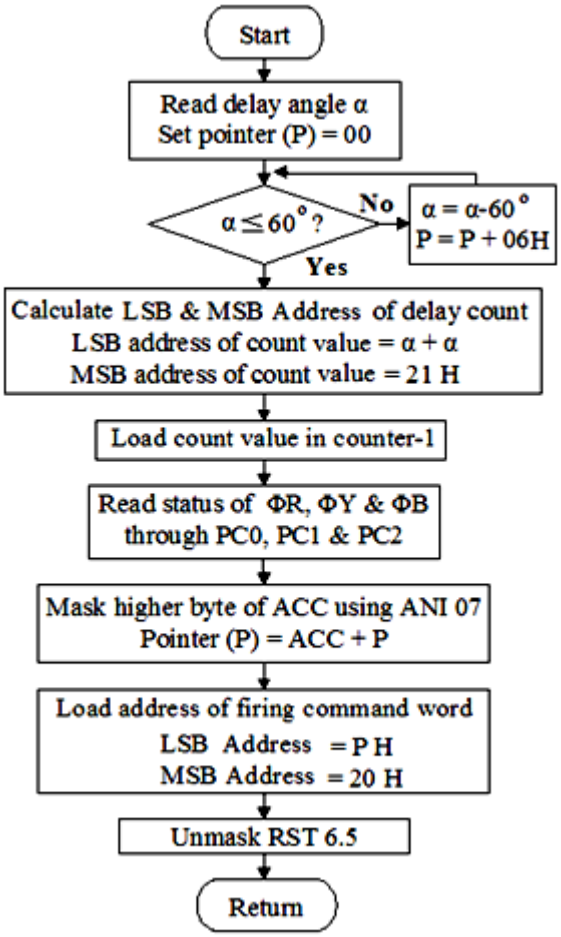

Fig. 4: Flow chart of main program

The count value is loaded in counter-1 from the look up table whose address has been calculated. This subroutine also calculates the address of firing command word which decides the pair of thyristors to be fired. The status of ΦR, ΦY and ΦB are stored in accumulator which in turn is ANDed with 07H. The Pointer 'P' is now modified by adding its content with the content of accumulator. This new value of 'P' is the LSB address of the firing command word. At the end of the subroutine RST 6.5 is unmasked. The firing command words which depend upon the range of the firing angle and status of ΦR, ΦY and ΦB are given in Appendix.

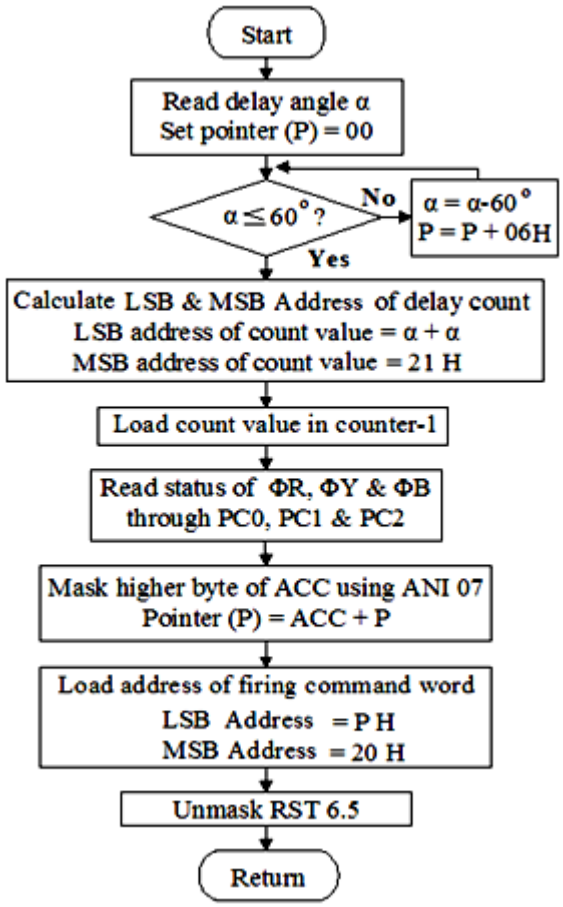

Fig. 5: Flow chart of service subroutine RST 7.5

(c) RST 6.5 service subroutine:

For each zero crossing signals, This subroutine provides firing pulses to the selected pair of thyristors and low level signals to the rest of the thyristors of the converter through pins PA1-PA6. The firing command word selected using RST 7.5 interrupt service subroutine is loaded in the accumulator and then outputted to the output port A. All six pins PA1–PA6 of port A are set or reset as per the bit pattern of the firing command word.

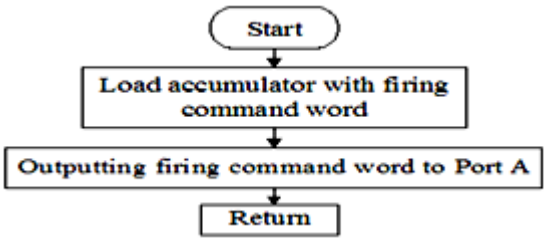

Fig. 6: Flow chart of service subroutine RST 6.5

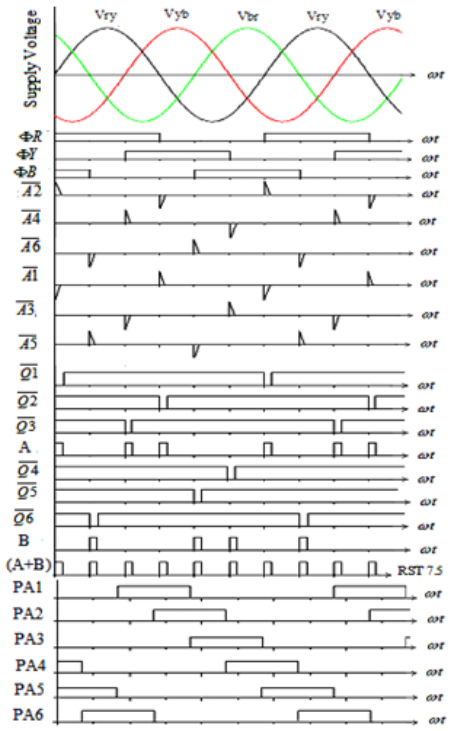

Fig. 7: Theoretical wave form at different points of synchronizing circuit and output port A

This condition of pins continues for 60^0 duration till issuing of next firing command word. The sequence of firing is such that a particular pin of port A is set for two consecutive periods i.e. 120^0 duration. Thus, each thyristor of the controlled converter receives firing pulse of 120^0 duration. The flow chart of this subroutine is shown in fig. 6.

The theoretical wave forms at different points of the synchronizing circuit and pins of output port A are shown in fig. 7.

3. Pulse shaping and driver circuit:

The pulse shaping and driver circuit is shown in fig. 8 for channel-PA1. This circuit does the power amplification and digitization of firing pulse. The firing pulses generated by the microprocessor at PA1-PA6 are continuous of 120^0 pulse duration of the line frequency and responsible for high gate power losses. To minimize the gate power losses, the continuous signal is ANDed with 13.85 KHz

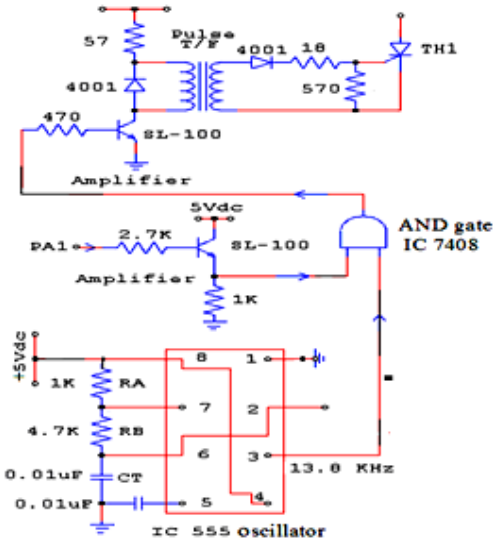

Fig. 8: Pulse shaping and driver circuit for thyristor-1 available at PA1 of port A

high frequency signal produced by IC-555 working as astable multivibrator. The firing signals generated by the microprocessor are quite weak hence, amplified before AND operation using SL-100 medium power transistor. The output of AND gate is a train of digitized pulses which protects pulse transformer against saturation. These digitized pulses are further amplified making suitable for firing of thyristors.

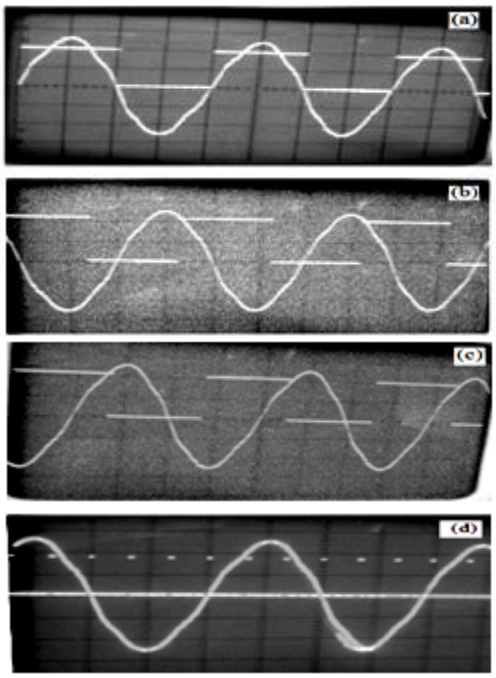

Fig. 9: Oscillograms of digitized signals ΦR, ΦY & ΦB with reference to line voltage Vry (a) ΦR (b) ΦY (c) ΦB (d) Zero crossing signals (2 V/div. and 5 ms /div.)

3. Experimental Results and Discussion

The proposed firing circuit is developed. The experimental setup runs smoothly using the control methodology discussed. All the oscillograms are shown with reference to the line voltage V_{ry}. The oscillograms of digitized signals ΦR, ΦY and ΦB which are in phase with line voltage V_{ry}, V_{yb} and V_{br} are shown in fig. 9 (a), (b) and (c) respectively. The oscillogram of zero crossing signals is shown in figure 9(d). The oscillograms shown in fig. 10 (a) – (f) show the firing pulses generated by the driver circuit at the firing angle of 100^0. The oscillogram of dc output voltage of the controlled converter is shown in fig. 10 (g). It is observed that the experimental wave forms shown at different points of the firing circuit resemble with the corresponding theoretical wave forms.

4. Conclusions

In the developed firing circuit the microprocessor generates the firing pulse of 120^0 duration and also decides the pair of thyristors of the controlled converter to be gated. The algorithms of the main program and service subroutine programs of RST 7.5 and RST 6.5 are developed, tested individually and also in combined form. The developed firing circuit has following salient features:

(i) Any change in the firing angle is effectively implemented in the next 60^0 duration of the line frequency.

(ii) As the microprocessor is interrupted at every zero crossing signal, hence, the drift which may occur during down counting is reset in every 60^0 duration.

(iii) The firing circuit is simple and can be implemented for line commutated converter for wide range of the firing angle.

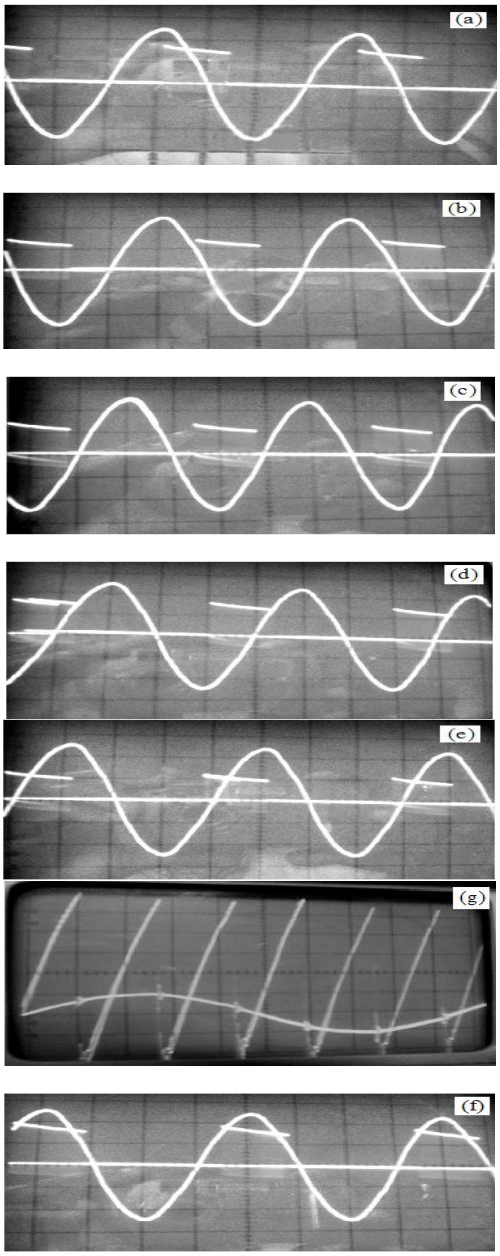

Fig. 10: Oscillograms of firing pulses generated by driver circuit for firing angle $\alpha = 100^0$ and dc output voltage of the controlled converter with reference to line voltage Vry (a) Thy1 (b) Thy2 (c) Thy3 (d) Thy4 (e) Thy5 (f) Thy6 (g) dc voltage (inverted) (5 ms /div.)

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Appendix

For Delay Angle $0 \le \alpha \le 60^0$

Line status command			Devices to whom	Firing
ΦB	**ΦY**	**ΦR**	**pulses be given**	**word**
0	0	1	1, 2	06 H
0	1	0	3, 4	18 H
0	1	1	3, 2	0C H
1	0	0	5, 6	60 H
1	0	1	1, 6	42 H
1	1	0	5, 4	30 H

For Delay Angle $60^0 \le \alpha \le 120^0$

0	0	1	1, 6	42 H
0	1	0	3, 2	0C H
0	1	1	1, 2	06 H
1	0	0	5, 4	30 H
1	0	1	5, 6	60 H
1	1	0	3, 4	18 H

For Delay Angle $120^0 \le \alpha \le 180^0$

0	0	1	5, 6	60 H
0	1	0	1, 2	06 H
0	1	1	1, 6	42 H
1	0	0	3, 4	18 H
1	0	1	5, 4	30 H
1	1	0	3, 2	0C H