*International Journal of Engineering & Technology*, 7 (3.1) (2018) 183-185

International Journal of Engineering & Technology

*Website: www.sciencepubco.com/index.php/IJET*

***Research paper***



# Low Power and Low Complexity Flip-Flop Design using MIFGMOS

**U Ragavendran & M Ramachandran**

*MPSTME, NMIMS (Deemed to be University), India 425 405.*
**Corresponding author E-mail druragavendran@gmail.com*

**Abstract**

Sequential logic is essential in many applications as data processing for speech recognition in cochlear implants. In this paper, a family of latches based on floating-gate MOS (FGMOS) transistors is presented. This family takes advantage on the fact that FGMOS logics process data using mostly passive devices, achieving small area and low-power, requirements of modern electronics. Post-layout SPICE simulations from an ON-Semiconductors 0.5 µm CMOS process technology shows improvements over conventional CMOS logic families, making FGMOS latches ideal for low-power applications.

*Keyword: MIFGMOS, Flip-flop, Low power design, low-power integrated circuits; FGMOS Transistors*

## 1. Introduction

Modern electronics present important challenges to design low-power, highly integrated data processing. To face these demands, digital design has developed many topologies to reduce power-delay product. Among these, floating-gate MOS (FGMOS) transistors have demonstrated to achieve power reductions while still maintaining speed in many high performance applications (Aunet, Berg, Tjore, Næss and Sæther 2001).This is possible due to the fact that FGMOS transistors process data within the capacitive network coupled to their gate (Shibata and Ohmi 1992). As data processing is carried using mostly passive devices at gate level, no switching nodes or leaky devices are involved achieving virtually no power dissipation.

## 2. Floating-Gate Logic

An architecture that takes advantage of the FGMOS transistors is Positive Feedback Floating-Gate Logic (PFFGL). This logic uses a positive-feedback loop to improve gain in order to reduce errors due to process variability or noise. This way, using smart layout techniques, noise is diminished by the common-mode rejection characteristics of the logic. As the noise-sensibility of the FGMOS transistor increases with small input capacitors, eliminating this constraint will allow reductions of input capacitances as well as area. Furthermore, as all data processing is carried by the capacitive network of the input FGMOS transistors, PFFGL achieve minimal transistor count resulting in low- voltage; reduced operational voltage and minimal switching transistors are the most straight-forward way to reduce power. In order to memorize data, PFFGL sequential gates take advantage of the p-MOS semiconductor. It consists of a -channel MOS transistor with a floating gate (first polysilicon layer) over the channel and in some cases extending over to the field oxide area. An array of control gates (multiple input gates) are formed by the second polysilicon layer over the floating-gate. The capacitive coupling between the multiple input gates and floating-gate and the channel.

## 3. PFFGL Sequential Gates

Latch used as comparator. While the input FGMOS transistors process data, the p-MOS semi-latch ensures a valid output. If eventually the FGMOS transistors are turned off by inducing the appropriate offset to their floating gates, the last output data is stored by the p-MOS semi-latch until the next computation be carried. To achieve this process, a control gate is added to the FGMOS transistors. If this control gate is connected to ground, the weighted sum of input voltages will be too low to turn any of the FGMOS transistors on. According to the above, the D latch shown in Fig. 1 is proposed. While normal operation, SET and RST inputs are normally set to 0. As these inputs have twice the weight of the rest of the inputs, the FGMOS transistors threshold voltage can only be reached when the clock input (Ck) is in a high state. If Ck and SET/RST inputs have a low state, no matter the state of the input D, both transistors will be off and the data at the outputs will be retained. If eventually Ck flips to a high state, the state of D will be large enough to trigger the latch. In the case that SET or RST has a high state, a change at the output will occur immediately; as these inputs has twice the weight of the other inputs will override the state of D or Ck. To achieve the set or reset process, Ck needs to be low to avoid the possibility that both input FGMOS transistor be turned on simultaneously resulting in an invalid output.

Due to their small transistor count, the proposed latch solve problems as body effect; implementations as CMOS or pass-transistor latches uses long chains of series transistors, resulting in a degradation of the output data. To restore output noise, buffers can be used. Although this solution can effectively restore output levels, it will increase both power and delay of the gate.

**Copyright © 2018 Authors. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.**

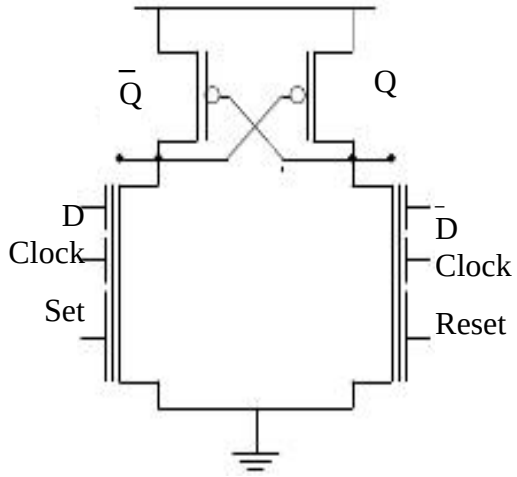



**Fig.1**: Latch D implementation using floating-gate transistors

## 4. Implementation

In this section, post-layout simulations are performed to compare the proposed PFFGL sequential gates against conventional logic families. The gate selected for this comparison is a D flip-flop. The floating-gate flip-flop proposed for evaluation is shown in Fig. 2. It consists in two D latches in series. Whenever the clock input Ck has a high state, the first D latch will pass the input data to its output. If Ck flips to zero, the input data will be stored at the first latch. Simultaneously, the second D latch will pass the held data to the output Q. When Ck flips back to high, the first gate will admit a new input data while the output latch will be holding the last output state.

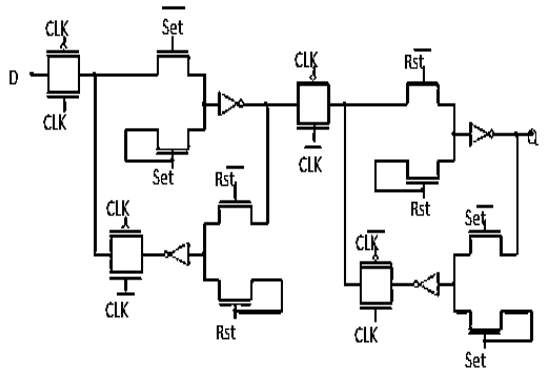



**Fig.2.**Proposed circuit for the implementation of a D Flip-Flop

Complementary pass-transistor logic (CPL) and standard CMOS versions of the D Flip-Flop (Waste and Eshraghian 2001) are shown in Fig. 3 and Fig. 4. The latching operation is realized by two cross coupled inverters. The feedback of the inverters will make possible the data holding. To modify the stored data, pass-gate transistors at the input of each of the two D latches are used. When Ck have a high state, the first pass- gate will allow data acquisition by the first latch while isolate the second. If Ck changes to low, the first latch will hold the last input data, passing through the second latch to the output Q. When a Set/Rst procedure is carried out, the feedback loop between the latching inverters is opened. Once the feedback loop is open, the Set/Rst data is applied. When this procedure is finished, the feedback loop is restored.

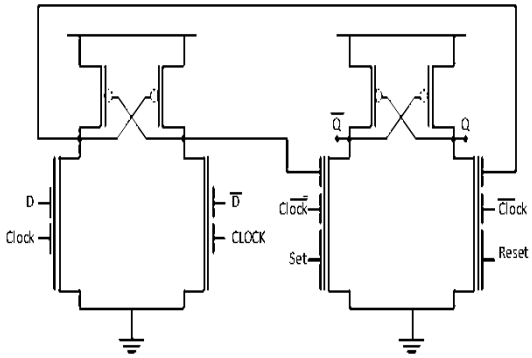



**Fig.3:** Complementary pass-transistor D Flip Flop.

The CMOS D flip-flop is shown in Fig 4. In this scheme, cross coupled transistors are used for data memorization. As well as the previous circuits, it consists in two D latches in series. This implementation requires five transistors in series, making the flip-flop to operate at very low frequency. Besides, the power requirement rises, making the implementation not suitable for low voltage. The voltage requirement, the transistor tree height and the large count of transistors and switching nodes, makes this implementation improper for energy efficient battery driven applications

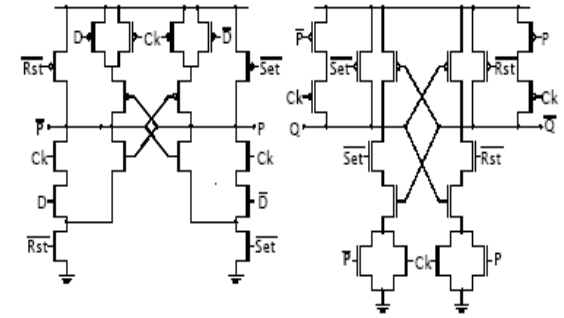



**Fig.4:** CMOS D Flip Flop.

Simulations were performed using SPICE with an ON-Semiconductors 0.5 µm CMOS technology. To achieve realistic results, the technique discussed in (Rodriguez- Villegas, Huertas, Avedillo, Quintana and Rueda 2001) is employed for simulation of floating-gate transistors. For each of the implementations, a load similar to a flip-flop of the same family was used at the output. Fig. 5 shows the simulation results for all of the flip-flop implementations. Even when FGMOS and CMOS were able to work at lower voltage, the simulations were performed at 3.3 volts. The long transistor chain of CPL implementation was not able to work properly below this voltage

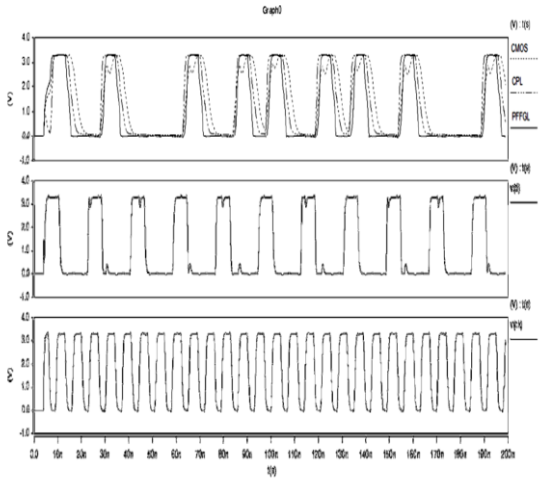



**Fig.5:** Spice simulation results for the three D flip-flop implementations

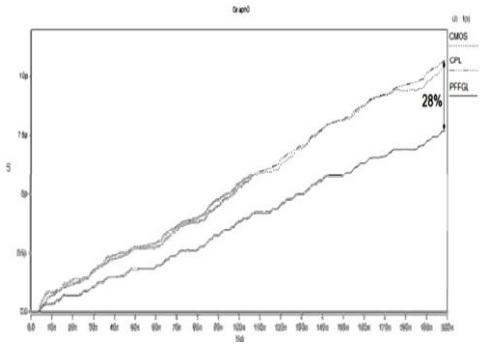



**Fig.6:** PFFGL D Flip Flop showed better power performance.

**Table.1:** Simulation Results

| Methodology | $t_d$(ns) | $t_r$ (ns) | $t_f$(ns) | Input Cap (fF) | Transistor Count |
|---|---|---|---|---|---|
| **CPL** | 2.01 | 0.90 | 2.49 | 40.05 | 26 |
| **CMOS** | 4.00 | 2.07 | 3.03 | 89 | 32 |
| **PFFGL** | 2.31 | 0.97 | 1.67 | <18.9 | 8 |

By using a high gain amplifier as comparator, PFFGL is able to use the smallest transistors allowed by the technology. This condition let using small input capacitances for the FGMOS transistors, achieving the smallest input capacitance of the comparison. The resulting input capacitance of the PFFGL flip-flop is less than 19 fF. Low voltage and small capacitance internal nodes allow PFFGL to show significant improvements in power characteristics. Fig. 6 is show an energy comparison between all the flip-flop implementations. CPL showed the worst case, consuming an amount of energy equal to 10.67 pJ along the test cycle. CMOS showed similar power characteristics, wasting 10.39 pJ along the cycle. The best power performance was reached by the PFFGL implementation, with a reduction of 28% in energy consumption resulting in an energy waste of 7.69 pJ. It was expected CMOS to have the worst performance in the comparison due to its large count of transistors and the long transistor trees. Even though, CPL resulted to be the worst case in voltage and power consumption. Table 1 shows the comparison of the three flip-flops. Can be seen that the floating gate flip-flop have the smaller transistor count in the comparison, requiring an area of 51 X 28 µm2. Besides the area reduction due to a small transistor count, there is an improvement due to a simplification of routing. Smaller devices and simplified routing leads to improvements in circuit integration.

From Table 1 can be seen that CMOS shows the worst propagation delay in the comparison. The latency of the CMOS flip-flop is significantly bigger than its counterparts. Moreover, CMOS achieved the worst rise/fall times, reducing its frequency of operation. The best speed characteristics were achieved by the PFFGL flip-flop, being able to work at 600 MHz while CMOS frequency of operation is about only 330 MHz and CPL is able to operate at a frequency of 400 MHz. Again, the small capacitance internal nodes led to performance improvements

## 4. Conclusion

A new sequential logic family featuring floating gate transistors was introduced. The principal features of this design style are low-power and high scale of integration. The logic style in which this family is based allows robustness to the typical problems of the floating gate logics while still maintaining its advantages. FGMOS transistors as inputs allow data processing in a very compact circuit. The proposed gates require less area than similar implementations in the comparison. Positive feedback realizes a fast establishment of the output state. The frequency of operation of the floating gate sequential logic is higher than conventional sequential gates. The sequential logic proposed in this paper will allow the construction of low power circuits. Sequential logic is essential in digital data processing. Thus, high performance low-power sequential logic is vital in the construction of circuitry for biomedical applications. FGMOS logic gate has been successfully used to construct processing and arithmetic blocks as adders and multipliers (Cisneros-Sinencio, Díaz- Sánchez and Ramirez-Angulo 2004). These processing blocks will fulfill the energy efficient, low-voltage, high integration requirements of applications like cochlear implants or machine-brain interfaces while still maintaining speed.

## References

[1] S. Aunet, Y. Berg, O. Tjore, Ø. Næss, T. Sæther, “Four-MOSFET Floating-Gate UV- Programmable Elements for Multifunction Binary Logic” Proceedings of the 5th World Multi conference on Systemics, Cybernetics and Informatics, 2001.

[2] U. Ragavendran, M. Ramachandran, Low Power Spike Analysis of Neuron Circuit with Floating Gate Transistors (FGMOS), International Journal of Pure and Applied Mathematics 119(12), 2018

[3] T. Shibata & T. Ohmi, “A Functional MOS Transistor Featuring Gate Level Weighted Sum and Threshold Operations”, IEEE Trans. Electron Devices, vol. 39, pp. 1444-1455, 1992.

[4] Ragavendran, U., M. Ramkumarraja, and M. Ramachandran. "Low power VLSI architecture for LTEx binary to gray converters." In 2017 3rd International Conference on Applied and Theoretical Computing and Communication Technology (iCATccT), pp. 107-109. IEEE, 2017.

[5] N. H. Waste, K. Eshraghian, “Principles of CMOS VLSI Design,” 2nd Ed., Addisson Wesley, Reading, Mass., pp. 217-219, 1998.

[6] E. Rodriguez-Villegas, G. Huertas, M. J. Avedillo, J. M. Quintana and A. Rueda, “A practical Floating-Gate Muller-C Element Using vMOS Threshold Gates”, IEEE Trans. Circuits and Systems II, vol. 48, pp. 102-106, 2001.

[7] Duraisamy, K, Ragavendran, U ‘Low Power Analog Multiplier Using MIFGMOS’, Journal of Computer Science (JCS), vol. 9, no. 4, pp. 514-520, 2013.

[8] L. F. Cisneros-Sinencio, A. Díaz-Sánchez, J. Ramirez-Angulo, "A Novel Serial Multiplier Using Floating Gate Transistors", Proceedings of the IEEE International Symposium on Circuit and Systems ISCAS´2004, Vancouver, CA.

[9] Ragavendran, U., Viral Mehta, Vishal Fegade, and M. Ramachandran. "Dynamic Analysis of Single Fold Symmetric Composite Laminates." International Journal of Civil Engineering and Technology 8, no. 11 (2017): 536-545.

[10] Medina-Vazquez, Agustín Santiago, Marco A. Gurrola-Navarro, C. A. Bonilla-Barragan, and JM Villegas Gonzalez. "A technique to improve the transconductance in amplifiers." In Electrical Engineering, Computing Science and Automatic Control (CCE), 2016 13th International Conference on, pp. 1-3. IEEE, 2016.