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Research paper

Design, Implementation and Analysis of 8T SRAM Cell in Memory Array

B. Kaleeswari[1]*, S. Kaja Mohideen[2]

[1,2]Department of ECE, B.S. Abdur Rahman University, Chennai, Tamilnadu-600048, India.
**Corresponding author E-mail: kaleeswariece@gmail.com*

Abstract

In modern VLSI designs, static random access memory plays a vital role because of its high performance and low power consumption qualities. As technology is scale down, the importance of the power analysis and leakage current of memory design is increasing. This paper describes about the 1 KB size memory design using SRAM. The proposed design of 8T SRAM single cell in implemented in array structure of size 32x32.The design structure reduces the power by 75% by reducing the leakage current. The proposed 8T SRAM cell is implemented and analyzed in 90nm technology using Digital schematic and Micro wind software.

Keywords: *WL, BL, BLB and SRAM.*

1. Introduction

In today's world, the information technology is depending on semiconductor based electronics. However the first transistor was invented in 1948, there will be a tremendous growth in semiconductor industry. There are two major fields which are benefited by the growth of semiconductor industry, are semiconductor based memories and microprocessors. The performance has improved by this technological advancement parallel the device density also increases.

The power dissipation in integrated circuit(IC) depending on different operating modes of the circuit .first one is during active mode of operation the dynamic power is dominating. Second one is two primary leakage sources the active and standby leakage component.

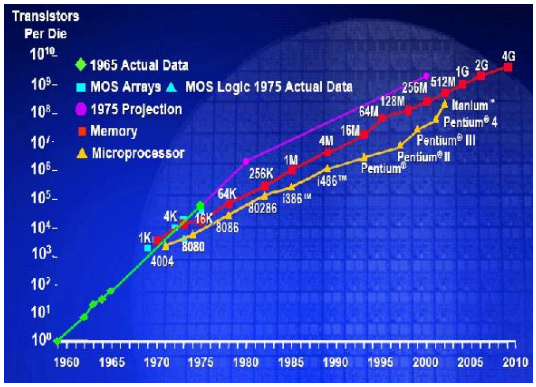


Fig. 1: Technology Scale Down

Section 1, describes about the introduction to VLSI circuits. Section 2, explains about the basic operation of SRAM. Section 3 briefs about the effects of power dissipation. Section 4, discusses about the proposed 8T SRAM circuit. Section 5, describes about the memory array architecture. Section 6 discusses about the implementation of 8T circuit in array structure. Section 7, discusses about the simulation and result .finally section 8 concludes the work.

2. Basics of SRAM

In static RAM circuit the data can be stored perpetually until the power supply is ON.In static RAM array; single storage cell always consists of simple latch circuit, in which two stable operating points are present. Figure 2 shows the single SRAM cell.

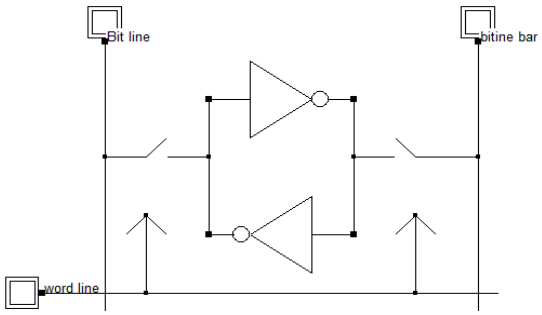


Fig. 2: SRAM cell

Based on conserved state of two inverter latch circuit, the data can be interpreted as logic '1' or logic '0'depending upon the data being held on the memory. Data contained in memory can be accessed through the bit line and bit line bar. In order to write a data in a memory a switch is used called word line.

2.1. CMOS SRAM Cell Design

The Single SRAM cell using CMOS transistor is shown in Fig 3. To design the low power CMOS inverter, use cross coupled CMOS inverter is used. The static power dissipation is very small in cross coupled inverter circuit. However there is the considerable amount of leakage current in the circuit. A simple CMOS inverter is connected back to back and two access transistors are present

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in a single memory cell. Whenever the word line is activated the two access transistors are turned ON [6].

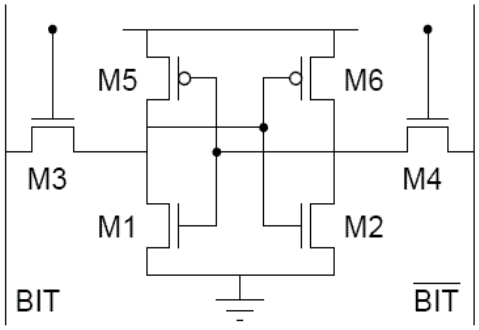


Fig. 3: SRAM Cell using CMOS

2.2. SRAM Read Operation

Initially a logic 0 is stored in the cell, the transistor M1 and M6 operates in linear region, and M2 and M5 in cutoff region .This results in the internal node V_1=0v and V_2=V_{dd}, before two access transistor get turn ON .This is shown in fig 4.Using row column circuitry, the two access transistors M_3 and M_4 are turned ON.

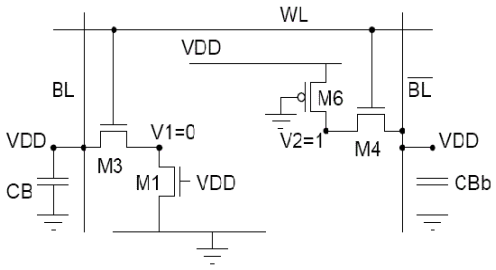


Fig. 4: Read Operation

The voltage at bit line bar will not change since there is no current flow through M_4 .on the other side the M_1 and M_3 will conduct a nonzero current .The voltage level at the capacitance of bit line will drop slightly. The voltage at V_1 will increase from '0 'v, however the V_1 may exceeds the threshold voltage of M_2during this process flipping of states will occur .Therefore V_1 must not exceeds the threshold voltage of M_2so the transistor M_2 remain turn off during read operation.

$$V_{1max} \leq V_{T,2} \quad (1)$$

The transistor M3 is in saturation whereas M1 is linear, equating the current equations we get

$$\frac{\beta_{N3}}{2}(V_{DD}-V_1-V_{TN})^2=\frac{\beta_{N1}}{2}(2(V_{DD}-V_{TN})V_1-V_1^2) \quad (2)$$

Substitute Eqn1 in Eqn 2

$$\frac{\beta_{N3}}{\beta_{N1}}=\frac{(W/L)_3}{(W/L)_1}\leq 2V_{TN}\frac{(V_{DD}-1.5V_{TN})}{(V_{DD}-2V_{TN})^2} \quad (3)$$

2.3. SRAM Write Operation

Assume that logic 0 has to written in the cell, consider a logic 1 is stored in the cell .Transistor M2 and M5 are operates in linear region and m1 and M5 are operating in cutoff region .Before the two access transistor turn ON, the node voltage at V_1= V_{dd} and V_2=0.The bitline voltage V_b is forced to 0 by write column circuitry. After the transistor M3 and M4 turns ON according to the equation V_{1max}<=$V_{T,2}$.

The node voltage at V_2 remains below the threshold voltage of M_1 .The voltage at node 2would not be sufficient .In order to store logic 1 force V_1=0 and V_2=V_{dd} this in turn off the transistor M_2 due to reduction in voltage V_1 below the threshold level .When V_1 =V_t, transistor M_3operates in linear region while M_5operates in saturation region

$$\frac{\beta_{P5}}{2}(0-V_{DD}-V_{TP})^2=\frac{\beta_{N3}}{2}(2(V_{DD}-V_{TN})V_1-V_1^2) \quad (4)$$

Rearranging the condition of V_1 in the result we get

$$\frac{\beta_{P5}}{\beta_{N3}}=\frac{\mu_P}{\mu_N}\cdot\frac{(W/L)_5}{(W/L)_3}<\frac{(2(V_{DD}-1.5V_{TN})V_{TN})}{(V_{DD}-V_{TP})} \quad (5)$$

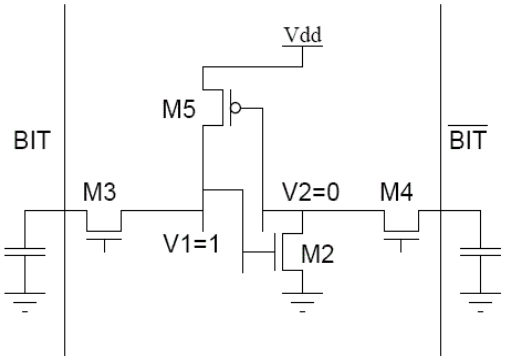


Fig. 5: Write Operation

3. Effects of Power Dissipation

The When power is dissipated, it invariably leads to rise in temperature of the chip. This rise in temperature affects the device both when the device is off as well as when the device is on.

When the device is off, it leads to increase in the number of intrinsic carriers, by the following relation:

$$n_i \propto e^{\frac{-EG}{KT}} \quad (6)$$

From the above equation it is observed that whenever there is increase in temperature the number of intrinsic carriers is also increased. The majority carriers are not affected by temperature change because the majority carriers are contributed by impurity atoms. When temperature increases the concentration of minority carriers get increased this in turn leakage current in the device get increased which in turn further increase in temperature.

3.1. Sources of Leakage Power

No there are four sources of leakage power in CMOS circuit

(i) Reverse biased junction leakage current(I_{REV})
(ii)Gate induced Drain Leakage (I_{GIDL})
(iii)Gate direct tunneling effect(I_G)
(iv)Sub threshold leakage(I_{SUB})

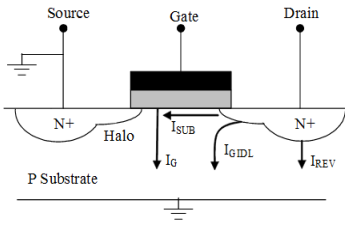


Fig 6: Leakage Current Components

3.2. Sub Threshold Leakage Current

In weak inversion region, the drain source current of transistor is operating. The main reason for occurring the sub threshold condition is diffusion current of minority carriers in the channel. In CMOS inverter the logic '0' input is given to NMOS transistor ,it

turns to off and output voltage is high. However V_{GS}= 0v thereis current flow in the channel of NMOS transistor due to V_{DD}. Because the sub threshold voltage depends on supply voltage, Temperature, device size and process parameter. Over which the threshold voltage plays a vital role.

3.3. Effect of Sub Threshold Leakage Current

The sub threshold leakage current I_{SUB} has a greater contribution for power dissipation than the other leakage current in CMOS technologies.
I_{SUB} is calculated using the formula

$$I_{SUB} = \frac{W}{L}\mu V_{th}^{2} C_{sth} e^{\frac{V_{GS}-V_T+\eta V_{DS}}{nV_{th}}} (1 - e^{\frac{-V_{DS}}{V_{th}}}) \quad (7)$$

Where W and L be the width and length of transistor, μ denotes the mobility of carriers, Vth is threshold voltage η is the drain induced barrier lowering coefficient

$$n = 1 + \frac{C_{sth}}{C_{ox}} \quad (8)$$

Where C_{ox} is gate input capacitance per unit area of MOS gate. When long channel transistor with V_{DS} larger than V_{th} is in off state

$$I_{SUB} = \frac{W}{L}\mu V_{th}^{2} C_{sth} 10^{\frac{-V_T}{S}} \quad (9)$$

Where S denotes the sub threshold swing parameter .It is highly desirable that S should be small as possible because it is going to determine the amount of voltage swing necessary to switch ON and OFF the MOSFET (typical values of S for bulk CMOS devices are 70-110 mV/decade; the theoretical lower bound is 60 mV/decade corresponding to n=1.)Increase in temperature results in larger S value this in turn increase the OFF.
In long channel devices there is a small amount of current flow due to the influence of I_{DS}. In short channel devices the channel lengths get reduced results in overlapping the source and drain depletion region get overlapped. The electrons will flow in greater amount with a small amount of charge in gate cause decrease in threshold voltage and increase in I_{OFF}.

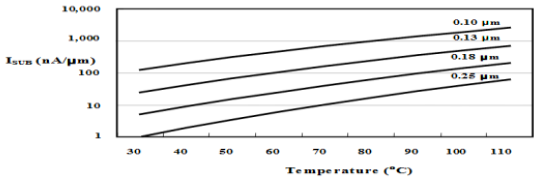


Fig. 7: Sub threshold current is function of Temperature

From the figure it is clearly understand that whenever there is increase in temperature there will be increase in sub threshold leakage current by a factor of 10 and decrease in threshold voltage by 100mV.As a result a device having low threshold voltage due to process variation undergone more leakage current.

4. Proposed 8T SRAM Circuit

By considering all the above factors that cause sub threshold leakage current ,the new circuit was proposed as shown if fig 8. The proposed 8T SRAM circuit consists of single 6T SRAM cell with two PMOS is added with pass transistors.

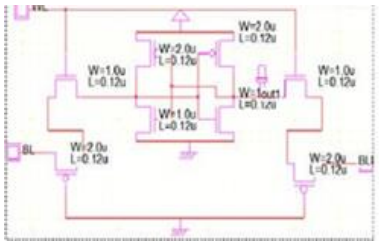


Fig. 8: Proposed 8T SRAM Circuit

In the proposed 8T SRAM circuit the sub threshold leakage current is reduced by two PMOS transistor connected the source terminal of two pass transistors.

4.1. Read Operation

During read operation the voltage at node V_1 (refer to fig 3) will not exceeds the threshold voltage of M2 transistor .But practically V1 voltage will exceeds the threshold voltage of M2 due to sub threshold leakage current caused by shrinking of device geometry. This will results in flipping of states and power dissipation also.

This effect will be avoided by introduce gate delay in the circuit. The gate delay will be introduced by increasing the channel length of two pass transistors .But this will increase the I_{oN} current .By considering all this into account two PMOS transistors are introduced. This two PMOS transistor introduce the delay in pass transistors, in order to maintain the I_{OFF} less than the threshold voltage of M2 transistor.

4.2. Write Operation

During write operation ,in order to store logic 1 force V_1=0 and V_2=V_{dd} (refer to fig 4) this in turn off the transistor M_2 due to reduction in voltage V_1 below the threshold level .When V_1 =V_t, transistor M_3operates in linear region while M_5operates in saturation region. The same condition prevails in read operation as discussed in above paragraph, I_{OFF} current will starts increasing this in turn exceeds the threshold voltage of M2 transistor results in flipping of states. This will be avoided by two PMOS transistor connected to pass transistor introduce delay .by introducing delay the V_2 is kept below the threshold voltage of M2 in order to reduce the power dissipation.

4.3. Analysis

The sub threshold leakage current is defined as

$$I_{SUB} = \frac{W}{L}\mu V_{th}^{2} C_{sth} e^{\frac{V_{GS}-V_T+\eta V_{DS}}{nV_{th}}} (1 - e^{\frac{-V_{DS}}{V_{th}}}) \quad (10)$$

From the equation it is clearly shows that the sub threshold leakage current is reduced by

(i) Decreasing the width of transistor.
(ii) Decreasing the mobility of charge carriers.
(iii) Reducing threshold voltage.
(iv) Exponential function of gate source voltage and drain source voltage.

Without changing the device geometry the sub threshold leakage current is reduced by proposed 8T SRAM circuit. The reason behind the without changing the device geometry is this will turn induce the second order effects of MOS transistors and fabrication of device is also too complicated.

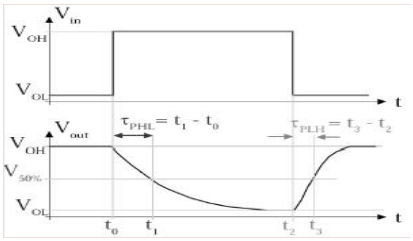


Fig. 9: Propagation Delay Graph

In exponential function of above equation the drain to source voltage V_{DS} and gate to source voltage is smaller value than V_T cause exponential reduction in sub threshold leakage current. In the proposed circuit this will be achieved by introduce the delay in the pass transistor circuit this will turn reduce the V_{GS} and V_{DS}.
The propagation delay of transistor is calculated by formula

$$\tau_p = (\tau_{pLH} + \tau_{pHL})/2 \quad (11)$$

τ_{pLH} - Low to high transition
τ_{pHL} - High to Low transition

5. Memory Array Architecture

The memory arrays are organized such a way that the horizontal and vertical dimensions of same order of magnitude in order to get the aspect ratio equals to one. Figure 10 describes the overview of SRAM memory design. A single address of N+ M bits is split into N row address and m column address. The row address is first decoded followed by column address.

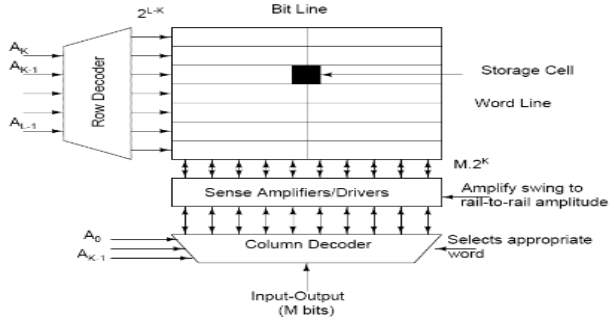


Fig. 10: Memory with Row and Column Decoders

5.1. Sections of Memory Array

The Memory Array consists of
1. Pre Charge Circuit
2. Array Structure
3. Row Decoder
4. Column Decoder
5. Sense Amplifier/Driver

1. Pre Charge Circuit: Pre charge circuit is one of important component in SRAM .The function of pre charge circuit is it enables the bit lines to charge to V_{dd} except during read and write operation.

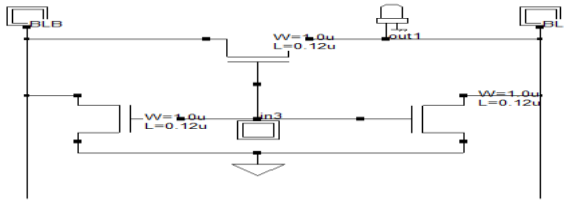


Fig. 11: Pre Charge Circuit

2. Row and Column Decoder: Row decoder is a circuit as shown in figure 12, which is used to select the particular row in a memory array. Similarly column decoder is used to select the particular column.

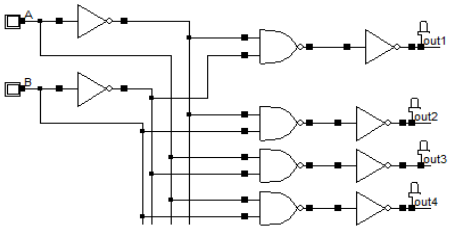


Fig. 12: Row and Column Decoder

3. Sensing Amplifier: The design of sensing amplifier plays a major role while deigning memories. The access time of memory is depends on the performance of sensing amplifier. When SE=1, the amplifier senses the differences between Bit and bit bar and produces the voltage.

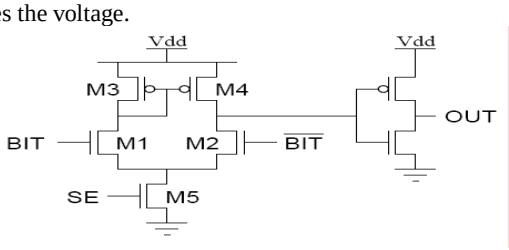


Fig. 13: Sensing Amplifier

6. Implementation of Proposed Circuit in Array Structure

The proposed 8T SRAM cell is implemented in array structure in different sizes and parameters are analyzed. Figure shows the 8x8 array structure analysis using proposed circuit.

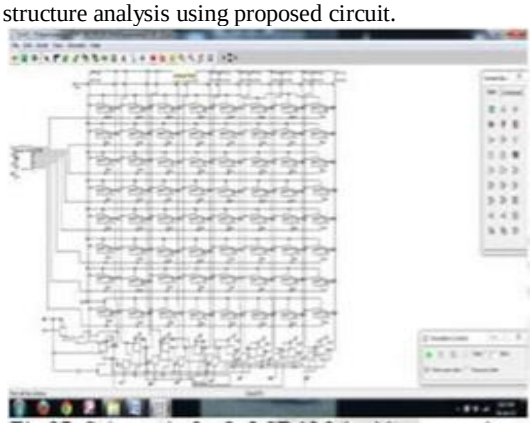


Fig. 14: Array structure using 8T SRAM cell

The memory array is constructed using 3:8 decoder for row and column decoder circuit and latch type differential sensing circuit is used .consider that for writing data in array circuit first select the row address followed by column address then set the data in bit line and bit line bar that is read by sensing amplifier and produce the output voltage.

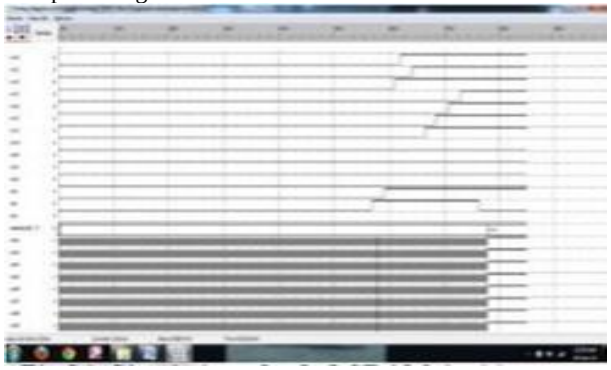


Fig. 15: Timing Analysis of 8x8 SRAM Array

7. Simulation and Results

By simulating the SRAM cell under different approaches at Vdd=1v and T=25^0 c Table 1 show the power comparison of different approaches for reducing the sub threshold leakage current in an SRAM array.

Table 1: Comparison of Power in SRAM Array

Array size	6T SRAM (uw)	P-gate(uw)	G-gate(uw)	Stacking(uw)	9T SRAM(uw)	Proposed 8T SRAM (uw)
2x2	495	950	935	224	154	125
4x4	666	1957	1256	468	234	195
8x8	845	3286	3134	624	350	258
16x16	1026	5342	5256	842	438	432
32x32	1253	8436	5436	1024	958	512

The graphical representation of Table 1 is shown in figure 16.power dissipation is compared between 6T, stacking technique,9t and proposed 8T SRAM structure in an array.

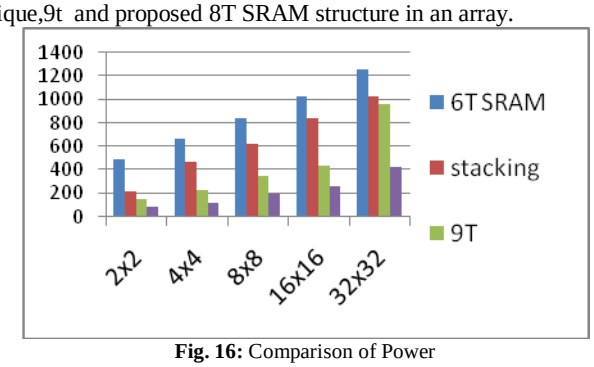


Fig. 16: Comparison of Power

Table 2 show the delay calculation of different approaches for reducing the sub threshold leakage current in an SRAM array.

Table 2: Comparison of Delay in SRAM Array

Array size	6T SRAM (um^2)	P-gate (um^2)	G-gate (um^2)	Stacking (um^2)	9T SRAM (um^2)	Proposed 8T SRAM (um^2)
2x2	73	78	83	653	92	84
4x4	288	310	314	16784	464	325
8x8	1148	1160	1154	64324	1468	1279
16x16	4645	4828	1245	248436	5942	5210
32x32	18464	19248	19526	3563241	24326	20840

From the Table it clearly shows that the delay values get reduced in considerable amount while comparing with other technique.
Table 3 show the area calculation of different approaches for reducing the sub threshold leakage current in an SRAM array.
From the Table 3 it clearly shows that the area values get slightly increased in considerable amount while comparing with 9T and 6T technique but less than stacking technique.

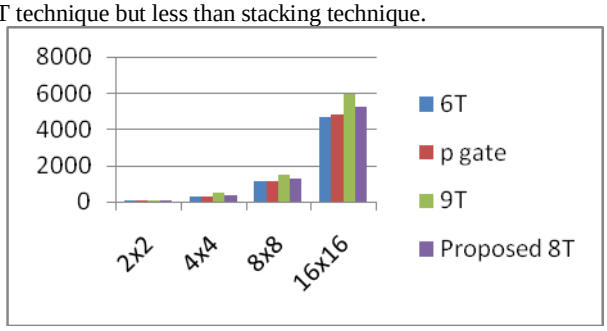


Fig. 17: Comparison of Area

Table 3: Comparison of Area

Array size	6T SRAM	P-gate	G-gate	Stacking	9T SRAM	Proposed 8T SRAM
2x2	382ns	364ns	395ns	412ns	376ns	344ns
4x4	763ns	725ns	784ns	826ns	756ns	688ns
8x8	1232ns	1195ns	1295ns	1520ns	1426ns	1081ns
16x16	82us	76us	89us	115us	82us	64us
32x32	240us	220us	222us	274us	212us	186us

8. Conclusion

The leakage current contributes 40% of total power dissipation in a memory cell. Proposed technique will reduce the power dissipation by 75 % as compared to other technique .By reducing the sub threshold current has greater impact on power dissipation. This technique will reduce the delay by considerable amount and slight increase in area which is also acceptable amount only Simulation carried out in 90 nm technology that is well suitable for industrial applications.

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