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Research paper

Review a Low Power CMOS Charge Pump using Power Gating Techniques to Reduce Leakage Power

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Abstract

In most case, charge pump circuit is designed based on capacitor, where voltage is increased at each stage depending on each stage voltage gain. Major elements are all charge pumps circuits one is Pumping capacitors and diode connected MOS.To increases pumping efficiency is very higher for each stage of charge pump circuits. Pumping efficiency are limiting by two parameters one is parasitic capacitance and threshold voltage. The power dissipated from the circuit can be increased by attain of leakage current .To resist this leakage in the circuits the supply voltage is major concern. To reduce the leakage with the help of power gating technique .Charge pump circuits are to be designed and verified by using tanner t-spice tools.

Keywords: *Capacitor, Charge pump, Power Gating Techniques, Power leakage, Threshold, Tanner Tools.*

1. Introduction

A charge pump is designed based on capacitors and NMOS, PMOS switches it is one of the converters such as dc-dc converters, here the purpose of the capacitor acts as a storage media it will produces higher outcomes (output power is high compared then input power).charge pump is act as a switching element and also it will control the connection of voltage flow to the capacitor. Charge pump is one of the energy harvesting application and also it's a non –volatile memory. Volatile memories are EEPROM & Flash memory, floating-gate devices (programming). Charge pump is a switching device based on capacitor it operated by low supply voltage but need high voltage to drive step-up transformer (analog switched).

A charge pump structure is always developing a highest output voltage from the lowest input voltage for this process amplifiers and transformers will not involves. A developing highest output voltage for each stage directly transferred charges to the corresponding so that the capacitors are made-up off semiconductor technologies (silicon) for that the input voltages are limited. Sometimes large amount of energy will be lost because that time the load current is decreased. In VLSI technology is now a day's very popular and also it has more advantages such as low power, low area, low time based on fabrication process, it will always depends on CMOS technologies. These technologies is decreased the power dissipation but it cannot able reduce the leakage current and also the circuit delay. However in this circuit need to reduce the delay at that same time decreased the leakage/static power or current by using VLSI methodology, that name is called low threshold .in this circuit applying low threshold achieving by power gating method. In this power gating technique has many methods to reduce the leakage such as sleep mode, active, mode, dream mode, MTCMOS mode, here using MTCMOS (multi-threshold

The rest of the paper is categories as follows. Section II surveys all of the previous works with cons and pros. Section III Analysis the charge pump's structure and their comparisons. Section IV Simulation results of Dickson charge pump, six stage charge pump and six stage charge pump prototype by using Power gating technique with the help of Tanner tools. Section V Conclusion and References.

2. Related Works

2.1. A Four stage Dickson Charge Pump

The circuit consists of two pumping clocks φ1andφ2, which are anti-phase and have voltage amplitude of Vφ. The diodes are replaced by MOS switches. This circuit consists of capacitor stages connected by diodes and coupled in parallel by two non-overlapping clocks. The diode-connected NMOS transistors are used instead of p-n junction diodes for developing the design in standard CMOS process.

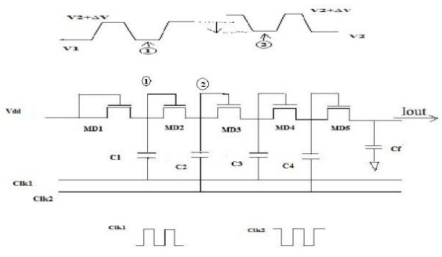


Fig. 1: A Dickson Charge Pump

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Table 1: Analysis of voltage on Dickson Charge pump

Input voltage	Frequency	Stop time	Dickson charge pump(round off)
1.0V	100.0M Hz	3000.0n s	15V
2.0V	100.0M Hz	3000.0n s	16V
3.0V	100.0M Hz	3000.0n s	17V
4.0V	100.0M Hz	3000.0n s	18V
5.0V	100.0M Hz	3000.0n s	19V

2.2. Implementation of Static CTS's in Charge Pump

An advanced version of Dickson charge pump it will increases the pumping gain. This type of charge pump made up of MOS switches and also capacitors. MOS switches properly ON/OFF during pumping at each stage. This type of charge pump produces forward voltage drop at each stage of pumping. In this construction MS2 switch can never ever switched off totally because it can able to do reverse charge sharing between two nodes may it have reduce the leakage and also increasing the pumping gain automatically.

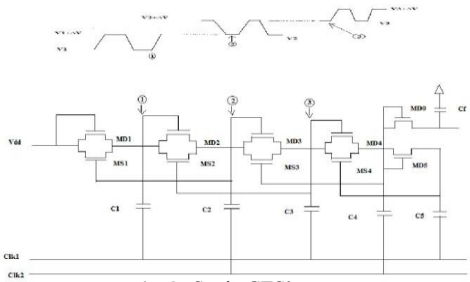


Fig. 2: Static CTS's pump

Table 2: Analysis of Voltage Static charge pump

Input voltage	Frequency	Stop time	Static charge pump(round off)
1.0V	100.0M Hz	3000.0n s	8V
2.0V	100.0M Hz	3000.0n s	9V
3.0V	100.0M Hz	3000.0n s	10V
4.0V	100.0M Hz	3000.0n s	11V
5.0V	100.0M Hz	3000.0n s	12V

2.3. Implementation of dynamic CTS's in charge pump

To reduce the disadvantages of statics charge pump by using dynamic charge pump.

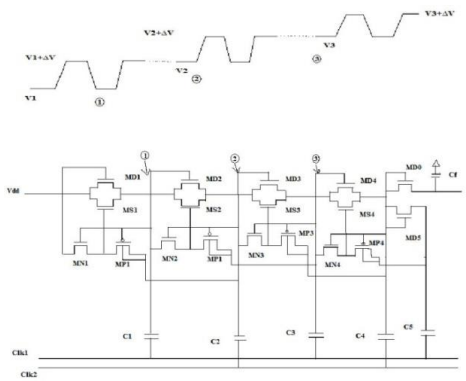


Fig. 3: Dynamic CTS's

Table 3: Voltage analysis of voltage dynamic charge pump

Input voltage	Frequency	Stop Time	Dynamic charge pump(round off)
1.0V	100.0M Hz	3000.0n s	18V
2.0V	100.0M Hz	3000.0n s	19V
3.0V	100.0M Hz	3000.0n s	20V
4.0V	100.0M Hz	3000.0n s	21V
5.0V	100.0M Hz	3000.0n s	22V

The dynamic charge pump made-up off MOS switches .The working principle everything like static charge pump .These type of charge pump provide low output power because of body effect, so that the NMOS transistor is connected output side.

2.4. Mixed-Structure Charge Pump

Minor changes –of CTS charge pump structure which combines the partially changes-CTS charge pump with a simplified cross-coupled output stage. A MOS switch when is completely on can pass charge from its drain to its source similar to a forward biased diode. It has the advantage that almost no voltage drop occurs between its drain and source terminal.

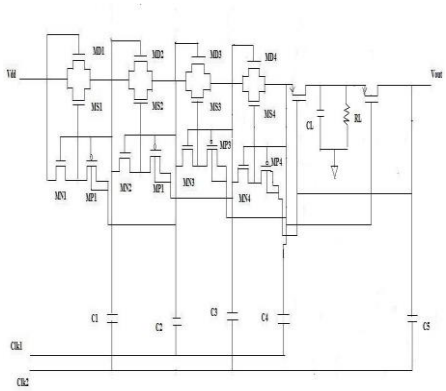


Fig. 4: Mixed charge pump

Table 4: Voltage analysis of mixed charge pump

Input voltage	Frequency	Stop time	Mixed charge pump(round off)
1.0V	100.0M Hz	3000.0ns	4V
2.0V	100.0M Hz	3000.0ns	9V
3.0V	100.0M Hz	3000.0ns	15V
4.0V	100.0M Hz	3000.0ns	20V
5.0V	100.0M Hz	3000.0ns	25V

If clock phase was properly applied for this charge pump can allow the charge only one direction in forward position when the MOS switches turned ON and OFF .in this charge pump specially constructed at each stage by dynamic inverters it will be control the ON/OFF operation at each stage

2.5. Six Stage Charge Pump

A low voltage charge pump is developed to help start up a step-up converter in energy harvesting applications. The six stage charge pump has two important parameter the first one is backward control scheme and two branches (A&B)of charge transfer switches (CTS) to direct charge flow. The first parameter uses the internal boosted voltage to randomly control the CTSs' gate, and the two branches utilize both MOS switches (NMOS and PMOS) to implement their switching structure. The combination of these two parameter operation allows the CTSs to be total turned on and off. Thus, the six stage outcomes will reduced reverse charge sharing

phenomenon and switching loss, which properly improves pumping efficiency.

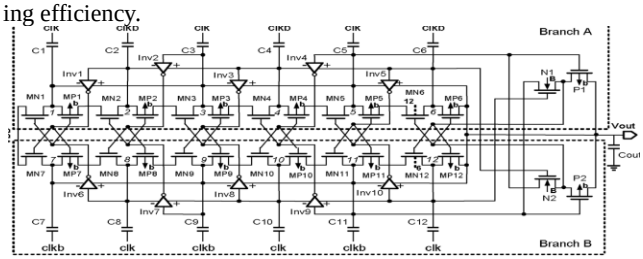


Fig. 5: Six stage charge pump

3. Comparison (Round Off Values)

Table 5: Comparative analysis on the basis of variation in input voltage

Input voltage	Frequency	Stop Time	Dickson charge pump	Static charge pump	Dynamic charge pump	Mixed charge pump	six stage charge pump
1.0V	100.0MHz	3000.0ns	15V	8V	18V		4.452V
2.0V	100.0MHz	3000.0ns	16V	9V	19V		9.78V
3.0V	100.0MHz	3000.0ns	17V	10V	20V		15.06V
4.0V	100.0MHz	3000.0ns	18V	11V	21V		20.32V
5.0V	100.0MHz	3000.0ns	19V	12V	22V	22V(with leakage)	25.07V

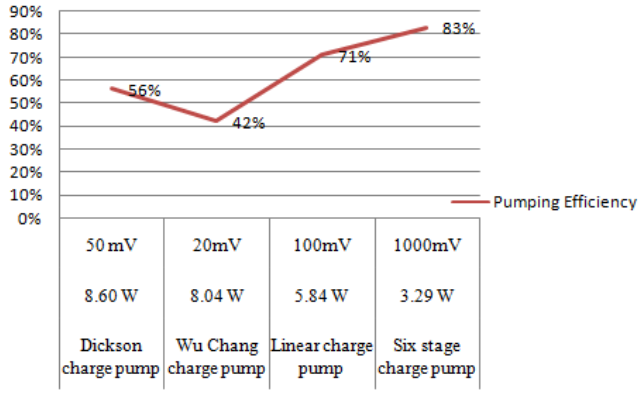


Fig. 6: Pumping Efficiency for each charge pump

4. Power Gating Technique

All types of charge pump has build by capacitor ,because of these capacitor leakage is there that name is called static leakage power .This type of leakage can be reduced by using power gating technique. Power gating techniques has many method here we are applying Multi-Threshold CMOS techniques during long periods of idleness. Power gating method was to provide more number of off modes such as active mode, dream mode; sleep mode etc, this method can able to reduce the static leakage power / current during short periods of inactivity. Power gating techniques requires a less design format and also less cost than clock gating techniques. In addition, in this paper we apply this technique only for six stage charge pump it will be reduced leakage. Six stage charge pump design and simulation we will see next part.

5. Simulation Result

The designing of this charge pump are implemented in TANNER EDA.

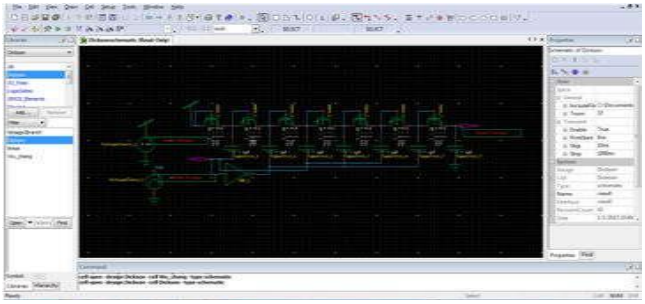


Fig. 7: Dickson Charge Pump design

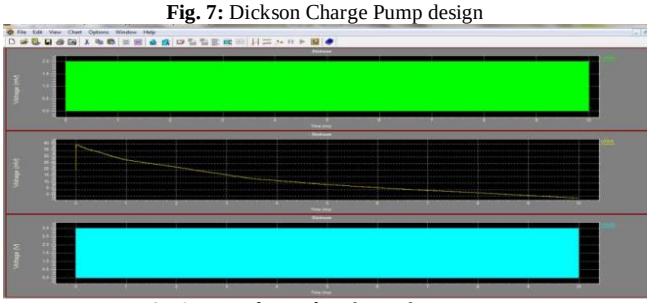


Fig. 8: Waveform of Dickson charge pump

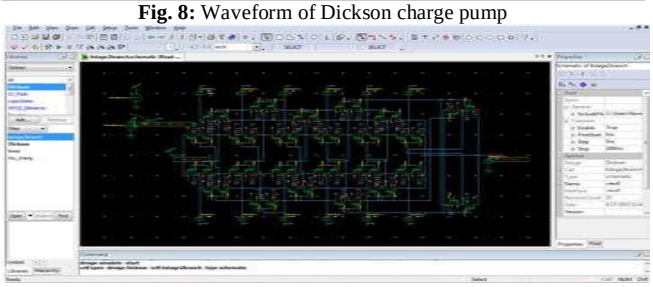


Fig. 9: Six stage Charge Pump design

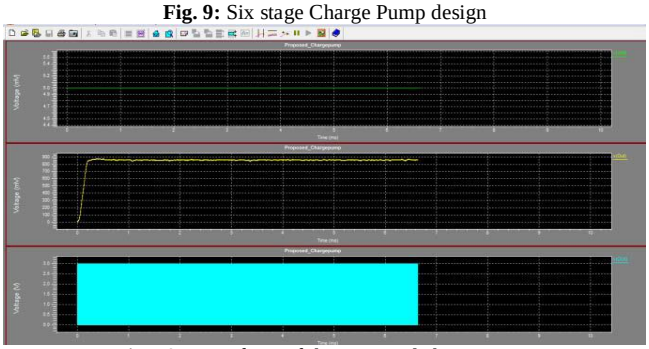


Fig. 10: Waveform of the proposed charge pump

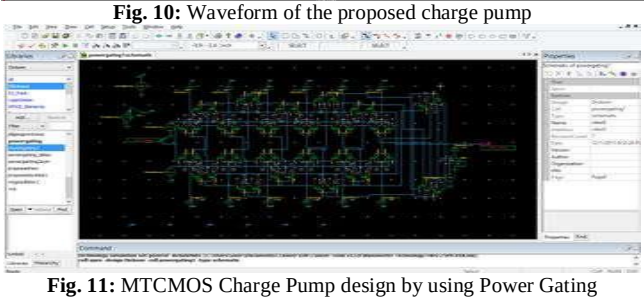


Fig. 11: MTCMOS Charge Pump design by using Power Gating

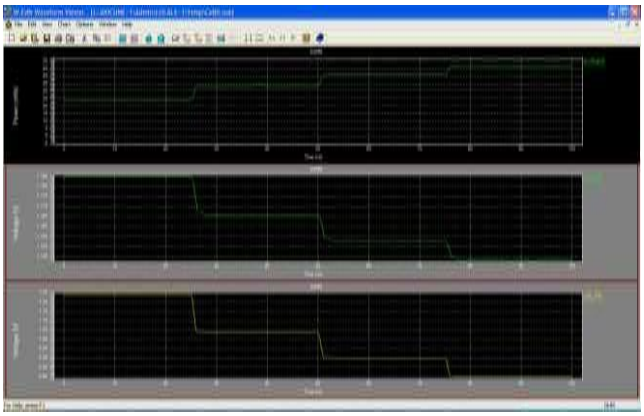


Fig. 12: MTCMOS Charge Pump design by using Power Gating

6. Conclusion

In this paper mainly discussed about all types of charge pump that is made-up of parasitic capacitance. The charge pump always provide higher value output this output we are comparing in previous part and also comparing the efficiency of all charge pump in each stage. The charge pump is too established by the test chip. it will gives better performance. However the pumping gains, transient response can be increased at each stage of charge pump. The charge pump pumping gain is calculated by formula i.e., Vout / Videal. Compared all types of charge pump designed will be modified in each stages and also the charge transferability. In this paper the six stage charge pump have very high charge transferability and also more number of capacitors. Six stage charge pump pumping gain is 85% .This circuit could be further used for the implementation of the like PLL based analog devices.

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