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Research paper

Designing and Implementation of Efficient (2^i x j) Reversible RAM-Array Module

Srija Alla*[1], Bharathi S H[2]

[1]Post-Graduation Scholar, [2]Professor,
[1,2] School of Electronics & Communication Engineering, REVA University, Bangalore India
**Corresponding Author Email: allasrijareddy@gmail.com[1]*

Abstract

In the modern digital-world, power dissipation in microprocessors is becoming a significant challenge for the researchers to design an efficient reversible logic circuit. Thus, study on reversible logic design has been rapidly increased in present days for its application in Nano technology as well as in low energized VLSI design etc. In this current study, have realized a QC (i.e. quantum-cost) efficient (2^i x j) reversible RAM array module with (3 x 3) New Modified Fredkin (NMF) reversible gate. Additionally, have introduced a Reversible D-Flip-Flop (RDFF) with less QC, and Reversible (i x 2^i) decoder which produces the effective results in terms of QC and garbage-outputs. Finally, the study analyzed the designed architecture in terms of worst case delay.

Keywords: *Quantum – Cost, Reversible Logic-Gates, Reversible D- Flip Flops, Reversible Random Acces Memory (RRAM)* **.**

1. Introduction

The reversible computing had attracted lots of attention over the existing irreversible computing due to their effective feature that is low power consumption without losing any information. The losing of information causes the dissipation of energy and generation of heat. The reason behind the losing information is when the complete input information is not recovered from its output information and 1 bit of information lost generates the KTln2jolues amount of heat energy, where 'T' indicates Kelvin-Temperature at which the execution and process is performed and K is the Boltzmann constant. So the power crises factor in the digital computing circuits can be reduced by employing the reversible computing. The reversible computing system is composed of reversible logic gates which takes m-input and gives m-output and 1-to-1 correspondence among the input and output vector which results no loss of bit information and in which input vector is fully recovered from the output vector. By this way the reversible logic process doesn't lose any information and release lesser amount of heat. The challenging task in constructing reversible circuit is to optimize various factors and cost metrics that are as: 1).Number of gates- The circuit must contains least no. of gates as much possible, 2).Constant Input- The constant input should be smallest while designing reversible logic circuits. The constant inputs parameters are added to the input which is added to nxn function to make it reversible, 3). Garbage outputs- It is an unused output of reversible gate and requires to maintain the reversible process. 4). Delay- the delay of reversible logic circuit refers to the maximum no. of gates in path form the input and the output path of logic circuit, and 5).Quantum cost- The quantum cost is parameter that used to decide the architectural complexity of each gates used in the circuit and it can be obtained from the reversible logic gates of circuit by tumble of fundamental quantum gates. Thus, the reversible computing provides a reliable and low

power design with maximum performance and optimal processing power that conserves the energy dissipation factor. [1][2]
The Random Access Memory (RAM) consists of 2D array of the memory cells and each memory cell keeps a single bit of the data information. Mostly, researchers have worked for the reversible memory elements and less work has focuses in this area in which no. of gates are not good metric and reversible-circuits are of different types of gates [3][4]. In this paper novel reversible architecture of Random Access Memory (RAM) array is designed which is efficient w.r.t to garbage outputs, quantum cost and delay factor. The system module is design and implement on the FPGA system and tested with Garbage output and Quantum cost and lastly, the presented architecture is compared with traditional architectures.
The remaining part of the paper work is arranged into the following manner: Section-2. Contributes the existing literature survey related with the presented work, Section3- presents the domain concept, Section-4 describes system design of reversible digital circuits and RAM array design, Experimental and Simulation results with performance analysis are present in the Section-5 and finally, Section-6 discusses the comparative analysis and presents the conclusion.

2. Fundamentals of Reversible Gates

This section presents the different types of reversible logic gates, its operations, and descriptions. It used in developing difficult sequential and combinational circuit

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2.1 Feynman Gate (FG):

In reversible gate it consist 2 inputs and similarly 2 outputs, is also called Feynman gate or Controlled Not Gate (CNOT). It achieves a controlled negation process. Figure-1 shows the schematic of FG, where two inputs A and B, two outputs P and Q are displayed.

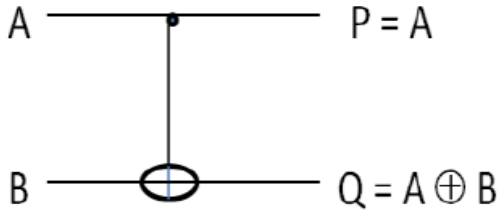

Fig. 1: The Feynman Gate representation

In figure-1 input A is interms of the control line and B is the target line. The target gets denied if the control line is set, else there will be no precess accomplished on the target line.

2.2 Double Feynman Gate (DFG):

In figure-2 shows a 3×3 FG. Here the input vectore is A,B, and C similarly the output vector are P,Q, and R. in DFG has one control line and two target line.

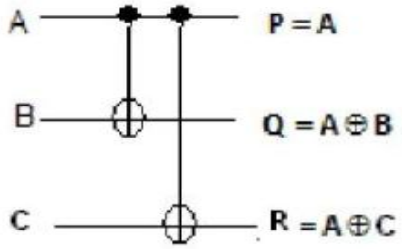

Fig. 2: The Double Feynman Gate representation

2.3 Swap Gate (SG):

The SG is a 2×2 reversible gate, it can exchanges the input and provides it to the output side. The swapping process is shown in figure-3, where the inputs are exchanged on the output side.

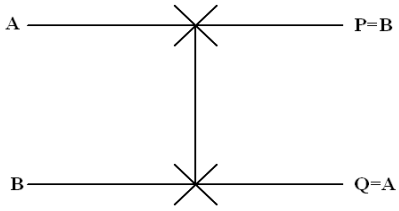

Fig. 3: The Swap Gate (SG) representation

2.4 Toffoli Gate (TG):

In figure-4 is displays the representation of 3×3 TG. In TG out of 3 inputs, 2 inputs perform as control lines and 1 input perform as target line.

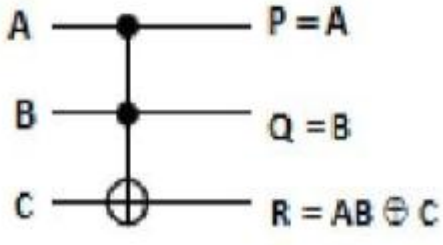

Fig. 4: The Toffoli Gate (TG) representation

The figure 3.4 shown with 3 inputs A, B, and C and 3 outputs P, Q, and R. the outcomes equation for TG is:

P=A, Q=B, R=AB XOR Z

2.5 Fredkin Gate (FG):

The figure-5 displays a 3×3 FG, which is created by E.Fredkin and T.Toffoli. The FG functions by exchanging 2 of its 3 inputs and post third input as an output.

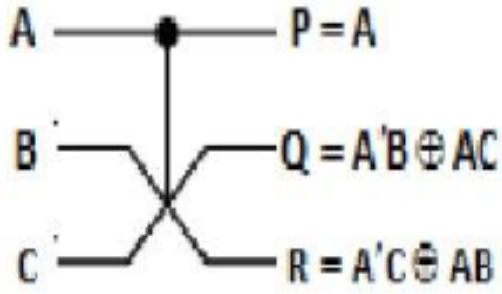

Fig. 5: The Fredkin Gate (FG) Schematic

The outcomes equation of FG is:

P=A, Q=A'B XOR AC, R=A'C XOR AB

2.6 Peres Gate (PG):

The PG is a 3×3 reversible gate, which has three i/p & o/p ports. The logical representation is shown in below figure-6. In PG, there are a 1 single control line and 2 target line. The PG is used in schematic because it has lowest quantum cost.

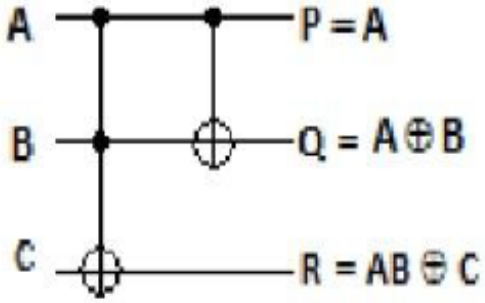

Fig. 6: The Peres Gate (PG) representation

2.7 New Gate:

A new gate 3×3 reversible is displays in figure-7. The New Gate is used to computation all logic gates like OR, NOR, NOT AND EXOR EXNOR and NAND gates.

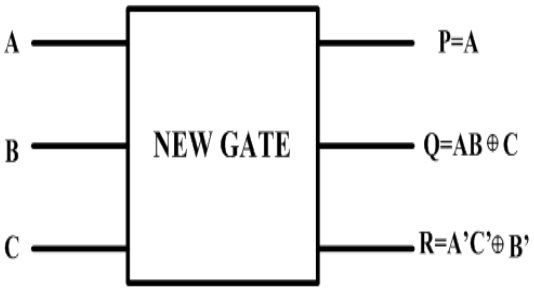

Fig. 7: A New Gate 3×3 Schematic

3. Proposed Methodology

At present, reversible logic circuits has gaining more attention owing to their low energy consumption. It means these circuits have the capability to minimize the energy dissipation which is the most significant requirement in the designing of low energized VLSI circuits. Thus, in this work have considering some fundamental reversible logic gates for the designing of RAM array

architecture on FPGA board. Therefore, this section mainly concerns about discussion of detail architectural view of proposed RAM-Array design by utilizing reversible logic gates.

3.1 Proposed RAM-Array Module Design

A modified design of proposed reversible logic gate i.e. RAMS array design is represented in the figure- 8. The proposed new modified Fredkin-gate (i.e.NMF-gate) composed with (3 x 3) Fredkin-Gate and four is the QC with 4Δ delay. If 'A' is one B and C is swapped in out-put the quantum representation is given as follows;

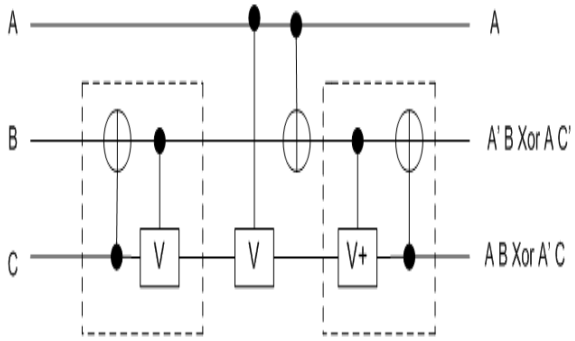

Fig. 8: Proposed NMF-Gate Quantum Representation

3.2 Proposed Reversible (i x 2^i) Decoder

The (i x 2^i) decoder is constructed using Feynman-gate. If Feynman gate contains one of input as '1' and other is 'A' then output will be 'A' and complement of 'A'. This (i x 2^i) decoder contains unit-QC, unit-delay and no garbage outputs. The circuit diagram of this decoder is presented as given below;

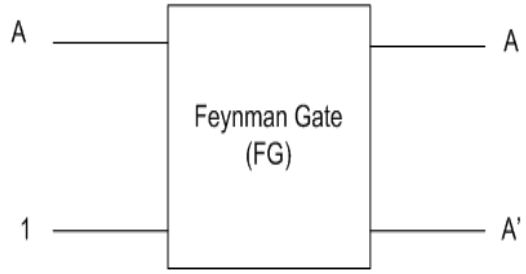

Fig. 9: Proposed (i x 2^i) Decoder

3.3 Design of (2:4) & (3 : 8) Reversible Decoders

A (2:2^2) decoder design contains single FG gate and a pair of NMF gates. The internal design of proposed (2:4) decoder is shown in figure-10(a). The Q-cost of such decoder is nine and delay is 9 Δ with unit garbage output.

Similarly, (3:2^3) reversible decoder constructed by connecting 4-different outputs of (2:4) decoders to 4-different NMF-gates the pictorial representation of this reversible decoder is displayed in the figure-10 (b).

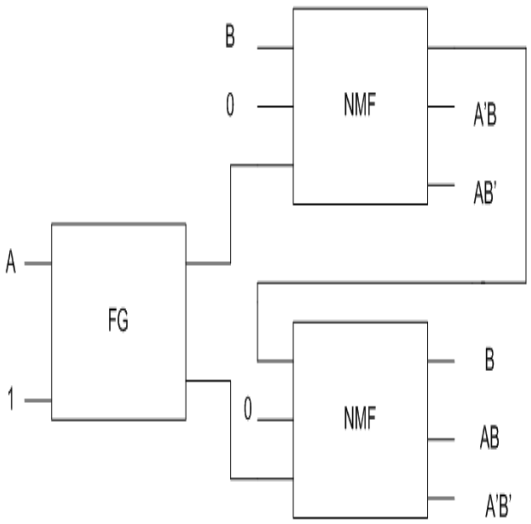

Fig. 10 (a): Design of (2:2^2) Reversible Decoder

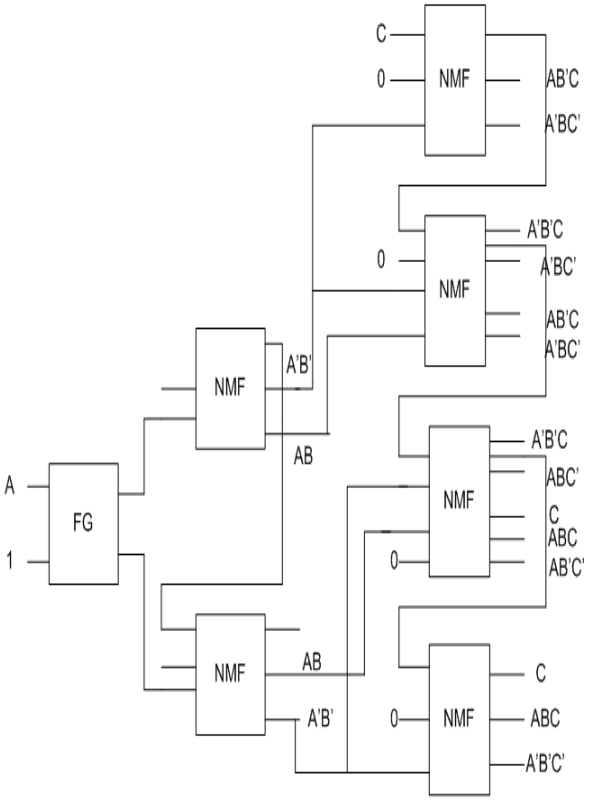

Fig. 10 (b): Design of (2:2^3) Reversible Decoder

3.4 Proposed (2^i x j) "Reversible-RAM"

The proposed (2^i x j) "Reversible-RAM" module consists of 2^i-number of rows and j^{th} no. of columns. For the election of single row of Master slave DFF, only single 2^i output lines get activate in reversible-decoder. The "WRITE" signal indicates Read/Write symbol. If the "WRITE" signal will be high, then no. of columns j-flip flops of selected rows which indicates D_0 to D_j inputs. If "WRITE" signal will low, all columns of flip-flops of selected rows will become updated with last bits at Q_1 to Q_j. The below figure-11 represents the circuitry design of proposed RRAM module.

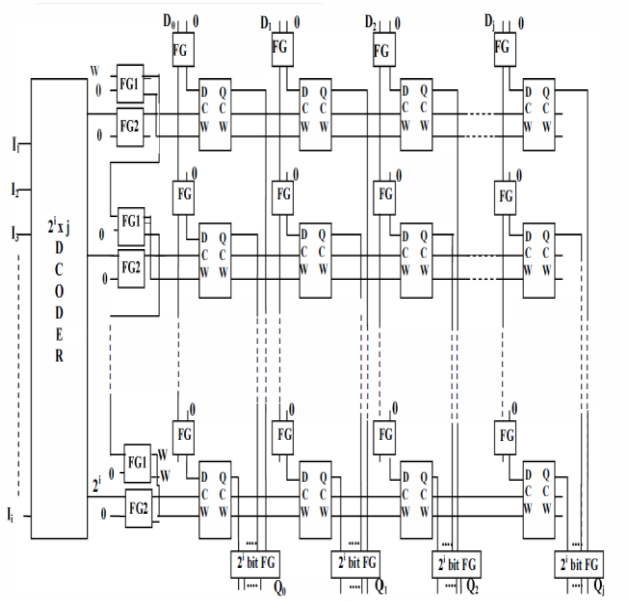

Fig. 11: Proposed (2^i x j) "Reversible-RAM"

4. Simulation Results

After the system design it has to be tested by proper tools and synthesized in Xilinx-14.7 using Verilog and simulated in Modelsim6.3f and implemented on Artix7 FPGA kit. The device is 7A100T-3 CSG324 and the followings are the related simulation results.

- **Simulation results of Reversible-RAM:**

In top level design of Reversible-RAM containing inputs are [d, i, clk, rst, and w] and makes outputs [q^0, q^2, q^3] based on inputs the system produces the simulation result which is described in below figure 1

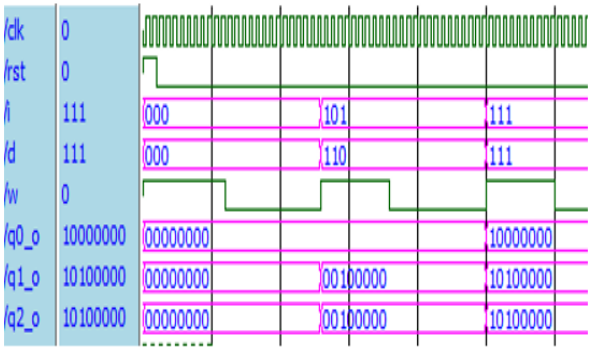

Fig. 1: Simulation results of RRAM

Similarly, in (2:4) decoder if we put [a, b] as input-parameter then it produce four output results [d1, d2, d3, and d4] is shown below in figure 2

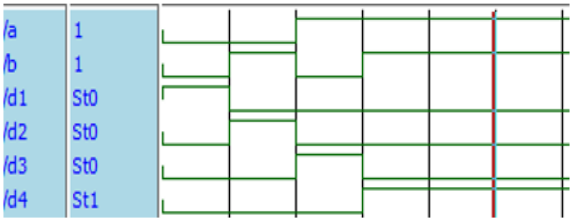

Fig. 2: Simulation results of (2:4)-Decoder

Based on (3:8) decoder, when we put [a, b, c] as input-parameter then it produce the eight outputs [f0, f1, f2, f3, f4, f5, f6, f7] is displays below in figure 3

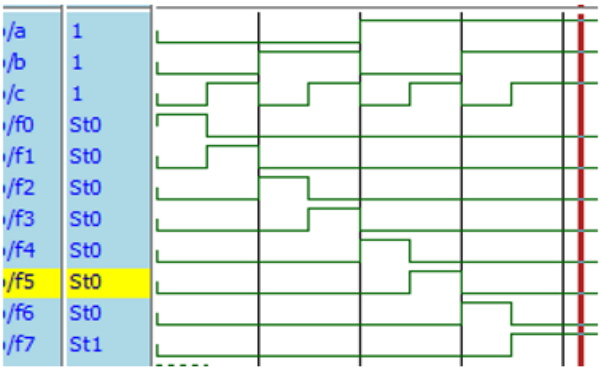

Fig. 3: Simulation results of (3:8)-Decoder

In NFG-Gate when we give [a, b, c] as the input value it generates the [p, q, r] as output values, the output results is shown in figure 4

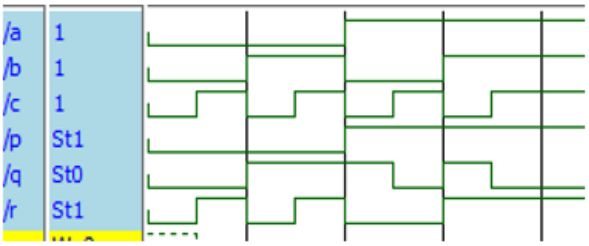

Fig. 4: Simulation result of NFG-Gate

The Write-enabled Master-slave D-FF, consist [clk, d-delay, rst and w] as inputs and generates [the one clk, q, and w_o] as output results, it displays below in figure 5

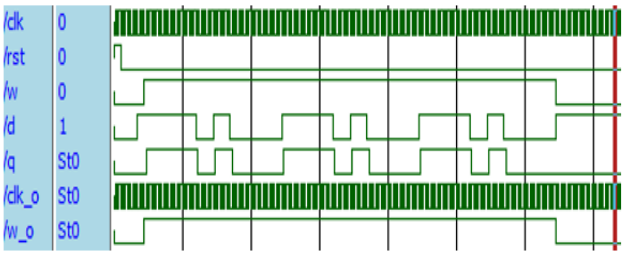

Fig. 5: Simulation results of "Write-enabled Master-slave D-FF"

Simulation result of 8-bit Feynman-gate contain [a, b, c, d, e, f, g, h] as eight inputs and produces only single output result therefor g(7:0). The simulation results is shown below in figure 6

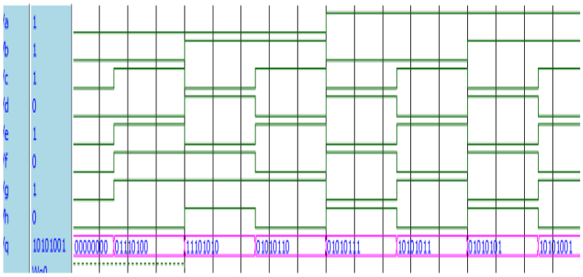

Fig. 6: Simulation results of 8-bit Feynman Gate

5. Comparative Analysis

A comparative analysis is performed on the previous designs to compare the proposed different components in RAM. The resource operation in terms of Quantum cost, no. Of gates and garbage-outputs as shown below in tables.

Table 1: D-FF Comparative analysis

D-FF Design	Quantum cost	No. of Gates	Garbage Outputs
Using F2G & FRG [1]	7	2	2
Using FS[2]	7	2	3
Using MF [3]	11	4	2
Our Design	**6**	**3**	**1**

Table 2: Write-enables Master-slave FF Comparative analysis

WE-MS FF Design	Quantum cost	No. of Gates	Garbage Outputs
Using F2G & FRG[1]	23	7	7
Using FS[2]	23	7	6
Using MF [3]	15	4	4
Our Design	**15**	**5**	**5**

Table 3: Comparative analysis of Decoder

Decoder Design	Quantum cost	No. of Gates	Garbage Outputs
Using F2G & FRG [1]	12	3	2
Using FS[2]	9	3	1
Using MF [3]	7	4	0
Our Design	**9**	**3**	**1**

Table 4: Comparative analysis of RAM

RAM Design	Quantum cost	No. of Gates	Garbage Outputs
Using FS[2]	1417	207	195
Our Design	473	194	103

RAM Design	Quantum cost	No. of Gates	Garbage Outputs
Using FS[2]	$2^i(58j+4)-7$	$2^i(8j+2)-1$	$2^i(7j+3)+i$
Our Design	$2^i(18j+6)-7$	$2^i(7j+3)+(j-1)$	$(i-j-1)+2^i(1+4j)$

In table 4, display the RAM comparative analysis with perferormance enhancements. Here no. of rows is i=3 and no. of columns j=3.

6. Conclusion

In this study, have introduced an efficient QC novel architecture of (2^i x j) Reversible RAM array module using proposed NMF-gate, RDFF, and Reversible (i x 2i) decoder. The architecture of RRAM-Array module was performed under Xilinx-14.7 ISE, the Verilog coding language. And it have been compared with existing design in terms of QC, no. of gates using, and garbage-outputs. The simulation design and analytical outcomes obtained from waveforms were testified for memory functionality of RAM. The proposed RRAM module plays significant role in the field of reversible logics to study further for the designing and development of S-RAM array & D-RAM array for their application in FPGA kit.

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