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***Research paper***

# Performance Evaluation of RingCounter using Gated Clock

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**Abstract**

Minimizing Power dissipation is one of the major concerns in the VLSI industry.Due the rapid growth in technology, there is a tremendous reduction in the chip size. Minimum power consumption has become a priority.In this paper, we propose a low power design techniquefor Ring counter using gated clock.In this paper, we demonstrate the working of ring counter using gated clock.The results are illustrated in Xilinx. The simulation results and the synthesis outputis shown.

***Keywords:*** *Gated clock, Johnson Counter, Ring counter.*

## 1. Introduction

Many a time, on-chip peripherals of processor work at lower frequencies than the actual frequency of processor. Counters have an important role under such circumstances.Counters are for counting the time allotted for a "process" by the scheduler.Further, counters can be used as clock dividers too. The main aim of doing this is to reduce the total power dissipation.

To minimize Power dissipation is one of the major concerns in recent VLSI designing. Minimum power of any system has become priority. A computer system consists of a number of sequential circuits, hence, efficient low power design of various sequential circuits is very important.Ring counters are specialisedcounter implemented with circular shift registers. Here, the output of the last shift register is fed to the input of the first register. The output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring.

## 2. Related Work

VeenaBattula and Vishal Moyal [1] have proposeda diode free adiabatic logic (DFAL) based Johnson Counter. The performance parameters in terms of power dissipation, time delay and PDP of the DFAL based circuit was used. The proposed work showed an improvement in with an energy saving upto 30%. Reversible logic has attracted a lot a attention in the recent years. Heranmoy Maity*et. al*.[2] propsed a 4-bit Johnson counter with reduced number of reversible gates, and derived quantum cost, constant inputs and garbage outputs.

Ranjana Yadav and Alka Agrawal [3] proposed a low power design scheme of Johnson Counter using MTCMOS technique. Their proposed system had lower power dissipation and power delay product as compared to the conventional CMOS design.Upwinder Kaur, Rajesh Mehra[4] have proposed a new and low-power architecture for synchronous ring counters which can noticeably reduce the switching activity of the conventional ring counters. They partitioned the ring counter into some blocks for each of which they used a special clock gator. The delay and area overhead of the proposed clock gator was independent of the block size; this enabled the designer to freely resize the blocks and compromise with area and power overheads.

There is a requirement for low power edge triggered flip flops in high speed and low power VLSI applications where heavy pipelining is used. Such pulsed latch techniques reduce the power consumption considerably in the designed circuit, hence, providing for an overall improvement in power delay product. Sani M. Ismail *et. al.* [5] proposed such a technique wherein the performance of ring counter was improved using pulsed latches.M.D. Mottaghi*et al.*[6] proposed a technique wherein the performance of ring counter wasboosted by using a negative edge triggered master slave D flip flop with 14 MOS as a part of its design compared to the conventional counter. Such designs are suited for the applications involving area, power and energy efficientVLSI designs.

## 3. Proposed Work

In this paper, we propose a simple gated clock (Fig.1.)scheme for low power dissipation. The proposed gated clock consists of two inputs U and D, and one output clk. Both the inputs produce pulses. When both the pulses are in the high state the output becomes high and the clock is triggered.In other words, the clock pulse is generated according to the inputs given through U & D.The clock generated as depicted in Table.1.The counter is sensitive to positive edge of the clock. Hence, the counter goes to the next state.

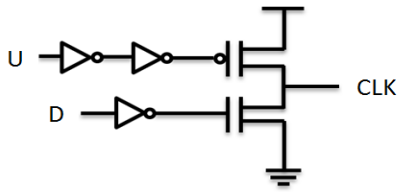


**Fig. 1:** Gated Clock

**Table 1:** Clock Pulse Generation

| U | D | CLK |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |

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| | | |
|---|---|---|
| 1 | 1 | 1 |

As we are aware, Johnson counter, a modification of ring counter, also known as Switch tail Counter is a sequential logic circuit built using shift registers. Here, the data is circulated in the counter depending on the clock pulse. Fig.2. and Fig.3. shows a simple Johnson counter and Ring Counter respectively. The clk used is the gated clock. The corresponding truth table are depicted in Table.2. and Table.3.

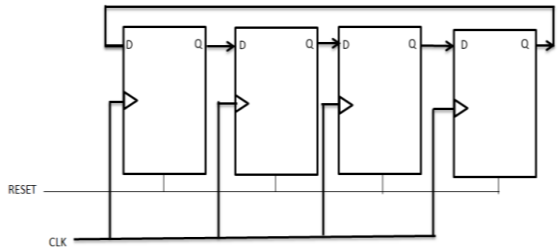


**Fig. 2:** A Johnson counter with Gated Clock

**Table 2:** Johnson Counter – Truth Table

| RESET | CLK (Gated) | Q3 | Q2 | Q1 | Q0 |
|---|---|---|---|---|---|
| 1 | X | 0 | 0 | 0 | 0 |
| 0 | ↑ | 0 | 0 | 0 | 0 |
| 0 | ↑ | 0 | 0 | 0 | 1 |
| 0 | ↑ | 0 | 0 | 1 | 1 |
| 0 | ↑ | 0 | 1 | 1 | 1 |
| 0 | ↑ | 1 | 1 | 1 | 1 |
| 0 | ↑ | 1 | 1 | 1 | 0 |
| 0 | ↑ | 1 | 1 | 0 | 0 |
| 0 | ↑ | 1 | 0 | 0 | 0 |

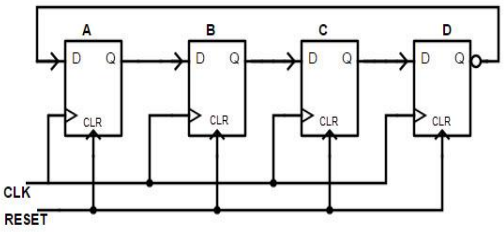


**Fig. 3:** A Ring counter with Gated Clock

**Table 3:** Ring Counter – Truth Table

| RESET | CLK (Gated) | Q3 | Q2 | Q1 | Q0 |
|---|---|---|---|---|---|
| 1 | X | 0 | 0 | 0 | 0 |
| 0 | ↑ | 0 | 0 | 0 | 0 |
| 0 | ↑ | 0 | 0 | 0 | 1 |
| 0 | ↑ | 0 | 0 | 1 | 0 |
| 0 | ↑ | 0 | 1 | 0 | 0 |
| 0 | ↑ | 1 | 0 | 0 | 0 |
| 0 | ↑ | 0 | 0 | 0 | 0 |
| 0 | ↑ | 0 | 0 | 0 | 1 |

## 4. Results and Discussion

The performance of ring counters are analyzed in Xilinx. The Simulation results (Figure 4 and Figure 5) and the RTL Schematic (Figure 6)is depicted in this section.The Power analysis results are also tabulated.

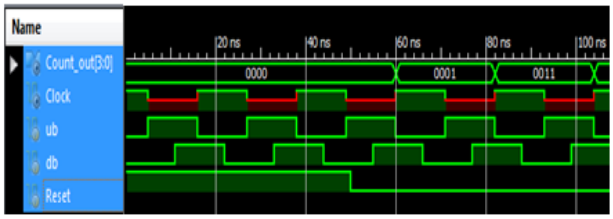


**Fig.4:** Simulation Results – Johnson Counter




**Fig. 5:** Simulation Results – Ring Counter

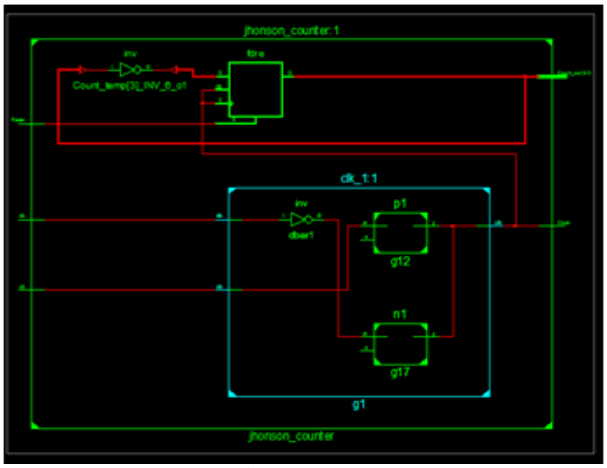


**Fig. 6:** RTL schematic of a Johnson Counter with Gated Clock

**Table 4:** Power Analysis

| Parameter | Ring Counter |
|---|---|
| **Power** | 0.56W |
| **I/O Used** | 7 |
| **Signals Used** | 3 |
| **Logic Used** | 1 |

## 5. Conclusion

In this work, we proposed a simple low power gated clock. Ring counters were clocked from gated clock. From the simulation results, it is observed that the clock remains off for half the duty cycle. This provides for power saving and hence low power consumption.

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