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***Research paper***

# A Ultra Low Power 12 Bit Successive Approximation Register for Bio-Medical Applications

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**Abstract**

Successive Approximation Register (SAR) analog to digital Converters (ADC) is favorable choice for the high resolution. As resolution of ADC increases, the no. of redundant cycles increases which increases power. So the Paper presents clock gated ADC with no redundant cycles/transition cycles for low power requirement and comparison between without Clock Gating and Clock Gated SAR. Using Simulation, Power consumption for Clock gated SAR 736.1nW at 1.8V power supply where as without Clock Gating SAR consumption is 54µW at 1.8 power supply.

***Keywords***: *Clock Gating, Power Consumption,*

## 1. Introduction

In Present scenario, there are wide applications of less power and average resolution analog to digital Converters (ADC) in different areas such as biomedical applications; wireless communication [1, 2]. In biomedical kind of application, SAR ADC is very useful due to its efficiency. The Block diagram of SAR ADC is exposed fig.1 and analog - to - digital conversions is finished on basis of the algorithm of binary search [3–6, 17]. As converter requires multiple comparisons as well as clock cycles for a generation the digital value due to which a sample - hold (S-H) circuit is used to store analog value. The polarity variation between reference voltage and analog sampled signal is determined by comparator. The Successive Approximation Register logic triggered by the comparator output which; further organize reference voltage for the next comparison which feeds by DAC.

In such type of ADC major sources of power utilization are comparator, DAC and SAR system. Main emphasis is done on power expenditure in SAR logic. For reduction of Power, different techniques are used at circuit and systems level like as clock system, voltage scaling, leakage reduction, logic reordering and interconnect optimization.

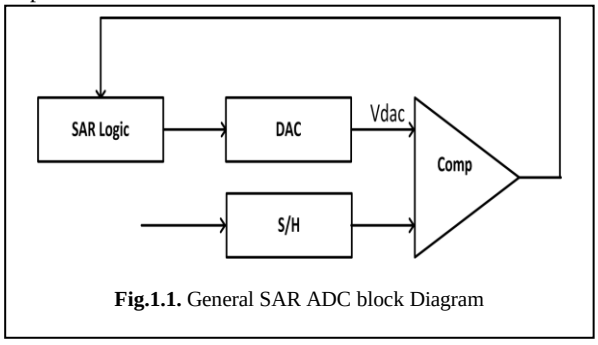



**Fig.1.1.** General SAR ADC block Diagram

Also, depicted that most power utilizing component is clock system.[7]. In article, 12 bit successive approximation register using clock gating technique is proposed that rely on initializing the clock only if required.

Section 2 illustrate the conventional SAR and also explain it has how much extra clock cycles and it consumes how much power. Section 3 and 4 illustrates the different types of Gate based Clocking Techniques and the architecture of Low power SAR ADC. Section 5 illustrates the projected 12 bit successive approximation register. Section 6 offers the various performance simulation results in 180ns CMOS technology. Section 7 provides conclusion and futuristic of the proposed design.

## 2. Conventional SAR

In different SAR's, Conventional SAR is most common and depicted in fig. 2.1.[8]. It consist of many n-bit registers i.e shift registers. A Kth FF (Generic) is linked into multiplexer for selection of three data inputs coming from, shown in figure 3:

a) (k+1)th flipflop(ff) output (right shift).
b) Comparator (Cmp) output (data load)
c) (kth) flipflop(ff) output it-self ( for-memorization)

Table -1 demonstrate relationship among Flip Flop (FF) operation and data inputs

Table 1 : FF Operations

| A(K) | Q(K) | Operation |
|---|---|---|
| 1 | x | Memorization |
| 0 | 1 | Data Load |
| 1 | 0 | Shift right ($Q_{k+1}$) |

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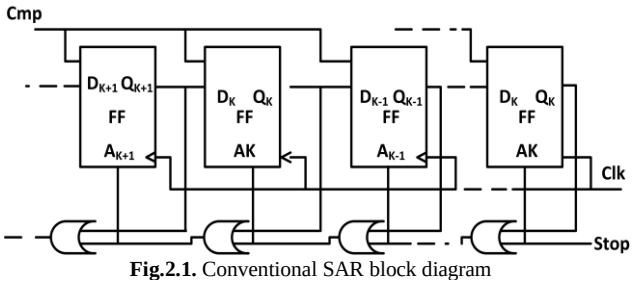



**Fig.2.1.** Conventional SAR block diagram

To illustrate the relationship, 8 bit SAR register is demonstrated in Figure in Table 2. MSB to be 1 and all other bits to be 0 are primarily assumed by SAR. During first clock cycle, the true-value (a8) for MSB is allocated by the output signal of the comparator (Cmp) and second MSB, is forced to be 1. The procedure will be continued until all bits are assigned, to their true values. To stop the conversion process, an OR gates sequences are added as depicted in equation (1).

$$A0 = \text{Stop}$$

$$A(k) = A(K-1) + Q(K-1) \quad (1)$$

**Table 2:-** Process of Conversion in SAR

| Conversion step | SAR Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | b8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | b8 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | b8 | b7 | 1 | 0 | 0 | 0 | 0 | 0 |
| 4 | b8 | b7 | b6 | 1 | 0 | 0 | 0 | 0 |
| 5 | b8 | b7 | b6 | b5 | 1 | 0 | 0 | 0 |
| 6 | b8 | b7 | b6 | b5 | b4 | 1 | 0 | 0 |
| 7 | b8 | b7 | b6 | b5 | b4 | b3 | 1 | 0 |
| 8 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | 1 |
| 9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b0 |

This equation is used when the result of conversion, can be stored up in a SAR at last step of conversion, of successive approximation sequence. The conversion table -2 illustrates that every FF requires n no. of clock cycle to end the process of conversion that signify n2 clock pulses will be required for the whole register. There are various redundant pulses, which dissipate power without effecting on output of FF.

# 3. Gate Based Clocking Techniques

## 3.1. AND Gate

Due to its simple logic circuit, this clock gating technique is most common used. For gating the clock, 2 input AND gate is connected between one terminal of circuit ordinary clock and other terminal is connected to Enable and output of AND gate, is known as Gated Clock output that is given to circuit where this gated applied to i.e. Clock to input to the register of SAR. When enable is high, the output of this gating varies according to ordinary clock. The circuit diagram of AND gating is shown in Fig3.1. [11, 12]

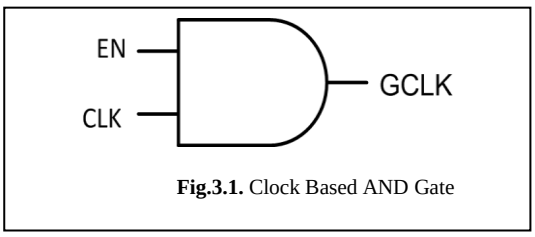



**Fig.3.1.** Clock Based AND Gate

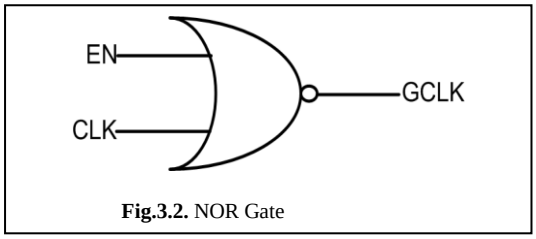



**Fig.3.2.** NOR Gate

## 3.2. NOR Gate

NOR based gating technique is generally used for positive edge of ordinary clock that given to digital circuits. In clock system, the output of NOR Gate provide 1 when both inputs are zero i.e. Enable and ordinary clock inputs are zero. Enable Signal is passed through NOT gate before applying one of input to NOR gate so that gated clock output is obtained when enable signal is on. Gate clock output is given to digital circuits. The circuit diagram of NOR gate gating is shown in Fig3.2. [11, 12]

# 4. Low Power Design SAR

Two approaches are proposed for designing of SAR logic one of them is proposed by Anderson which consist a sequence register and code register and in this logic 2N Flip-flop is used. Other one is that proposed by Rossi that consist N no. of flip flop and some digital circuit. These configurations perform on basis of binary search algorithm. The objective of this article is to reduce power consumption of sequence/code register Configuration SAR Logic. At the time $t_0$ (starting time), the 1st register determines the value of Most Significant Bit and to be set to 1. This value is putted on the bus. Now value of MSB is converted to its analog value and compared with sampled input of SA DAC by the comparator. The Comparator establish whether Most Significant bit should be left 1or if it should be reset 0 during time, $t_1$.In this way, same conversion process is repeated. As see, there are two clock pulses that are active in each conversion process. The order of these register are from MSB to LSB and its values are calculated, after that these values are stored in their respective register.

## 4.1. Fundamental Unit of SAR

The basic unit of SAR is D flip-flop and D flip flop are design with transmission gates are show in Fig.4.1. This type of flip flop is positive edge triggered and there is reduction of no of transistors as comparable with conventional D flip flop.

## 4.2. Sequence/Code Register Configuration

Two types of registers are basically used in this Configuration. The former i.e. sequencer registers, is used to provides the sequence and later one i.e. code register, is used to save value of bits. The Sequence and code register arrangement is shown in fig.4.1.
To minimize the delay, the arrangement is such that the Q-bar (non-Inverted) outputs of sequence registers (shift register) are connected to set the registers inside the code registers. As reset line is connected to set line of first flip flop and also connected to

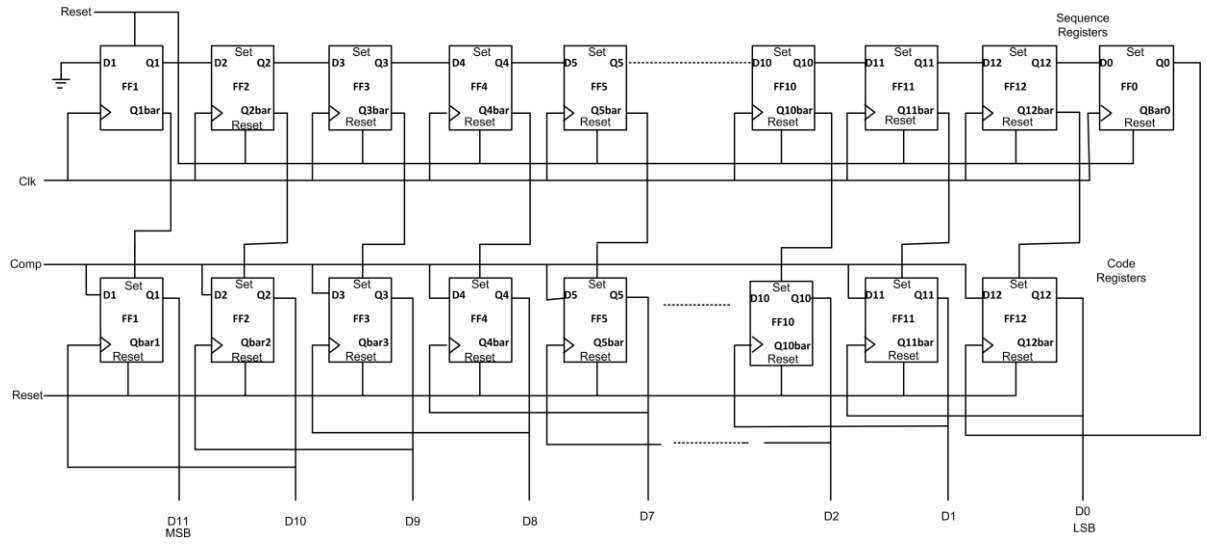



**Fig.4.2.** General Block Diagram of SAR Register

reset line of other flip flop of sequence registers. Also, same reset line is connected to reset line of other flip flop of code registers. So reset line controls the set and reset of sequence registers and code registers. Now firstly, the reset line set to be 0V and output of first flip flop is set to 1 (Q) and 0 (Q-bar) respectively. Also the output Q-bar is connected to set line of the first flip flop of code register, so Q-bar control the set line of first flip flop and its output goes to 1. This stores the Most Significant bit. As it is MSB, its value is weighted by full scale range of voltage, which is 0.5Vref. It is noticeable that reset is done in all sequence registers and set is done in all code register except first flip flop of code register that at logic 1. The outputs of other code registers are at logic 0. In this trick, MSB of sequence is 1 and all other are 0. Now analog equivalent of this weight is generated by Digital to Analog Converter (DAC). Further Reset line goes to high and Clock is event triggered, and then the output (Q) of first flip flop turns into to 0 because the input (D) to first flip- flop grounded. Now output of 2nd flip - flop goes to high and thus the transition of low to high, 2nd flip flop triggers the code register of 2nd flip - flop to store high value that is comparator output to its output. When again clock signal goes high and run further, 2nd flip flop of sequence register goes to low and it's corresponding, code register output goes also low. This conversion process is repeated for each flip flop until N clock cycle with a high logic comes from flip flop of sequence register controlling least significant bit of flip flop of code register.

## 5. Proposed Clock Based SAR

As discussed, there are many redundant clock pulses in the conventional SAR as every FF changes its state once or twice during entire conversion process. Such type of difficulty can be solved by means of the clock gated FF given away in Fig. 5.1. [9].

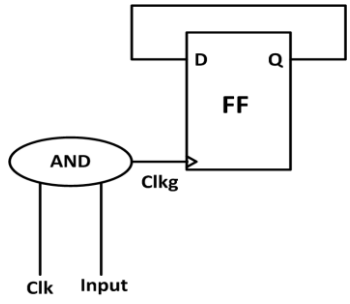



**Fig.5.1.**Clock Gated Flip Flop

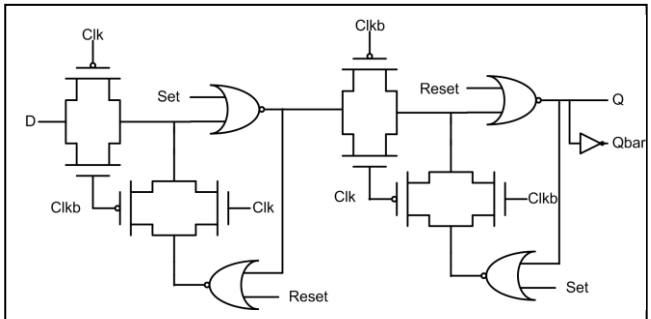



**Fig.4.1.**Transmission based D flip flop

The FF takes the output of logic block. Flip-flop's gated input terminal and the clock signal is taken as isolated. The change in states of the clock signal depend its frequency. It does not participate in the activity of the FF input signal. According to the result, there are many extra pulses that consume power without effecting on the state of FF.

This problem is resolved by the clock gated FF. The main idea that by connecting logic block terminal (AND Gate) to flip-flop clock port and output of FF , Q, to input port, D. By arrangement of this pattern, Clkg i.e. gated clock signal, shall be stay active as long as FF desires to varies it's state and proposed clock based SAR is shown in fig. 5.1.1. A clock gated signal will never be activated, if a FF holds it's state. The main concept is that when input (D) and clock are high, the output of the gate provides the Clock to the register of SAR.

## 6. Simulated Results

The SAR is compared between SAR register without Clocking and SAR register with clock gated. In this experiment, the external factors like capacitive load have excluded from measurement. So power of switching is considered only by exclusion of external loads. The no. of count of transistor is increased in Clock Gated SAR because AND is required in Clocking System. Each AND Gate is realized with 6 transistors.

Using 180nm CMOS technology, the simulated results of transient response of SAR logic without Clock Gating technique as show in fig. to compute its performance at 500 Hz at 1.8V supply on spectre simulator, is shown in Fig.6.1.

The Comparison table 3 shows the summary of simulated results.

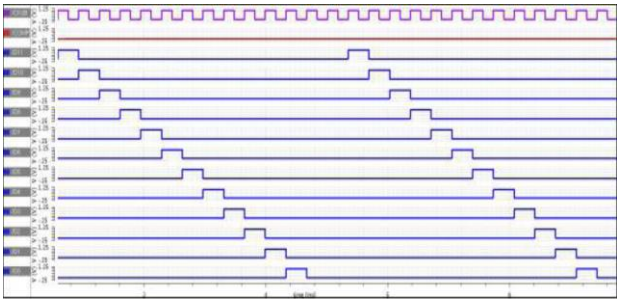


**Fig.6.1.** SAR without clock gating

Using 180nm CMOS technology, the simulated results of transient response of SAR logic with Clock Gating technique as show in fig.6.2 to compute its performance at 500 Hz at 1.8V supply on spectre simulator, is shown in Fig.

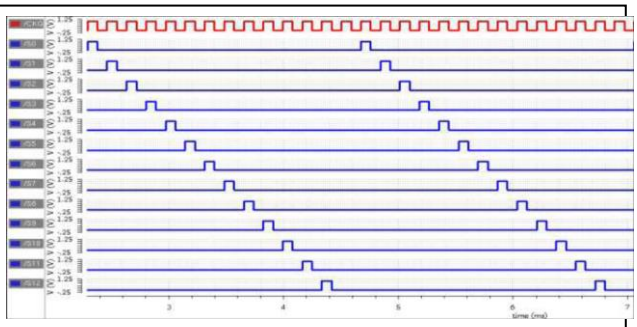


**Fig.6.2.** SAR without clock gating

**Table no 3**

| | SAR Without Clock Gating | SAR with Clock Gating |
|---|---|---|
| Technology | 180nm | |
| Supply Voltage | 1.8V | |
| Resolution | 12 | |
| Power Consumption | 54µW | 736.1nW |
| Extra No. of transistor required in Clock gating Technique | 72 | |

From Table no 3, Consumption of power of without clocking system is more as compared with Clocking system. Whereas Consumption of power is reduced, but no. of transistor are increased which also consumes power.

## Conclusion

For Bio-medical applications, 12 Bit SAR has been designed for elimination of redundant cycle of clock signal. High percentage of power is saved by the proposed design as compared to Convectional SAR. The proposed design (register) has been designed with supply of 1.8V in 180nm CMOS technology. The proposed register saves power using Clock Gating Technique.


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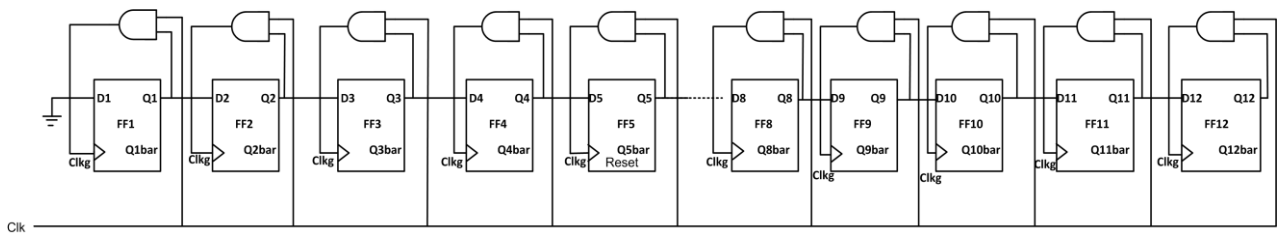




**Fig. 5.1.1** Block diagram of Clock Based Proposed SAR