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Research paper

FPGA Implementation of UART with Single Error Correction and Double Error Detection (UART-SEC-DED)

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Abstract

The Universal Asynchronous Receiver Transmitter (UART) is the very simple and significant sequential communication protocol which is basically utilized for microprocessors & microcontroller systems. It is a shorter range communication protocol, which able to perform half-duplex and full-duplex type of communication at baud rates. Though, UART is a type of shorter range communication still they are not resistant to noisy channel which leads to communication errors by flipping or loosing of bits. These kinds of signal errors are named as forward-errors. The correction of forward errors is a mechanism to handle and rectify those errors (i.e. Burst errors and Random bits error). Thus in this methodology, have introduced a UART-SEC-DED communication module design which utilizes the Hamming encoder and decoders to achieve the forward error correction. Finally, the proposed system will simulated and implemented on FPGA board and experimental outcomes shows the better efficiency in single error correction and detection of double errors.

Keywords: *AES, ASIC, Data security, GPP, VLIW architecture.*

1. Introduction

A "Universal Asynchronous Receiver Transmitter" called UART which is sub system component of serial communication IC module that is implemented on the CPUs mother board and is responsible for enabling communication or sharing data between the serial devices. The main function of URTA microprocessor is to receive and transmit the data into two way format that it converts parallel data format into a serial data stream that is sent via communication medium as analog signal and when these analog signals is received in form of serial data and it converts them to parallel data and send back to source system to communicate. [1]

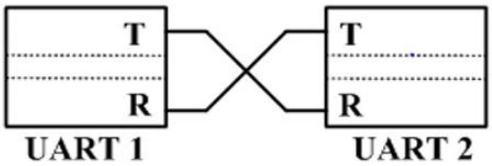

Fig. 1: Communication between UART

The above figure1 shows a simple connection setup between the UARTs to perform communication process. TheUART devices contains Receiver pin and the transmitter pins in which formulation of connection is made in such way that the transmitter pin of one UART is linked to receiver pin of another UART device and in the same way receiver pin of one UART is linked with Transmitter pin of another UART device. The first UART device receives set of bytes of data and transmits the individual bits in a serial format and a second UART re-assembles the bits into total bytes. [2] [3]

The serial process of data transmission in UART devices performs in the data frame at some frequency rate that is called baud rate, which having at least one start bit, 4 to 9 data bits, one stop bit and Parity bit may optional as shown in figure 2.

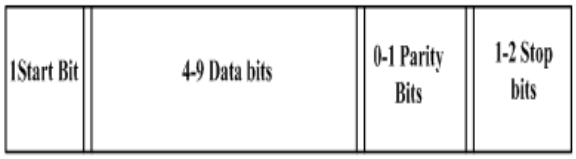

Fig. 2: shows UART Data Frame Formatting

In the communication process the link medium is generally influenced by some environmental disturbance and noise factor such as external and internal noise, signal interference. These noise factors created unwanted impact on the data that is transfer via channel causing random bit errors and some other UART errors such as Overrun error Under-run error, Framing error, Break error, Parity error caused by thevariance of baud rates and dropping of framing bits. There are various methods that are adopted to control such errors by detecting random bit error and correcting these errors. The detection technique used to identify the location of errors in the data bit streams by employing redundancy factor into the transmitted bits and then ensures the received bits for its consistency and correction techniques such as Hamming coding , Manchester coding, Hamming-Manchester coding technique that are used for performing reconstruction task on the data bits errors signals. [3]

In this paper a novel framework of UART with Single bit Error Correction (SEC) and Double bit Error Detection (DED) is proposed. The proposed model issimulated and implemented on the FPGA and tested with Adaptive constraints and lastly, the presented framework is compared with traditional models. The

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rest of the paper is organized as- Section-2 provides detail review of existing techniques. Section-3 presents the domain concept of UART design; Section-4 describes system design of proposed SEC and DEU UART design, Experimental and Simulation results with performance analysis is present in the Section-5 and finally, Section-6 reveals the conclusion and the future work.

2. Basic Concept of UART Design

The UART design has capabilities of error correcting and error identifying. The UART architecture and its capabilities are defined here.

Error Identifying UART Architecture:

The UART architecture can identifying errors like parity error, over-run error, frame error and break error. Figure 3 displays the general architecture of UART architecture. It consist four essential modules, which are Receiver, Line Control Register (LCR), Baud-Rate generator and Transmitter. [4]

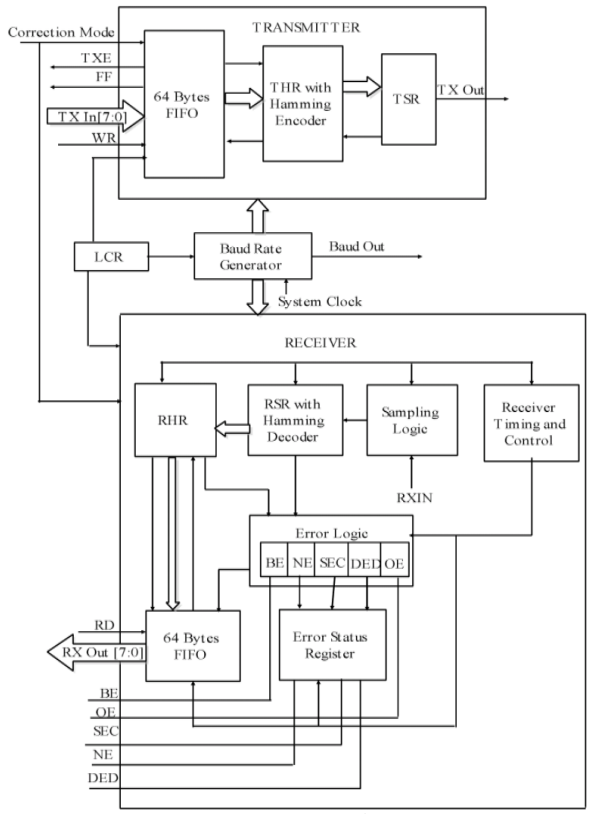

Fig. 3: General architecture of UART module

i. Receiver:

In receiver sections it includes an 8-bit Receiver Hold Register (RHR), 12-bit Receiver Shift Register (RSR) 16-bit FIFO and error logic block. Primarily, the RSR transfer 8-bit data to RHR. The error logic section used rest bits which is not sends to RHR. The RHR sends it to FIFO, if FIFO is unfilled from which an equivalent data is formed. The error logic identify over-run error, break error, parity error and frame error. After that it arranged bits in status registers sequent to PL, SL, OL and break bits.

ii. LCR:

The LCR is a byte register, which contain 8-bit and it helps in baud rate configuration and frame formatting.

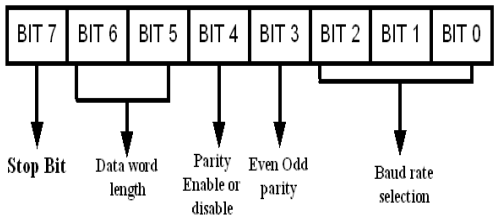

Fig. 4: Format of LCR

Figure 4 has shown the LCR format, where the function of bits 0, 1 is to select the length of word from 5-8 bits. Bit-2 is for sets the stop bit length. The bit-6 works for sets the break control and bit-7 for sets the Divisor Latch Access Bit (DLAB). Where, 0 allows access to IER, THR and RBR and 1 is allows to access from DLL and DLM.

Table 1: LCR bit-configuration details

Bit	Value			Description
	Bit2	*Bit1*	*Bit0*	*BR Sel.*
0,1,2	0	0	0	57600
	0	0	1	38400
	0	1	0	19200
	0	1	1	9600
	1	0	0	4800
	1	0	1	2400
	1	1	0	1200
	1	1	1	600
3	0			Even Parity
	1			Odd Parity
4	0			Parity Disable
	1			Parity Enable
	Bit4	Bit3		DW Length
5,6	0	0		5
	0	1		6
	1	0		7
	1	1		8
7	0			1 Stop Bit
	1			2 Stop Bits

iii. Baud-Rate Generator:

It is a function which helps to create the baud rates for the receiver and transmitter. Here not compulsory for different functions like reads and writes. For calculating the baud rate the formula is shown below,

$$BR = \frac{CF}{(SR) \times (D)}$$

Where BR: Baud-Rate;
CF: Clock Frequency;
SR: Sampling Rate;
D: Divisor.

iv. Transmitter:

The transmitter segment receives parallel data and also builds a serial data frame and sends it from the Transmitter Output pin. It

contains an 8-bit THR, a 12-bit TSR and a 16 byte FIFO. For data transmission, FIFO and THR communicate with together. The framing happens in the TSR and transmitted out through transmitter output.

3. Proposed Methodology

Serial protocol is the most significant communication protocol which is widely utilizing in industrial sector for several measurement equipments. Such that "Universal asynchronous receiver transformer" (UART) is a serial communication module which is specifically implemented in microcontroller and embedded devices to exchange the data among the terminals. The significant characteristic of this transmitter is to transfer and receive the data in particular data-format in a sequential order.
In this section have mainly discussing about proposed system design aspects (i.e. UART) module.
The top-level module of proposed UART design is described as follows.

A. Top-Level Module of Proposed UART

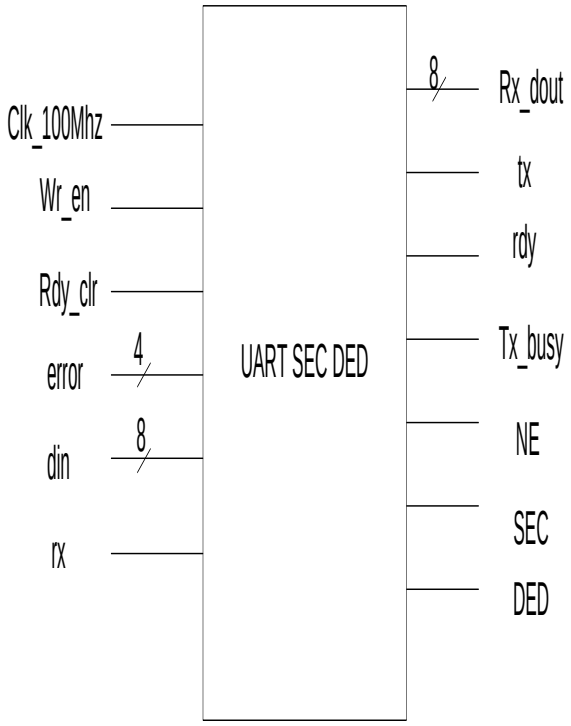

Fig. 5: "UART" Top Model

The above figure:5 depicts the top-level module of UART design which contains relevant input and output parameters. As already state that, significant role of UART module is to transmit and receives the data signals in serial order at defined baud-rate. The system takes the eightbits binary input data (din) and results the serial output ports also system takes the serial-data (i.e. rx) and generates the eightbits parallel data interms of dout-signals. The brief description about all input and output signals are given in the following table-2.

Table 2: Description of Input & Output Signals.

Signal name	Description
Clk_100 Mhz	External clock signal with 1000Mhz clock frequency.
Wr_en	External-control signal enables writing to the transmitter buffer
rdy_clr	External control signal to clear the previous data from receiver memory
Error	A 4-bit signal which represents the error in the channel.
Din	8-bit parallel input data, is to be forward sequentially.
Tx	Single-bit output port which transmits single-bit data
Rx	Onebit input port which receives single-bit data
Rx_dout	8-bit output-port which holds the received data parallelly
Rdy	A status signal is to ready for data reception.
Tx_busy	A status-signal which shows busyness of the TX module.
NE	indicates that received data signal contains no error (NE)
SEC	Single-bit status signal represents that single-bit error is corrected (SEC)
DED	Double Error detection (DED) indicates that presence of double errors in the received signals.

B. Proposed UART Architecture with SEC_DEC Capabilities.

The detail architectural design of proposed UART module is represented in the following diagram (figure: 6). The typical architecture of proposed (UART) module integrated with five major blocks, each block performs their respective operations. Such major blocks are; 1) UART_Transmitter, 2) UART_Reciever, 3) Baud-Rate generator, 4) Hamming_Encoder (H_EN) and 5) Hamming_Decoder (H_DC).
The significant role of designed UART system is to forward and receives the data signals in sequential order, also corrects the single error and detects the double-errors in the receiver end.
The Transmitter module (**UART_Tx**) contains 8bits data inputs which send the input data signals serially via Tx port. Initially, the transmitter contains four states (i.e. Idle, Start, Data and Stop). The data transmission process begins with idle-state, during the receiving of Wr-en signals, data moves into start-state. During this process, the data signal is considered from din and waits for clk_en signal. Later, the data is forwards to data transfer state, where data-bits are forwarded serially. Finally, data bits are re-forwarded if the bits level reaches at 7 and enters into the stop state

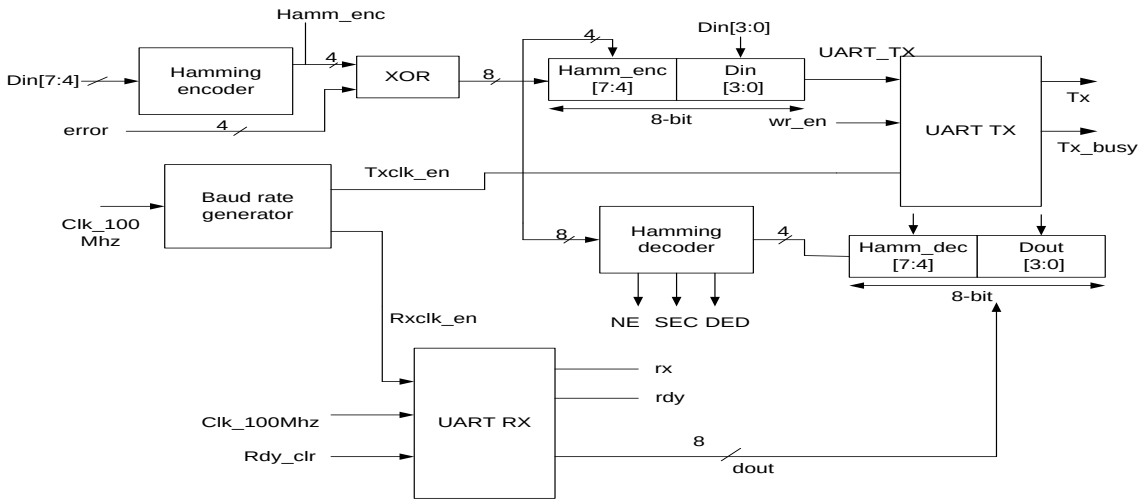

Fig. 6: Proposed "UART" architecture.

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The receiver module (**UART_Rx**) contains four input ports (Clk_100MHz, Clk_En, rdy_clr and rx). Through the Rx-port system receives the bits and stores in a shift register. The stored data bits are sent out in parallel order through the dout.

The baud-rate generator (BRG) responsible to generate the signal samples for the UART_Tx and UART_Tx modules. Internally, the BRG has a input port (Clk_100MHz) with two output ports (i.e. TxClk-en and Rxclk-en). Additionally, the BRG exploits a mod-16 counter which generates the baud frequencies i.e. frequency range for UART_Tx is 100MHz/(115200 x 16) and for UART_Rx is 100MHz/115200.

The hamming encoder (H_EN) utilized in this design which takes the fourbits input data signals and encodes into eightbits coded data. This coded data is EXORed with fourbits error signals which are the input of this module. Later, these coded signals (i.e. eightbits hamming data) are concatenated with 4-bit din signal and create a frame and utilized as an input for UART_Tx module.

The hamming decoder (H_DC) is responsible to correct the single-errors and finds the double errors (i.e DDE). H_DC fed with H_EN which contains (7:4) bits of data and checks the errors in the encoded data and corrects the single errors.

4. System Implementation

The following section discusses about proposed work implementation detail i.e. proposed UART-SEC-DED module which is designed using Xilinx of version 14.7, and implementation design has been performed on Artix-7 FPGA board. The obtained simulation outcomes and its detail explanation are given below.

Results of Top level Module of UART-SEC-DED

The top-level module design of proposed UART feature is shown in fig: 7.

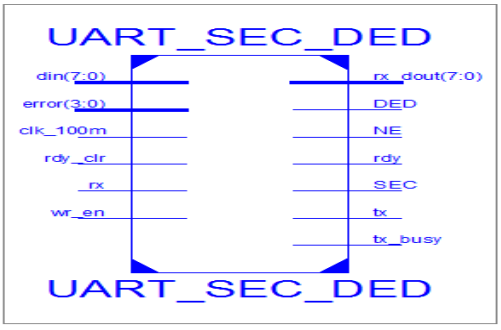

Fig. 7: Top-level module of proposed UART-SEC-DED

Generally, it contains 8bits din, 4bit error-signal, onebit control signal-receive, rdy-clr and write-enable input parameters. And outputs are the eight bit dout signal, single-bit no error signal, single-bit single-error correction, single-bit transmit signal, ready signal and transmit ready signal.

The simulation waveform results of top level module of proposed UART design is given in figure:8 (a), (b) and (c) which describes the 3-different cases i.e. (a) displays the waveform results when UART receiver module represents NE (no error) data received.(b) displays the simulation results of single error corrected for UART module and (c) shows the waveform results of double errors occurring in transmitted signals.

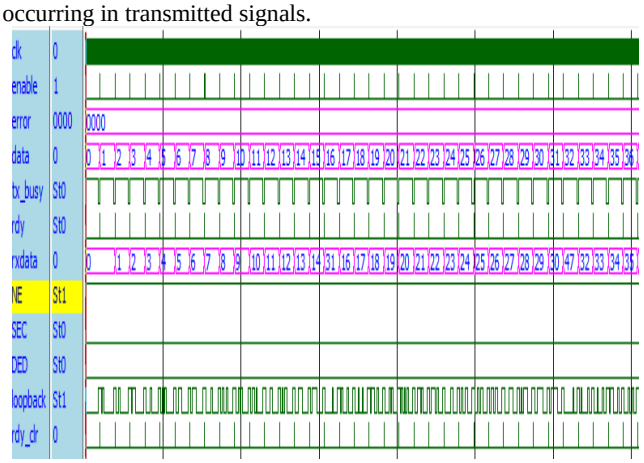

Fig. 8.(a): No Error Simulation results- UART-SEC-DED module

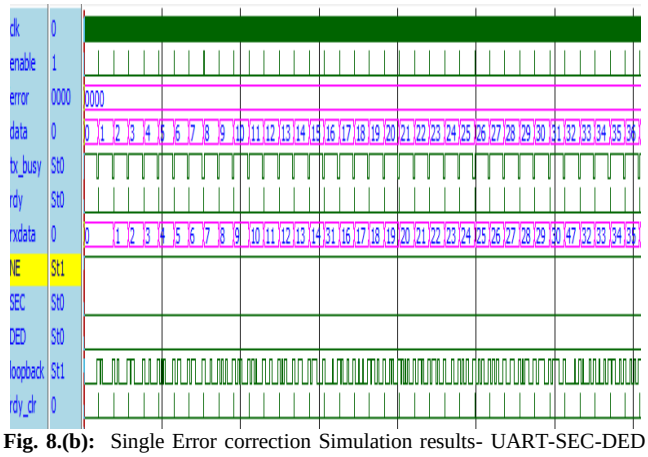

Fig. 8.(b): Single Error correction Simulation results- UART-SEC-DED module

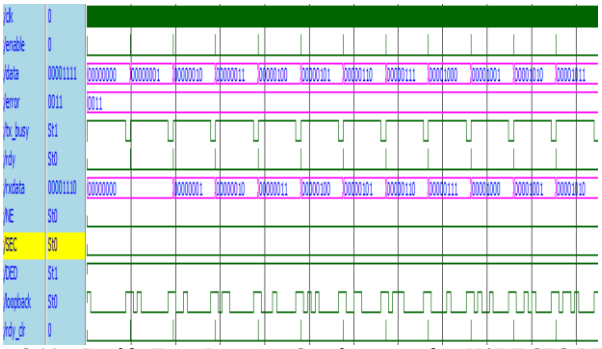

Fig. 8.(c): Double Error Detection Simulation results- UART-SEC-DED module

The transmitted signals are the sequence of eight bit binary number which starts from 00000001 to 0000 l lll. The waveform results 5. (b) represents the received signal as '00000000 l' to '0000 l lll' that is the similar as transmitted signals. This represents that if we add a single bit error to transmit signal, the single bit error is updated by UART module. The single error correction signal remains higher as the updating is done continuously for series of transmitted signals. While in 5. (c) error signal '00 l l' indicates the double errors. This error signal is added with transmitted signal. The DED signal remains higher for complete simulation waveform and therefore the data signal generated from the receiver remains '0000'.

The snapshot of FPGA board design implementation and its testing is displayed in the below figure: 9. In this we are using hyper-terminal software which generating input char 'a', received outcome on LED = 'l l 0000 l'. The ASCII value of char 'a', 8`b l l 0000 l (97 decimal) is the result.

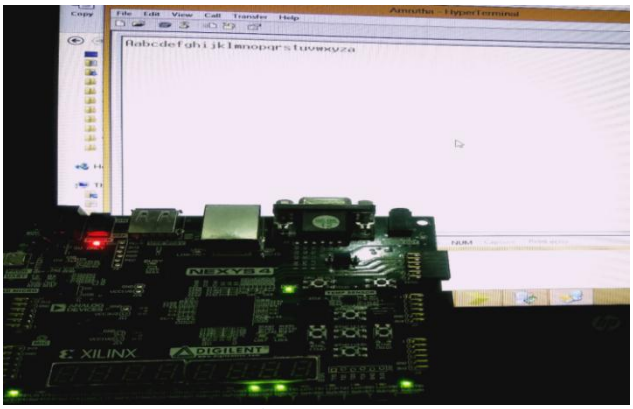

Fig. 9: An Hyper terminal software giving inputs and receives result on FPGA in LED's.

5. Conclusion

The Universal Asynchronous Receiver Transmitter (UART) is the very simple and significant sequential communication protocol which is essentially utilized for microcontroller systems. Lots of research studies were carried out by different researchers for enhancing the design of UART module with respect to detecting types of error like parity-error, overrun error, framing error as well as improvising ofbaud rate also. But those techniques have some drawbacks. Thus, to overcome those issues, the present study have introduced UART module which involves hamming encoder and decoder two essential components. The proposed module adding eight encoder and four decoder which able to detect the double errors during the transmission of data signals along with it able to corrects the single bit errors also. Thus, designed UART module named as UART-SEC-DED. The proposed UART-SEC-DED module was simulated and implemented on FPGA version 14.7. Finally, the experimental analysis was carried out by evaluating of single error correction and double error detection capability.

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