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Research paper

FPGA based least mean square algorithm for noise cancellation in communication system

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Abstract

We present modified Distributed Arithmetic (DA) based architecture for LMS Adaptive filter which has improved the throughput of the filter also area and power has been comparatively been reduced. As we know, the adaptive filter uses continuous recalculation and generation of new coefficients will generate the negative effect on the use of algorithm. We have used a special temporary LUT addressing technique has overcome the issues resulting in better performance and good results. In this paper, we have discussed about the adaptive filter and implementation of DA adaptive filter and also discussed the results obtained from the design. Comparison with traditional design has also been done to show the effectiveness of the algorithm.

Keywords: *Least Mean Square (LMS) Algorithm; Distributed Algorithm (DA); Adaptive Filter; Field Programmable Gate Array(FPGA); Throughput; Efficiency; Convergence Rate; Power Analysis; Look Up Table(LUT); Convergence Matrix; Interference Signal.*

1. Introduction

Array of reception apparatuses or sensors is broadly utilized as a part of numerous applications like correspondence, radar and so on. Points of interest of such frame-work are higher degrees of opportunity, excess, adaptability and so forth. In genuine the signs got by the cluster comprise of wanted flag as well as the obstructions from the sources in the encompassing condition, it is fundamental to expel the meddling sign and increment the Signal to Interference in addition to Noise Ratio (SINR) of the coveted flag... Obstruction corrupts the execution of the framework and diminishes the recognition and estimation of the coveted flag in the got flag. Slightest Mean Squares (LMS) calculations depends on figuring of minimum mean square of the flag having mistake and the real flag. At the end of the day, we can state it is the distinction of real flag and they got flag.

As the name suggests adaptive means keeps on changing. The filter is designed in such a way that it's coefficient are continuously changing due to the feedback system into the filter to re-move the noise from the output signal till the time is minimum. The filter keeps on updating the feeding the generated noise error to the feedback till the total system output power, updating the weighting coefficients as the need arises. The advantage of this system is that it works well in non- stationary conditions, i .e. when the relative difference in the characteristics of the RFI in the primary and reference channels change with time.

Interference is the kind of time-varying, unknown signal. This characteristic requires the filter can automatically track the changes of signals, and respond to the changes by adjusting the weight coefficient quickly. What is more, this just fits well with the functions of the adaptive filter. Thus, the adaptive filter is what to be chosen for the interference cancellation. The principle of adaptive filtering interference cancellation is shown in Figure 1

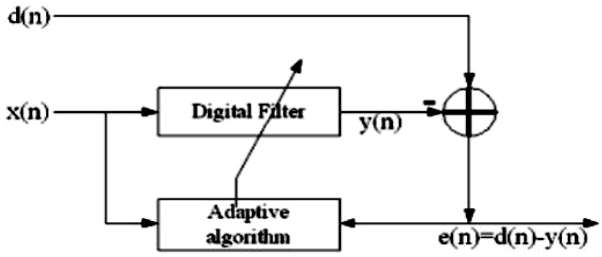

Fig. 1: Block Diagram of Adaptive Filter.

Where x(n) is the input signal to a digital filter y(n) is the corresponding output signal d(n) is an additional input signal to the adaptive filter e(n) is the error signal that denotes the difference between d(n) and y(n). The adaptive canceller will not distort the spectrum of the astronomical signal, yet it will provide a high degree of interference attenuation. Noise injected by the reference channel can be minimized if and a large number of filter taps are used. The higher the interference to noise in the reference channel relive to that in the Primary channel, the lower there residual noise in the system

LMS Algorithm

The primary highlights that pulled in the utilization of the LMS calculation are low computational many-sided quality, confirmation of joining in stationary condition, fair union in the intend to the Wiener arrangement, and stable conduct when executed with limited exactness math. The meeting investigation of the LMS displayed here uses the freedom supposition.

Derived the optimal solution for the parameters of the adaptive filter implemented Through a linear combiner, which corresponds to the

case of multiple input signals this solution leads to the estimation of the reference signal d(k) using minimum mean square error. If good estimates of matrix, denoted by ˆ R (k), and of vector p, denoted by ˆ p (k), are available, a steepest-descent-based algorithm can be used to search the Wiener solution as follows:

$$W(k+1) = w(k) - \mu \hat{} gw(k)$$

$$= w(k) + 2\mu(\hat{} p(k) - \hat{} R(k)\, w(k)) \quad (3.1)$$

For k =zero, 1, 2... Where ˆgw (k) is an estimate of the gradient vector for the filter coefficients with respect to objective function.
Convergence and Stability of the LMS algorithm
The LMS algorithm initiated with some arbitrary value for the weight vector is seen to Converge and stay stable for $0 < \mu < 1/\lambda$ max (3.3)

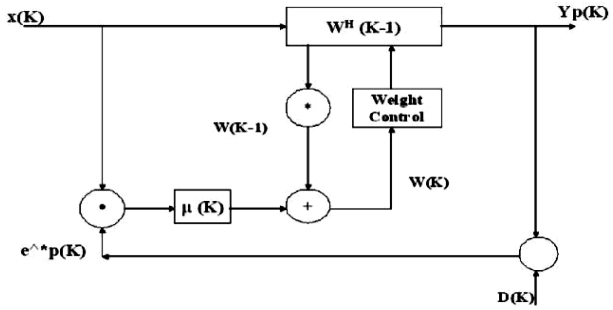

Fig. 2: Block Diagram of LMS Algorithm.

Where λ max is used to represent the correlation matrix R comprising of highest Eigen values. As we probably am aware for count of joining of information we have to take the corresponding converse of the relationship network R that has Eigen esteems. At the point when the Eigen estimations of R are far reaching, union might be moderate. The Eigen esteem spread of the relationship grid is evaluated by figuring the proportion of the biggest Eigen incentive to the littlest Eigen estimation of the net-work. If μ is chosen to be very small then the algorithm converges very slowly. It is a very obvious fact that if we increase the value of μ it will definitely increase the convergence rate however it will lead the system to be less stable at the minimum value.

2. Proposed system

The DA implementation of an adaptive filter mainly consists of shift registers; Arithmetic table like LUT's and special addressing LUT's, scalable accumulator including add or subtract unit and registers. When DA algorithm is directly used to implement adaptive filter, the complicated calculation operation of multiplication-accumulation is replaced with shifting and adding operation. To achieve best configuration in terms of changing coefficient of adaptive filter, the special addressing scheme and the temporary LUT's are used, the DA algorithm not only optimizes but also improves performance of the system.
The generalized block diagram of the DA based system is shown in the figure 3. The basic architecture of DA mainly consist of n-bit shift register, look up tables comprising of partial products of the design coefficients and adder and subtract unit to perform the necessary action at the output stage. This architecture reduces hardware to a very great extent and hence used in most of the filtering operations for the optimization of the hardware and in-crease of throughput.

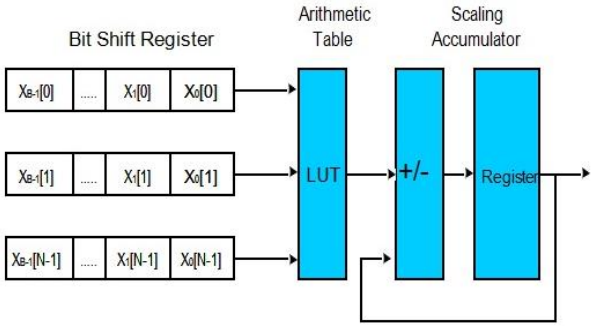

Fig. 3: Block Diagram for DA Based System.

Here, we propose reconfigurable DA-based adaptive filter on FPGA implementation. As we know registers are scarce resource in FPGA since each LUT in many FPGA devices contains only two bits of registers. Therefore, the LUTs are required to be Implemented by distributed RAM (DRAM) for FPGA implementation. These LUTs are used to store the values of partial products generated during the multiplication of weights and input signal. A special temporary LUT is used to store the values of the weights to be used for generating the partial products. Further these partial products are feed to add or subtract unit to do the further processing of signal. This process helps is fast calculation and improves the throughput of the design.

3. Results and analysis

The whole architecture of the LMS has been built on Xilinx platform using verilog language. The design is developed and coded to obtain various results such as design summary and simulation results as discussed below. It has been observed that the architecture has a very good performance over the other traditional architecture in terms of reduced area and timing configuration. Below shows the design summary obtained on Xilinx ISE 14.1 based on Atrix 7 series of FPGA from Xilinx.

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	932	3584	26%
Number of Slice Flip Flops	987	7168	13%
Number of 4 input LUTs	1402	7168	19%
Number of bonded IOBs	67	141	47%
Number of MULT18X18s	10	16	62%
Number of GCLKs	1	8	12%

Fig. 4: Design Summary for LMS.

It can be clearly observed from the above figure the device utilization is only 26% of the slices giving opportunity to the other design to be implemented on the FPGA. Also the minimizing the area has caused reduction in static power of the design. The timing report of the system shows an great improvement in the frequency of the design with operating frequency of 136MHz. Figure 4 shows the top level RTL Schematic obtained from the code after synthesis. It can be seen that the module has two set of input one desired signal tremed as din and the other actual signal termed as xin. We do have other synchronizing signals such as adapt enable signal that initiates the feedback loop and helps the design to enter in error correction mode to minimize the error. The processed output can be observed on you and the generated error signal can been seen on error out signal available on the module.

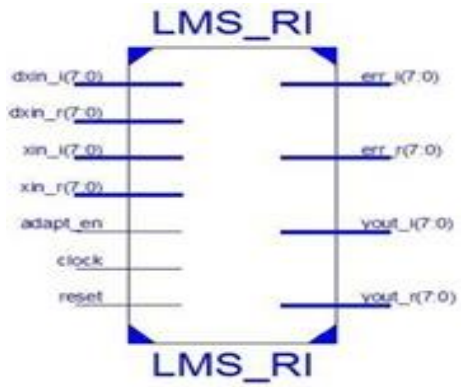

Fig. 5: Top Level RTL Schematic.

The design has been simulated using modelsim simulator. The test bench has been written to fed the continuous signal to the design. A text file with sine wave as one input and a noisy signal is generated in MATLAB to feed as an input to the design and check the corresponding output as shown in figure 5.

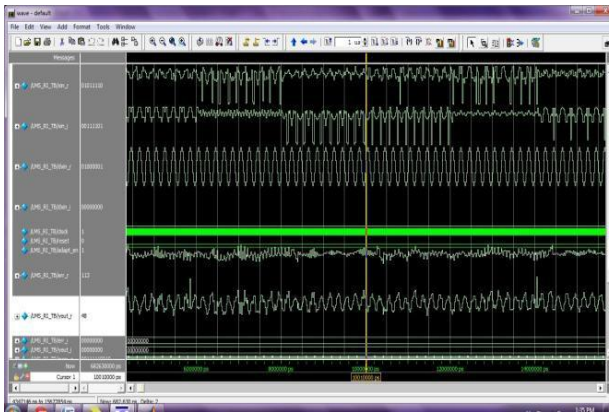

Fig. 6: Simulation Results for LMS Algorithm.

4. Conclusion

In this paper, the proposed scheme for high-throughput DA-based implementation of adaptive filter based on LMS algorithm that is successfully developed and implemented in FPGA. It is shown that hardware cost could be substantially reduced by sharing the same registers by the DA units for different bit slices. The pro-posed structure of filter for FPGA implementation supports up to 163 MHz input sampling frequency and compared to convention design. it is also observed that the proposed system is better in terms of speed and area (slices).

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