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Research paper

Genetic algorithm based 15 level multilevel inverter with SHE PWM

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Abstract

This research paper describes Selective Harmonic Eliminating Pulse Width Modulation (SHEPWM) amalgamated Genetic Algorithm (GA) based asymmetrical Multi Level Inverter (MLI) (15 Level) investigated by using Field Programmable Gate Array (FPGA) for single phase inverter. Multilevel inverter (MLI) have been frequently used in industry particularly to get superior quality output voltage in terms of Total Harmonic Distortion (THD).In SHE PWM equations are capable of determining the required band of switching angles to eliminate desired value of harmonics. GA algorithms playing with band of switching angles randomly to find out best solution for the MLI. Linear feedback shift register (LFSR) has been used to find the random selection of particular switching angles from the band of switching angles. Hence, the proposed method does the capable of eliminating a huge number of specific harmonics and the output voltage results in a minimum THD value. The simulation results show that the proposed method successfully attains the global solution faster than other algorithms. The de-tailed spectrum and FPGA results are presented.

Keywords: *Genetic Algorithm; Selective Harmonic Elimination; Pulse Width Modulation; Multilevel Inverter; Field Programmable Gate Array; Linear Feedback Shift Register; Total Harmonic Distortion.*

1. Introduction

In recent years, power electronic devices have been broadly served in many industrial applications due to the impact of load harmonics, which are aiding to produce overheat of the magnetic cores of transformer and motors. Inverters are playing major roles in power electronics for power conversion [1]-[2]. Multilevel inverter (MLI) is one of the power conversion devices having stepped output voltage which is used to reduce the magnitude of load harmonics. With increasing of demanded power in industry, MLI has been used as an alternative to traditional two level inverter. Multilevel inverters have been enticing attention for their high efficiency, high voltage capability, low electromagnetic interference and it can operate in low switching frequency. Various circuit arrangements have been proposed over the years. From the circuit configurations of the MLIs, It can be broadly classified into four major categories 1.Contour of the usage of the passive and active devices 2. H-Bridge 3.contour of the number levels 4. Based on the switching angle optimization algorithms used 5.Based on the DC Sources.

In the first category, it can be further categorized as 1.Diode Clamped MLI (DC-MLI), 2.Flying capacitor MLI. In these MLIs are required extra clamping diodes and capacitors.

H bridge inverter can be categories based on the number of voltage sources connected to one H-Bridge, and the more number of single H-Bridge with single source connected in series. The later one calls it as cascaded MLI. In the cascaded MLI, the number switches will be more for delivering a multilevel output compare with first one which is having a single H-Bridge connected to the multiple sources are having less number of switches especially which are having different dc sources (Asymmetric).

Based on the number of levels, it can be divided into any odd number of levels. The odd number of levels avoids the abrupt transition from positive to negative levels and also aids to avoid the shoot through fault between switches. But, if the number of levels are increasing beyond the certain limit for achieving less THD then more number of switching devices forced to be used which turns to increase the cost of the entire system and reduce the efficiency of the system. So, there is a tradeoff between number of levels achieving and the number of switches used playing a major role.

Predicated on the poor arrangement of the switching angle in the MLI, the system will engender more THD. In order to get lowest THD, the switching angle arrangement is eminent. Selective Harmonic Elimination (SHE) PWM methodology is the widely used switching strategy to unambiguously eliminate the selected harmonics from the output waveform of the inverter. The optimized switching angles are calculated by cracking transcendental equation based Newton Raphson method. But the real time implementation of such transcendental equations are having some drawbacks such as swallow too much execution time, requirement of more memories, require defining initial values and also provides no optimum solution. The selection of best switching angle can be chosen by using any kind of optimization algorithms. Genetic algorithm (GA) technique is used for eliminating some higher order harmonics while preserving the necessary fundamental voltage [3]-[4]. GA is a computational approach to solve optimization problems using genetic methods and the theory of evolution. But for the accomplishment of this method, proper selection of a few parameters such as initial population size, crossover operation,

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mutation operation etc. are required; thereby implementation of this algorithm becomes mind-numbing for higher level MLIs.
The bands of optimized switching angles are calculated by solving these equations in offline for various levels is the best solution to avoid the above said drawbacks of NR method. And these bands of switching angles are the deciding factors for the initial population sizes of the GA methods.
Linear feedback shift register (LFSR) involved pseudo random binary sequence is the best method to select the random values from the set of variables [5]-[7]. The mutation operation is possible among the GA population by using this kind of LFSR for producing the new generation. In this article, 15 level asymmetrical MLI consists of single phase H-bridge inverters connected with three different DC sources by using the hybrid of NR method with GA optimization is designed. Field programmable Gate Arrays (FPGAs) have turned out to be one of the foremost admired accomplishment media for digital circuits, and their introduction in 1984. The key to success of FPGAs is their programmability in nature which allows whichever circuit to be instantly self-possessed out by appropriate programming [8]-[11].

2. Proposed method

The block diagram of the proposed method consists of three modules namely Transcendental Equation solver, GA Based Search Algorithm, 15 level MLI as shown in Fig1.

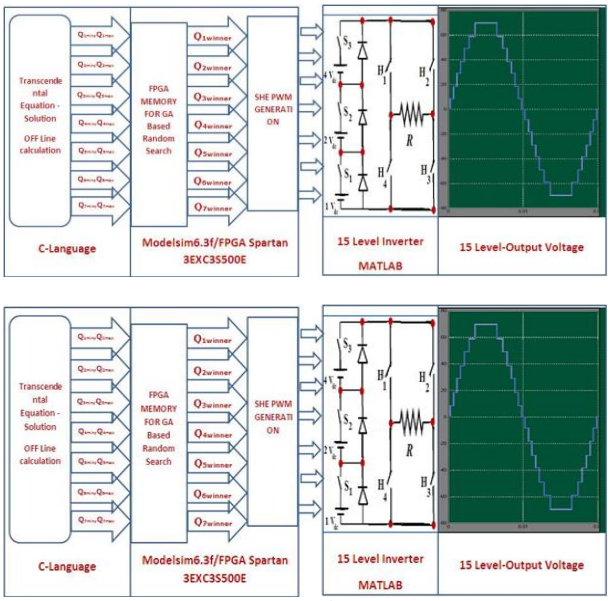

Fig. 1: Block Diagram of Proposed Scheme.

3. Transcendental equation solved for selective harmonic elimination

The harmonic content of output voltage will be the conclusive factor of an Inverter's performance, with whichever switching strategy, is commonly acknowledged.
For a multilevel inverter, switching angles at fundamental frequency are obtained by solving selective harmonic elimination equations in such a way that the fundamental voltage is obtained as preferred and specific lower order harmonics are eliminated. The advantages of SHE PWM over conventional carrier based PWM which are given below:

- For a chosen inverter switching frequency, the foremost uneliminated harmonic frequency is almost twice that of the switching frequency, thus resulting in a far superior pole switching waveform harmonic spectrum.
- A much superior pole switching waveform fundamental amplitude is achievable before the lowest amount pulse-width limit of the inverter is reached.
- The switching frequency of the inverter can be diminished up to 50 % when compared with the conventional carrier modulated sine PWM scheme.
- Higher voltage gain due to over modulation is possible and hence contributes to the better utilization of power conversion development.
- The DC link current is also small while considering the high quality of the output current and voltage. Hence the size of the DC link filter components is minimized.
- The switching losses of the inverter can be reduced due to the reduction in switching frequency.
- The use of precalculated optimized PWM program, switching patterns eliminate on line computations and provides simple implementation of a high performance technique.
- The proposed method MLI switching angles are shown Fig 1, should fulfill the two constraints,

Constraint 1.

$$\theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 < \theta_6 < \theta_7 < \frac{\pi}{2}$$

Constraint 2.
SHE based corresponding transcendental equations are

$$h_1 = \frac{4V_{dc}}{3\pi}[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) + \cos(\theta_6) + \cos(\theta_7)] = V_1$$
$$h_3 = \frac{4V_{dc}}{3\pi}[\cos(3\theta_1) + \cos(3\theta_2) + \cos(3\theta_3) + \cos(3\theta_4) + \cos(3\theta_5) + \cos(3\theta_6) + \cos(3\theta_7)] = 0$$
$$h_5 = \frac{4V_{dc}}{15\pi}[\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) + \cos(5\theta_6) + \cos(5\theta_7)] = 0$$
$$h_7 = \frac{4V_{dc}}{21\pi}[\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) + \cos(7\theta_6) + \cos(7\theta_7)] = 0$$
$$h_9 = \frac{4V_{dc}}{27\pi}[\cos(9\theta_1) + \cos(9\theta_2) + \cos(9\theta_3) + \cos(9\theta_4) + \cos(9\theta_5) + \cos(9\theta_6) + \cos(9\theta_7)] = 0$$
$$h_{11} = \frac{4V_{dc}}{33\pi}[\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) + \cos(11\theta_6) + \cos(11\theta_7)] = 0$$
$$h_{13} = \frac{4V_{dc}}{39\pi}[\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) + \cos(13\theta_6) + \cos(13\theta_7)] = 0$$

The fundamental voltage and the maximum obtainable voltage depend on the modulation index. Modulation index ma is defined as the ratio of the fundamental output voltage V1 to the maximum obtainable voltage V1max. If all the switching angles are zero then the output voltage would be maximum. V1max=4Vdc/3π. The expression for ma is therefore,

$$m_a = \frac{\pi V_1}{4sV_{dc}}$$

Where s is the number of switching angles which also equals to the number of DC sources if it is symmetrical MLI. In this proposed unsymmetrical method,

$$s = 2^n - 1$$

Where n is the number of dc sources. In this research 3 dc unsymmetrical sources are being considered. So the number of levels is equal to 15. Fig. 2 describes the pictorial representation of 15 level MLI switching angles. In this method SHE based transcendental equations are solved by C language by off line shown in Fig. 3. And resultant band of switching angles are stored in memory. These switching angles are the input of GA based search algorithms.

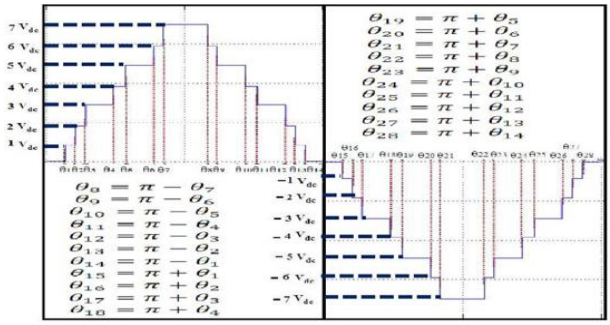

Fig. 2: Switching Angles for the 15 Level MLI.

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C Language Programme to find the band of switching angles
for(q1=4;q1<15;q1+=0.1){
for(q2=q1;q2<20;q2+=0.1){
for(q3=q2;q3<27.5;q3+=0.1){
for(q4=q3;q4<44.6;q4+=0.1){
for(q5=q4;q5<55;q5+=0.1){
for(q6=q5;q6<70;q6+=0.1){
for(q7=q6;q7<85;q7+=0.1){
y=cos(q1)+cos(q2)+cos(q3)+cos(q4)+cos(q5)+cos(q6)+cos(q7);
y1=cos(3*q1)+cos(3*q2)+cos(3*q3)+cos(3*q4)+cos(3*q5)+cos(3*q6)+cos(3*q7);
y2=cos(5*q1)+cos(5*q2)+cos(5*q3)+cos(5*q4)+cos(5*q5)+cos(5*q6)+cos(5*q7);
y3=cos(7*q1)+cos(7*q2)+cos(7*q3)+cos(7*q4)+cos(7*q5)+cos(7*q6)+cos(7*q7);
y4=cos(9*q1)+cos(9*q2)+cos(9*q3)+cos(9*q4)+cos(9*q5)+cos(9*q6)+cos(9*q7);
y5=cos(11*q1)+cos(11*q2)+cos(11*q3)+cos(11*q4)+cos(11*q5)+cos(11*q6)+cos(11*q7);
y6=cos(13*q1)+cos(13*q2)+cos(13*q3)+cos(13*q4)+cos(13*q5)+cos(13*q6)+cos(13*q7);
if (((y>-((mo*4)-0.5)) && (y<=((mo*4)+0.5)))&& (y3>=-0.5 && y3<=0.5) && (y2>=-0.5 && y2<=0.5)
&& (y1>=-0.5)&&(y1<=0.5)&& (y4>=-0.5)&&(y4<=0.5)&& (y5>=-0.5)&&(y5<=0.5)&& (y6>=-
0.5)&&(y6<=0.5)){
myfile<<q1<<" "<<q2<<" "<<q3<<" "<<q4<<" "<<q5<<" "<<q6<<" "<<q7<<" "<<y<<" "<<y1<<"
```

Fig. 3: C Language Program for Selecting Band of Switching Angles.

4. Operation and design of 15 level multilevel inverter

This section explains the 15 level multilevel inverter operations. Seven switches have been used for the conversion. Any cascaded multilevel inverter can be categorized into 2 groups based on the usage of switches.

In the asymmetrical 15 level MLI shown in Fig.4.switches S1,S2,S3 conducts for both positive and negative half cycles, whereas switches H1,H3 are switching for positive half cycle and H2,H4 for negative half cycle. The switching patterns are shown in Table 1

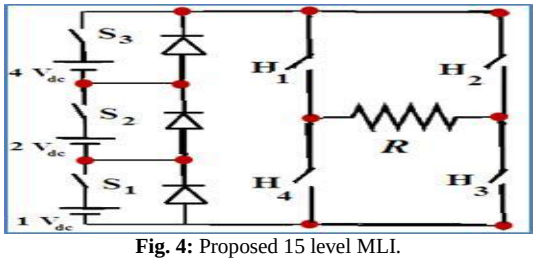


Fig. 4: Proposed 15 level MLI.

Table 1: Switching Pattern

Levels	S1	S2	S3	H1	H2	H3	H4	Output Voltage
1	√	×	×	√	×	√	×	1 Vdc
2	×	√	×	√	×	√	×	2 Vdc
3	√	√	×	√	×	√	×	3 Vdc
4	×	×	√	√	×	√	×	4 Vdc
5	√	×	√	√	×	√	×	5 Vdc
6	×	√	√	√	×	√	×	6 Vdc
7	√	√	√	√	×	√	×	7 Vdc
8	×	×	×	√	×	√	×	0 Vdc
9	√	×	×	×	√	×	√	-1 Vdc
10	×	√	×	×	√	×	√	-2 Vdc
11	√	√	×	×	√	×	√	-3 Vdc
12	×	×	√	×	√	×	√	-4 Vdc
13	√	×	√	×	√	×	√	-5 Vdc
14	×	√	√	×	√	×	√	-6 Vdc
15	√	√	√	×	√	×	√	-7 Vdc

The DC sources are Vdc (10 Volts), 2 Vdc(20 Volts) and 4 Vdc(40 Volts) which are illustrated in Figure 4. The structure avoids the use of extra clamping diodes and voltage clamping capacitors. VR->Voltage across load resister.

Level 1: The switch S1 is alone ON and S2 and S3 are OFF->VR= ±10 Volts.

Level 2: The switch S2 is alone ON and S1 and S3 are OFF->VR=±20 Volt.

Level 3: The switches S1 and S2 are ON and switch S3 is OFF-> VR =±30 Volt.

Level 4: The switch S3 is alone ON and switches S1 and S2 is OFF-> VR =±40 Volt.

Level 5: The switches S1 and S3 are ON and switch S2 is OFF-> VR =±50 Volt.

Level 6: The switches S2 and S3 are ON and switch S1 is OFF-> VR =±60 Volt.

Level 7: The switches S1, S2 and S3 are ON -> VR =±70 Volt.

Level 8: The switches S1, S2 and S3 are OFF -> VR =0 Volt.

During Positive half cycle, the switches H1, H3 are ON and H2, H4 are off.

During Negative half cycle, the switches H2, H4 are ON and H1, H3 are OFF. The current flow for all the levels are shown in Fig. 5.

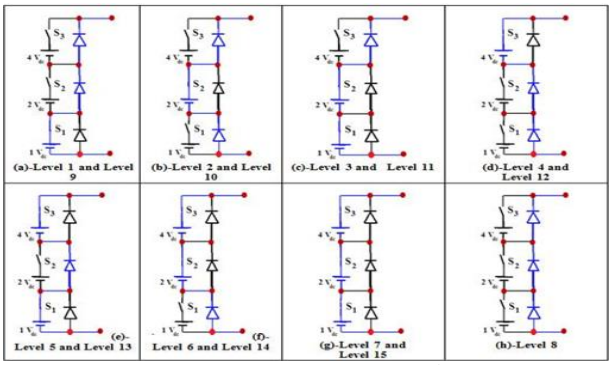


Fig. 5: Current Flow in All Levels of MLI.

5. Genetic algorithm implementation

Genetic Algorithm (GA) is a search-based optimization technique based on the principles of Genetics and Natural Selection. It is regularly used to find optimal or near-optimal solutions to tricky problems which would otherwise take an era to resolve. In methodology near-optimal solutions are derived by offline and these near optimal solutions are key elements to get best optimal solutions.

Population − It is a subgroup of all the feasible solutions to a given obstacle. The population for a GA is analogous to the population for human beings except that instead of human beings, we have Candidate Solutions depicting human beings. All the feasible switching angles are population here.

Chromosomes − A chromosome is one such solution to the given problem. A set of switching angles for one cycle is mimic of the chromosomes.

Gene − A gene is one element position of a chromosome. Position of particular switching angle is a copycat of gene.

Allele − It is that value a gene takes for an especial chromosome. Switching angle for one level is a mimic of Allele.

Fitness Function – It is a function which takes the solution as input and produces the suitability of the solution as the output. In some cases, the value of fitness function and objective function may be the same, while in others it might be dissimilar based on the problem. The THD is one of the performance parameters for any inverter. THD is an imitator of fitness function.

Genetic Operators – The operators which alter the genetic composition of the children includes crossover, mutation, selection, etc.

The generalized flow of GA and how are them used for MLI is shown in Fig 6.

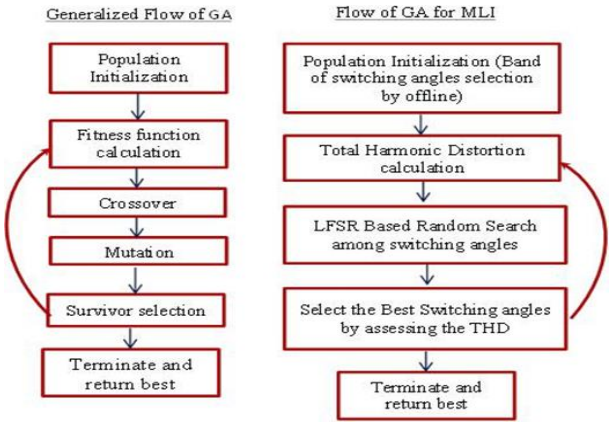


Fig. 6: Flow Chart of GA for Proposed Method.

6. Simulation results and discussions

The Proposed scheme has been simulated by using Co-simulation methodology. Two softwares have been used for Co-simulation process. 1. Modelsim6.3f for GA implementation and switching pulse generation, 2. MATLAB for 15 level MLI. The EDA (Electronic Design Automation) language VHDL has been used for the GA implementation and PWM generation.

6.1. GA implementation in FPGA

The FPGA design of GA Implementation is comprises of 3 modules shown in Fig 7.
The modules are

1) 50 Hz clock Generation.
2) One MHz clock generation.
3) GA algorithm switching gate pulse generation.

Clock divider principle has been used to generate 50 Hz clock from the FPGA board source clock of 50 MHz. FPGA XC3S500E devices has been used for this implementation.
The bands of switching angles are shown in Fig. 7.

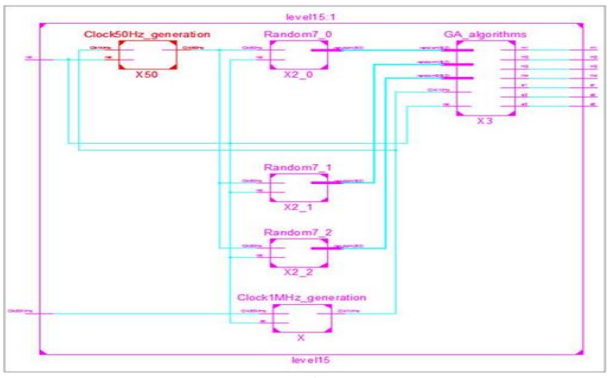
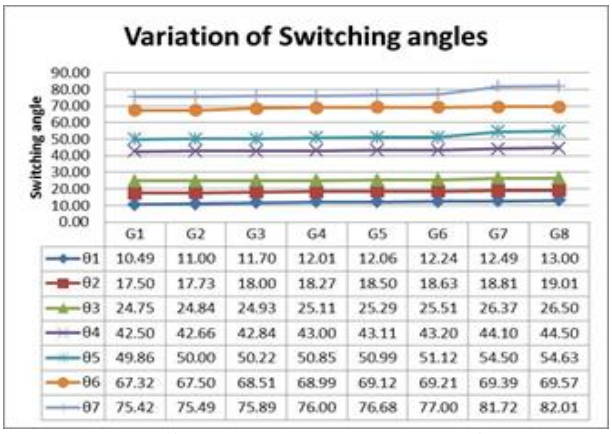


Fig. 7: FPGA Design of GA Implementation.

Module 2 called 1 MHz clock generation, which used to generate exact number of 1 MHz clock pulses required for each switching period.
Module 3 GA Implementation by using LFSR.



	G1	G2	G3	G4	G5	G6	G7	G8
θ1	10.49	11.00	11.70	12.01	12.06	12.24	12.49	13.00
θ2	17.50	17.73	18.00	18.27	18.50	18.63	18.81	19.01
θ3	24.75	24.84	24.93	25.11	25.29	25.51	26.37	26.50
θ4	42.50	42.66	42.84	43.00	43.11	43.20	44.10	44.50
θ5	49.86	50.00	50.22	50.85	50.99	51.12	54.50	54.63
θ6	67.32	67.50	68.51	68.99	69.12	69.21	69.39	69.57
θ7	75.42	75.49	75.89	76.00	76.68	77.00	81.72	82.01

Fig. 8: Band of Switching Angles (Combination of GENES).

The seven set of switching angles (Chromosomes) has been received by offline (θmin and θmax). Each set contains 8 possible angles (GENES). The variation of switching angles for θ1 from 10.49° to 13.00° and the variation of switching angle for θ7 from 75.42° to 82.01°. The cross and mutation among the genes or random search among the switching angles is performed by using LFSR and multiplexers combination which is shown in Fig 9.

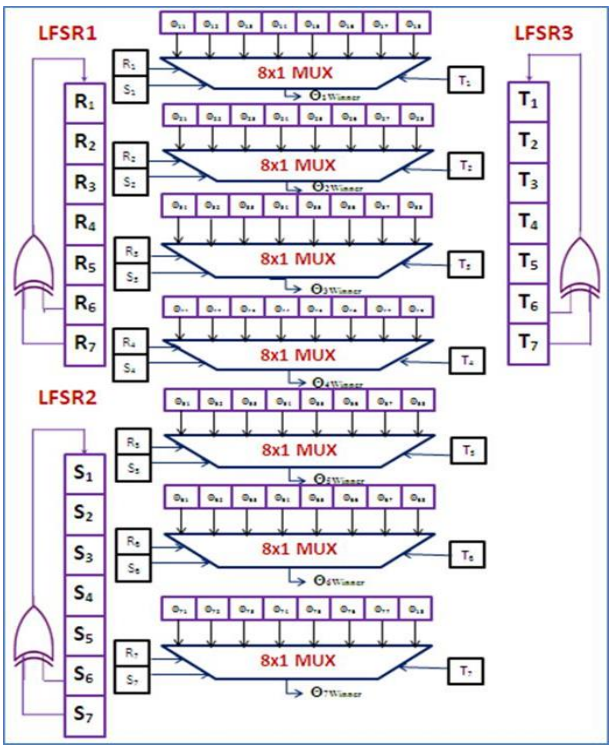


Fig. 9: Random Search for Gas.

Three LFSRs has been used to generate three random bits. These three random bits act as a selector line of the 8x1 multiplexers. 7 multiplexers are used to generate 7 switching angle for the 15 level MLI.

6.2. Simulation results

VHDL language has been used to implement entire digital design PWM pulse generation.

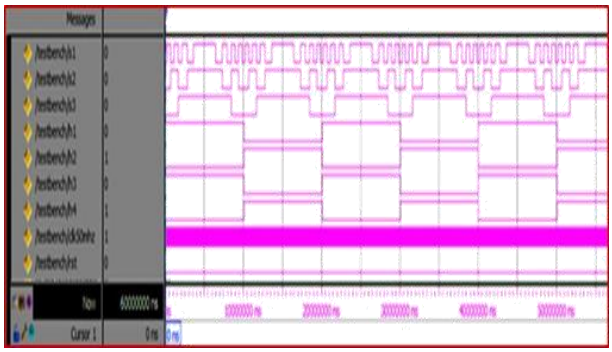


Fig. 10: Shows Simulation Results of All the Switching Pulses.

From Fig.10 Switch S1, 14 times transition from its state (number of ON and OFF per cycle), whereas S2 and S3 are 6 and 2 respectively. The inversion switches H1, H2, H3 and H4 gets transition its state only one during one cycle. From the above discussions, in this MLI scheme, the switching loss will be less since frequency of switching is less compared to standard Sinusoidal Pulse Width modulation.

The Fast Fourier Transform (FFT) analysis done by using MATLAB is shown in Fig 11. Standard R load has been used for analysis. The Final Switching angles derived from the GA algorithms are θ1=3.9°, θ2=12°, θ3=20.2°, θ4=29.0°, θ5=38.5°, θ6=49.6°, θ7=64.2° .The resultant THD will be 5.65%.

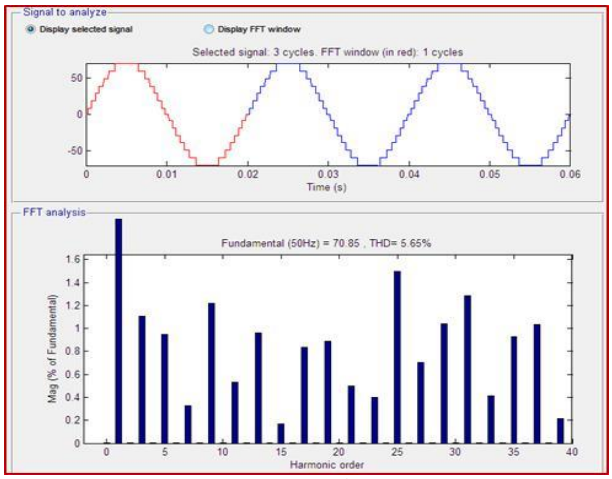


Fig. 11: FFT Analysis of 15 Level MLI.

7. Conclusion

The main objective of this research is to establish investigation on modern technique to solve Selective Harmonic Eliminating Pulse Width Modulation (SHEPWM) amalgamated Genetic Algorithm (GA) based asymmetrical Multi Level Inverter (MLI) (15 Level) with unequal dc sources by using FPGA for single phase inverter. The simulation is done by using co-simulation methodology. The detailed RTL design architectures are presented in section III. The results are shown in Fig 10 and Fig 11 are the evidence of this research, moreover the implementation this algorithm in FPGA occupies the less utilization (10 % of 4 input LOOK up table out of 9312).

References

[1] Mohammed H. Rashid, "Power Electronics", Prentice Hall of India Pvt. Ltd, 2nd Edition, 1994

[2] D. G. Holmes, T. A. LipoThomas.: (Pulse Width Modulation for-Power Converters), USA: IEEE Press, 2003.

[3] Albert Alexander.S," Development of High-Performance Solar Photovoltaic Inverter with Advanced Modulation Techniques to Im Prove Power Quality", International Journal of Electronics 104 (2017) 174-189.Electronics, vol. 10, No. 14, 2017, pp. 1993 – 2001.

[4] S. Albert Alexander and T. Manigandan, "Digital Switching Scheme for Cascaded Multilevel Inverters", *Proceedings of Third International Conference on Power Systems, Indian Institute of Technology, Kharagpur*, (2009) 1-6.

[5] Muthukumar P, Melba Mary P, Sankaragomathi B, "Assorted carrier-variable frequency-random PWM scheme for voltage source inverter", IET PowerElectronics, vol. 10, No. 14, 2017, pp. 1993 - 2001.

[6] Valantina Stephen, L. Padma Suresh and P.Muthukumar, "Field programmable gate array based RF-THI pulse width modulation control for three phase Inverter using matlab modelsim cosimulation",American Journal of Applied Sciences vol. 9,No.1"1,pp 1802-1812. 2012

[7] Jayamala V, Ramasamy S , Jeevananthan S, Investigation of Pseudorandom Carrier Pulse Width Modulation Technique for Induction Motor Drives. Proceedings of second International Conference on Current Trends in Technology EE22, NuCONE: 2011 pp. 1-5.

[8] B. Hariram, Dr. N. S. Marimuthu.: (*Evaluation of FPGA based speed control of induction motor*), Journal of Electrical Engineering, 2006.

[9] Teena Jacob ; Anjali Krishna ; L. Padma Suresh ; P. Muthukumar, "A choice of FPGA design for three phase sinusoidal pulse width modulation", International Conference on Emerging Technological Trends, 2016,DOI: 10.1109/ICETT.2016.