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Research paper

An area efficient approach on nonvolatile processors using pack architecture

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Abstract

Nonvolatile processor can hold its state when the power is off. The major drawback of the nonvolatile processor is the excess area occupied by the nonvolatile registers in it. Contrasted with consistent CMOS flip-flop, the ferro electric nonvolatile flip-flop takes a vast area because of its hybrid structure. Later nonvolatile processor with floating gate transistor was developed. But this structure also has a drawback that it occupies 40% of memory area. In this paper, Parallel Compare and Compress (PaCC) design architecture is utilized to reduce the area of the nonvolatile registers in the non-volatile processors. The fundamental blocks in PaCC design are PaCC encoder, PaCC decoder, volatile registers, nonvolatile registers and nonvolatile flip flop controllers. The PaCC encoder and the PaCC decoder are the works that are mainly focused in this paper. The PaCC design utilizes Run length encoder (RLE) technique. Run length encoder (RLE) is a simple technique used for compressing data. Here runs of data's are stored as a single data value and as count. The PaCC decoder decodes the outputs from the PaCC encoder, thus the original input data can be obtained. The results shows that this design architecture can reduce the number of nonvolatile registers by 70%-80%, thereby reducing the overall area. The design was modeled using VHDL in Xilinx ISE Design Suite 14.5 and simulated using Modelsim 6.5b.

Keywords: *Run Length Encoder; PACC Encoder; Parallel Compare and Compress Architecture; Non-Volatile Registers; VHDL; Xilinx ISE 14.5; Modalism 6.5b.*

1. Introduction

With the rising memory advances, nonvolatile processors are getting increasingly consideration. Contrasted and the volatile processors, the nonvolatile processors are fabricated with nonvolatile registers and have the accompanying favorable circumstances: I) zero-standby power: the processor can hold its state when not controlled, while the conventional ones experience the ill effects of the expanding spillage energy to keep information; II) moment on and off: the processor can continue its work inside a few cycles from the slowed down point, while the customary one needs a huge number of instating cycles; III) high flexibility to control disappointments: the processor can work dependably under the situations with recurrence control intrudes, for example, vitality collecting and remote fueled applications; IV) fine-grained control administration: the processor can be closed down at whatever point conceivable because of the ultra-low vitality and quick recouping qualities.

Ferroelectric arbitrary access memory (FeRAM) is an ease nonvolatile memory innovation manufactured with two extra veils to a standard CMOS innovation [5], which has been broadly utilized as a part of minimal effort and low power applications. These flip-flops are utilized as a part of a conveyed form and can keep up framework states with no power supply inconclusively. A productive controller is utilized to accomplish parallel peruses and keeps in touch with the flip-flops. A reconfigurable voltage location framework is intended for the programmed framework reinforcement amid control failures.The information exchange between an unstable processor and optional NV stockpiling cause repetition after some time .The PaCC engineering to diminish the quantity of the bits to be put away in the NVFFs, and henceforth the number and zone of NV registers. The design embraces a contrast and pack technique with enhance the pressure proportion. A pressure codec in view of a parallel run length encoding is utilized. A territory proficient two-arrange moving system is intended to limit the codecs zone, which lessens the region of the first barrel moving system. A configurable state table structure in PaCC to store the reference vectors utilized for examination. For particular application to figure the reference vector determination issue as an improvement issue and create heuristic calculations to fathom it.

2. Theory

Compression is an approach to lessen the quantity of bits in an edge however holding its importance .It diminishes space, time to transmit, and cost. It is a strategy to recognize repetition and to dispose of it. Information pressure is the craft of decreasing the quantity of bits expected to store or transmit information. At the point when information pressure is utilized as a part of an information transmission application, speed is the essential objective. Speed of transmission relies on the quantity of bits sent, the time required for the encoder to produce the coded message and the time required for the decoder to recoup the first outfit. In an information stockpiling application, the level of pressure is the essential concern .Various lossless information pressure calculations have been proposed and utilized. A portion of the fundamental

systems being used are the Huffman Coding, Run Length Encoding, Arithmetic Encoding and Dictionary Based Encoding.
Lossless information pressure is only the orginal information can be recreated precisely from packed information. Lossless pressure is for the most part utilized for applications that can't endure any distinction between the first and remade information. Content pressure is a vital region for lossless pressure. In lossless techniques, unique information and the information after pressure and decompression are precisely the same. Repetitive information is expelled in pressure and included amid decompression.
Lossy information pressure in which information after pressure and decompression are precisely the same. Lossy information pressure in which information after pressure and after that decompression recovers a document that isn't precisely as the orginal information as there will be loss of information. These strategies are less expensive, less time and space.

3. methodology

3.1. PACC architecture

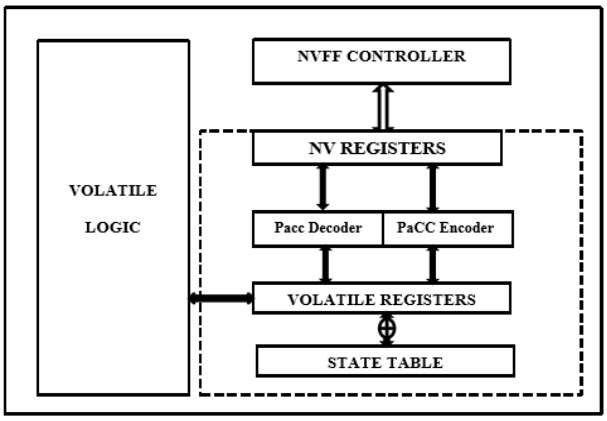

Fig. 1: Pacc Architecture.

The PaCC engineering comprises of volatile registers which stores the present framework state V, a state table, a pressure codec (separated into a PaCC encoder and a PaCC decoder), and a little arrangement of NV registers. The state table is utilized to store V_{ref} ; the pressure codec is utilized to make transformation amongst V_{diff} and V^{c}_{diff} ; and the correlation is finished by the bitwise XORs. In spite of the fact that the unpredictable registers, the state table, and pressure codec may build the territory, the critical lessening in the quantity of NV registers prompts a considerably littler general chip region. Pacc encoder in the Pacc engineering is the work that is for the most part engaged.

3.2. Block diagram

The fundamental square graph for the Parallel think about and pack encoder is as appeared in figure 2. Piece outline comprise of information end moving system, yield end moving system, Run Length Encoder, All 0/1 indicator square and length control. Two phase moving system comprise of Fixed N bit moving system and 2N bit barrel shifter. Settled N bit moving system is utilized to just move the contribution by N .This shifter is to a great degree territory effective and no multiplexor is required. The settled moving system is utilized to refresh the rest of the piece of the unstable registers. A Barrel shifter is an advanced circuit that can move an information word by a predefined number of bits in a single clock cycle .It can be executed as a grouping of multiplexers and in such a usage the yield of one mux is associated with the contribution of the following multiplexer .The information to be packed is moved by the barrel shifter.

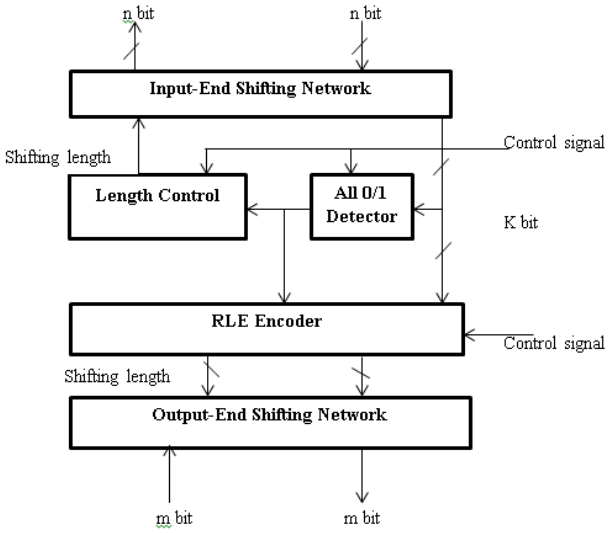

Fig. 2: Pacc Encoder.

1) Input-End Shifting System It shifts n-bit differential vector, Vdiff from the unstable registers to the RLE encoding module. The n-bit yield is the moved an incentive for refreshing the unpredictable registers.
2) Output-End Shifting Network The yield end moving system moves the m-bit pressure results to the NV registers.
3) All 0/1 Detector The every one of the 0/1 locator square executes k-bit parallel perception and produce a sidestep flag to the RLE encoder and length controller
4) Length Controller The length controller gives the moving length to the info end moving system as indicated by the sidestep motion and Observation window width k.
5) Run Length Encoder the RLE encoder packs the k-bit input serially when the sidestep flag is incapacitated, generally sidesteps the k-bit input. The arrangement of the pressure result depends on the limit, Lth. Once the RLE encoder achieves the pressure, it sends the q-bit packed section. Run length encoding is a simple, surely understood information pressure technique utilized as a part of various application, for example, information exchange or productive picture putting away. The yield of a run length encoder is an arrangement of runs. Run-length encoding (RLE) is an extremely basic type of information pressure in which keeps running of information are put away as a solitary information esteem and tally, as opposed to as the first run.

3.3. Two phase shifting network

Two phase moving system comprise of Fixed N bit moving system and 2N bit barrel shifter.

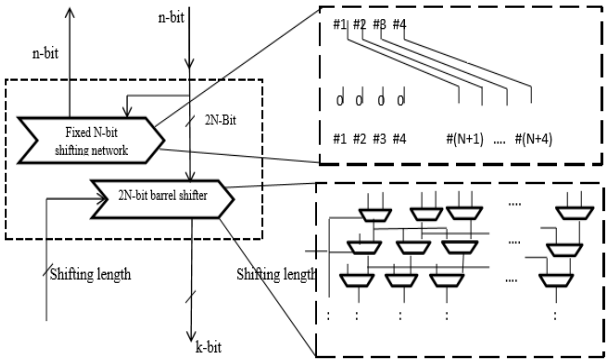

Fig. 3: Two Stage Shifting Network.

Fixed N Bit Moving System
Settled N bit moving system is utilized to just move the contribution by N. This shifter is to a great degree zone productive and no

multiplexor is required. The settled moving system is utilized to refresh the rest of the piece of the unpredictable registers.
2N Bit Barrel Shifter
A Barrel shifter is an advanced circuit that can move an information word by a predefined number of bits in a single clock cycle. It can be actualized as a grouping of multiplexers and in such a usage the yield of one mux is associated with the contribution of the following mux. The information to be packed is moved by the barrel shifter

3.4. Data compression and decompression utilizing run length encoding (RLE)

Run-Length Encoding (RLE) is made particularly for information with strings of rehashed images. For instance, if we somehow happened to pack the string AAAABBBAACCCBBBB we would get the compacted string 4A3B2A3C4B. Here one can see that the string of 15 bytes can be communicated as a string of 10 bytes. The fundamental favorable position of RLE is that it performs lossless information pressure in which the original information can be consummately recreated from the packed information.
Run length encoding has a shortcoming of its unwavering quality on the idea of the info information. At times, it can even give a bigger compacted string than the original. For instance if the info string is ABDBAC, the compacted string would be 1A1B1D1B1A1C, which is twice as huge as the original. RLE is similarly exceptionally effective in a contrary situation. In the event that the information is fundamentally the same as then the pressure rate is superior to different algorithms. As an illustration if the information string is AAAAAAAAAA, the compacted information would be 10A, which is one fifth the measure of the original gate.

4. Results and discussion

The modules are displayed utilizing VHDL in Xilinx ISE Design Suite 14.5 and the reproduction of the plan is performed utilizing Modelsim SE 6.5b to check the usefulness of the outline. Here a basic model is utilized for the coding purpose.The parallel compare and compress encoder comprise of moving Networks,Run Length Encoder ,All 0/1 finder and length control. Coding for input end moving Network, yield end moving system and Run Length Encoder is finished. PACC Encoder depends on Threshold based parallel RLE calculation. At that point the entire piece of PACC encoder was simulated.

4.1 Simulation result

Fixed N bit moving system is utilized to just move the contribution by N.This shifter is to a great degree of area efficient and no multiplexor is required. Let the 12 bit input information is

a=10101111000, moving control length = 1000 at that point yield y=000010101111

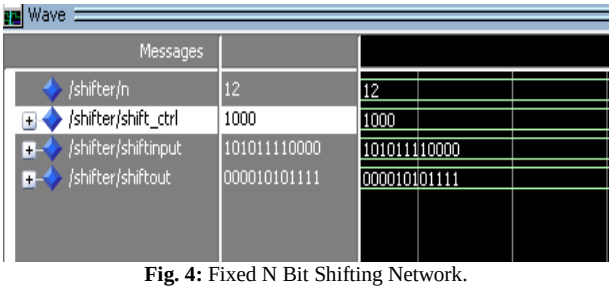

Fig. 4: Fixed N Bit Shifting Network.

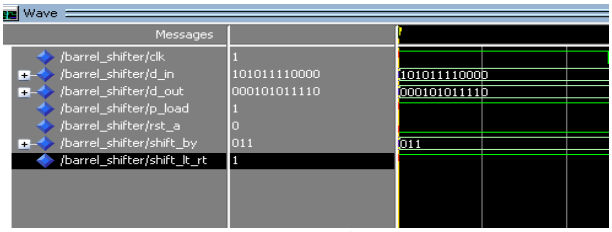

Fig. 5: N Bit Barrel Shifting Network.

A Barrel shifter is an advanced circuit that can move an information word by a predefined number of bits in a single clock cycle. It can be actualized as a succession of multiplexers and in such a usage the yield of one multiplexer is associated with the contribution of the following multiplexer Let the 12 bit input information is

D_In = 101011110000, moving length,shift_by = 011 at that point yield y=000101011110

4.2 Simulation result of PACC encoder

Run Length Encoding is a basic type of information compression technique. Same information esteem happens in numerous back to back information components are put away as a solitary information esteem and check. PaCC Encoder comprise of information (input) end moving system, yield (output) end moving system ,run length encoder,length control and every one of the 0/1 locator. Let the 12 bit input information is given as information data_in = 101011110000, after run length encoding and data compression the output will be, data_out = 101000000000.

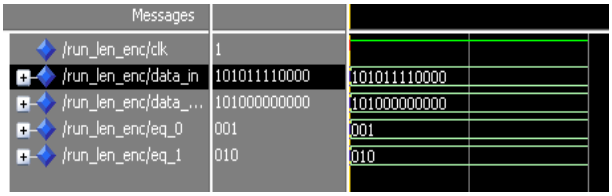

Fig. 6: PACC Encoder.

4.3. Simulation result of PACC decoder

Non volatile processors are produced with nonvolatile registers .Parallel compare and compress design is utilized to reduce the region of nonvolatile registers. PaCC decoder depends on parallel RLE calculation. PaCC decoder comprise of information end moving system, yield end moving system ,run length decoder, length control and every one of the 0/1 locator.PaCC decoder decodes the output from PaCC encoder, so that the original data is obtained. Let the 12 bit information be data_e = 101000000000, which is the output of PaCC encoder. Now the PaCC decoder decodes the input and the output will be , data_d = 101011110000.

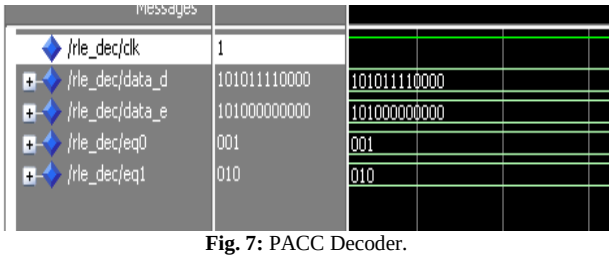

Fig. 7: PACC Decoder.

5. Conclusion

Parallel contrast and pack design is utilized with diminish overabundance region of non unstable processors. Nonvolatile processors are fabricated with nonvolatile registers. A novel PaCC codec and a reconfigurable state table were presented and the relating heuristics were produced to enhance reference vector determina-

tion. PaCC design is utilized to decrease the quantity of the bit to be put away in the nonvolatile flip-flops. Pressure codec in light of a parallel run length encoding plan is utilized. A territory productive two stage moving system is intended to limit the codec region. Half breed nonvolatile flip flops prompt huge zone increment since they contain nonvolatile capacity other than standard flipflops. The nonvolatile stockpiling, for example, ferroelectric capacitors, attractive passage intersections or drifting entryway transistors more often than not involves a vast zone. While self controlled inserted framework use on chip ferro electric arbitrary access memory to counteract information misfortune amid influence disappointments. With the help of PaCC decoder we can decode the encoders output, thereby getting the original input data. By utilizing PaCC design in nonvolatile processors, it might decrease area overhead and increment the speed.This framework can be extended by replacing 12 bit RLE encoder by 32 bit RLE encoder and a comparative study on the area of both these encoders have to be done.

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