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Research paper

Technique to Improve SNR for Sigma Delta Adcs for Audio Signals

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Abstract

A RISR architecture for Sigma-delta analog to digital converters with modified noise transfer function to obtain a better performance in terms of SNR is proposed. Cascading of two modified second order modulators are done to achieve 4th order modulator. Behavioral simulations are done to study the performance of feed-forward and the modified cascaded architecture. They are designed to operate at 1.28MHz clock frequency for audio applications (OSR of 32). It is noted that SNR of 115dB is achieved by cascading of two Modified second order RISR architectures which is 8dB more than the normal RISR architecture.

Keywords: *Sigma-Delta ADC, SNR, RISR architecture, OSR, NTF, STF, noise shaping.*

1. Introduction

Among the many analog to digital converter architectures, Sigma-delta analog to digital converters have been successful in realizing high resolution consumer audio products, such as MP3 players and cellular phones for some time now. Sigma-delta converters use very high sampling rates compared to Nyquist rate[1]. It also uses the technique of Noise shaping. Resolution of the Nyquist converters is mainly limited by the technology by which the chips are fabricated, because these converters need high matching of components. However sigma-delta converters can provide a resolution as high as 24 bits with less requirements on matching.
By using feed-forward architecture, the swings at input and output of the integrators can be reduced to a large extent and it is preferred over conventional topologies. We have suggested a slight modification to this architecture which can provide better performance. This changes the noise transfer function keeping the signal transfer function as unity. The behavioral simulations of different architectures mentioned above were carried out to study the performance. Sigma-delta modulator operating at a clock frequency of 1.28MHz with an OSR of 32 is designed in different architectures and the performances are compared. A fourth-order sigma-delta modulator, as a cascade of two second-order sigma-delta modulators, is designed and simulated, for both low distortion and modified architectures.

The SNR of the second order noise shaping modulator is [2]

$$SNR = 6.02N + 1.76 - 12.9 + 50\log(M) \qquad (1\text{-}1)$$

The SNR of a sigma-delta modulator for L^{th} order is given by the following relation [3] .

$$SNR = 6.02N + 1.76 - 10\log\left(\frac{\Pi^{2L}}{2L+1}\right) + 10(2L+1)\log(OSR) \qquad (1\text{-}2)$$

N=No. of bits of internal quantizer
L=order of modulator
OSR=Over Sampling Ratio
One of the ways to increase the SNR is to increase the order (L) of the integrator. But integrators with order more than two suffer from instability due to the accumulation of large signals. Another method is to increase the oversampling ratio. But the maximum clock frequency of the circuit is mainly limited by the technology. By using higher resolution internal ADCs also we can increase the overall SNR. Sigma-delta modulators are mainly used in low frequency applications as high OSR can be used. Higher oversampling ratio reduces the accuracy requirements of the analog components. However sigma-delta modulators have been tried for moderate frequency of the order of several MHz, like in broadband communication applications, with low OSR. In this case, better linearity of the components should be assured and distortion should be minimized. We can do architectural modification, without changing the transfer function to achieve the same. Such low distortion architectures are discussed below.

2. Review RISR Sigma-Delta ADC's

RISR Architecture

For better linearity and lower harmonics, a new architecture with a feed forward is suggested as shown in the Fig 2.1. As it reduces the swings at the input and output of integrators, it is called the Reduced Integrator Swing Range (RISR) architecture [5].

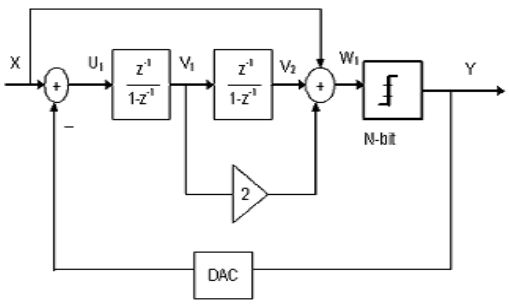


Fig. 2.1: RISR second order sigma-delta modulator

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$$Y = X + (1 - z^{-1})^2 E_N \quad (2\text{-}1)$$

$$U_1 = -(1 - z^{-1})^2 E_N \quad (2\text{-}2)$$

$$V_1 = -z^{-1}(1 - z^{-1}) E_N \quad (2\text{-}3)$$

$$V_2 = -z^{-2} E_N \quad (2\text{-}4)$$

Here the noise transfer function is the same as in the conventional sigma-delta ADC. Both U_1 and V_1 no longer depend on the modulator input X as noted from the equations 2-2 and 2-3. So the signal ranges required for U_1 and V_1 can be greatly reduced by employing multi-bit quantization. Smaller U_1 avoids op-amp slewing and smaller V_1 allows the use of lower gain op-amps, and hence reduce power dissipation. Moreover, since V_1 is now decoupled from the input X, a large full scale input can be used.

3. Modified RISR Architecture

By slightly changing this RISR architecture as shown in Fig 3.1 we can modify the noise transfer function, so that higher SNR can be achieved. This can be done keeping the signal transfer function unity. By introducing poles in the NTF, SNR can be made to increase. Another advantage is that it will increase the stability of the system by reducing the Out of Band Gain (OBG).

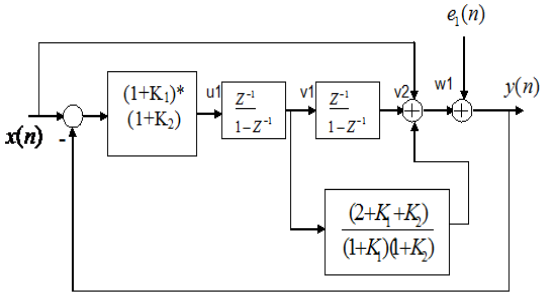


Fig. 3.1: Modified RISR architecture

$$STF = 1 \quad 3\text{-}1$$

$$NTF = \frac{(1 - z^{-1})^2}{(1 + K_1 z^{-1})(1 + K_2 z^{-1})} \quad 3\text{-}2$$

$$U_1 = \frac{-(1 + K_1)(1 + K_2)(1 - z^{-1})^2}{(1 + K_1 z^{-1})(1 + K_2 z^{-1})} * E_N \quad 3\text{-}3$$

$$V_1 = \frac{-(1 + K_1)(1 + K_2) z^{-1}(1 - z^{-1})}{(1 + K_1 z^{-1})(1 + K_2 z^{-1})} * E_N \quad 3\text{-}4$$

$$V_2 = \frac{-(1 + K_1)(1 + K_2) z^{-2}}{(1 + K_1 z^{-1})(1 + K_2 z^{-1})} * E_N \quad 3\text{-}5$$

K_1 and K_2 should be less than 1 to maintain the stability. Comparison of conventional second order modulator and Modified RISR architecture is shown in Fig 3.2. As the value of K_1, K_2 increases, the peak of the transfer function also increases. But the values of the transfer function at low frequencies get reduced. The low frequency portion in the audio frequency range is shown in Fig 3.3.

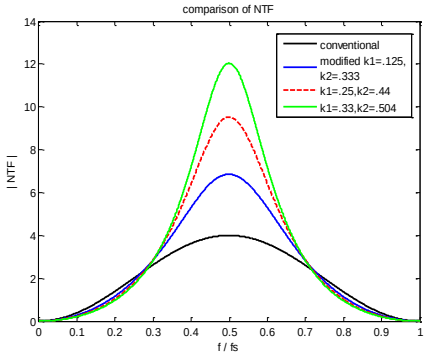


Fig. 3.2: Comparison of various Noise Transfer Function (NTF)

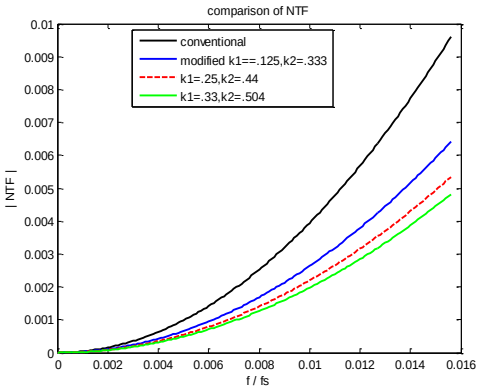


Fig. 3.3: Comparison of various NTF in the audio frequency range

From Fig 3.3, it is clear that as we go for higher K_1 and K_2 values, the low frequency portion of the noise get suppressed more and more. As we use a decimator low pass filter at the output of the modulator, the high frequency part of the noise can be removed. Hence by this method we can achieve higher Signal to Noise Ratio (SNR).

From equations 3.3-3.5, it is clear that inputs and outputs of the integrators depend on the K_1 and K_2. Hence, K_1 and K_2 should be chosen in order to keep the integrator input and output to a specific level. This level can decided depending upon the swing that can be achieved by the opamp used in the integrator.

Modified RISR 4th Order Modulator

We designed a 4th order modulator by cascading two Modified second order RISR architectures.

$$H_1(z) = \frac{(1 - z^{-1})^2}{(1 + K_1 z^{-1})(1 + K_2 z^{-1})} \quad 3\text{-}6$$

$$H_2(z) = 1 \quad 3\text{-}11$$

$$NTF = \frac{(1 - z^{-1})^4}{(1 + K_1 z^{-1})(1 + K_2 z^{-1})(1 + K_3 z^{-1})(1 + K_4 z^{-1})} \quad 3\text{-}7$$

This gives an improvement in SNR.

4. Results

MATLAB is chosen for behavioral simulations [1].

Simulations to determine optimum K_1, K_2 values:

It is assumed that opamp can provide 60% of the fullscale (FS) voltage. Hence simulations are carried out to find maximum K_1, K_2 values for which the integrator swing is less than 60% of FS, for inputs of amplitude less than or equal to 80% of the FS. It is observed that as the K_1, K_2 values increases, swing at the input

and output of the integrator also rises. The maximum value of the input and output of the integrators for different K1, K2 values are plotted as shown in Fig 4.1, Fig 4.2 and Fig 4.3.

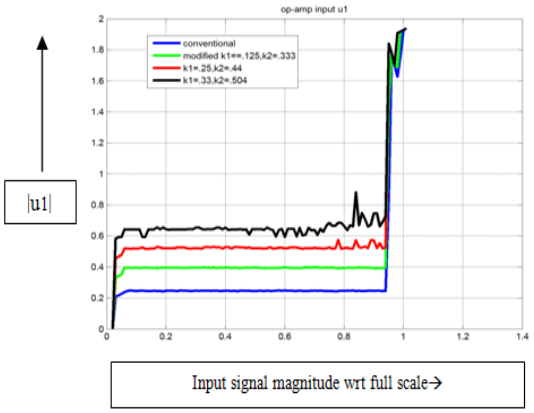


Fig. 4.1: Maximum magnitude of input of the first integrator

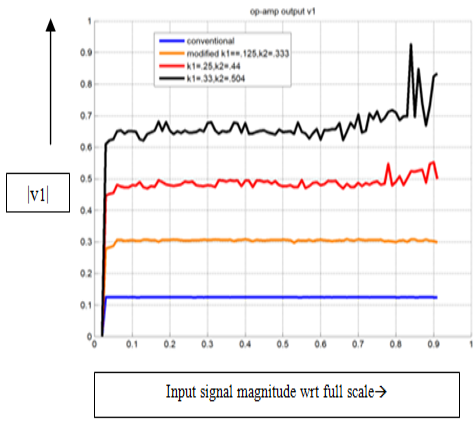


Fig. 4.2: Maximum magnitude of output (input) of the first (seond) integrator

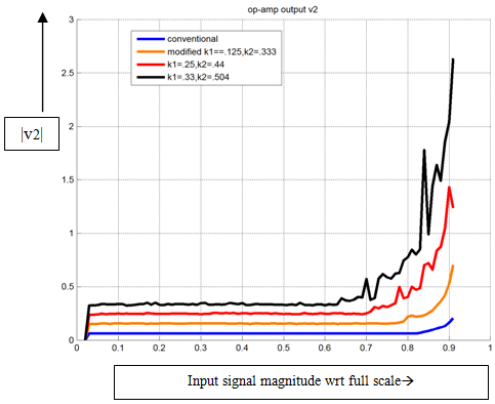


Fig. 4.3: Maximum magnitude of output of the second integrator

For $(1+ K_1)*(1+ K_2) > 1.5$, the opamp output is more than 60% FS. Many K_1-K_2 combinations could be used. In this, we have used $K_1 = 0.125$ and $K_2 = 0.333$ and simulations were done for these values. To get further improvement, cascading of two modified second order RISR architectures were done.

5. Conclusion

Comparison of SNR for RISR and Modified RISR modulators:
By increasing K_1, K_2 values SNR increases. Optimized K_1, K_2 values are selected which is $K_1 = 0.125$ and $K_2 = 0.333$ by considering op-amp input and output swings. We get maximum SNR of 80.5dB for Conventional RISR modulator and 84.5dB for Optimized Modified RISR modulator which shows 4dB improvement as shown in Fig 5.1.

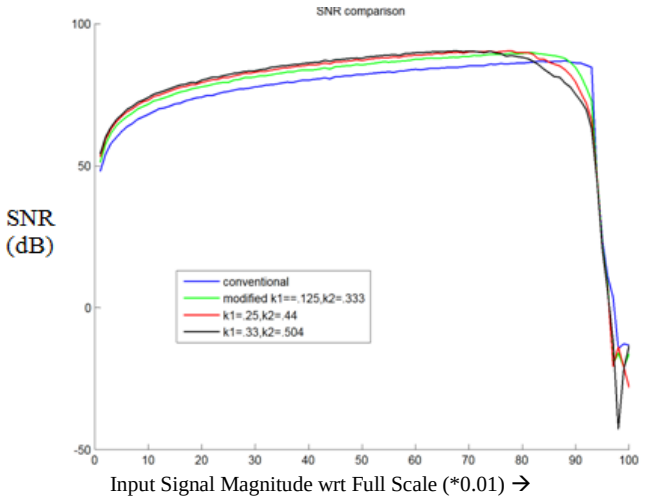


Fig. 5.1: Variation of SNR vs input amplitude (comparison) cascaded modified (2-2) Sigma delta modulator

It is noted that SNR of 115dB is achieved by cascading of two Modified second order RISR architectures which is 8dB more than the normal RISR architecture as shown in Fig 5.2.

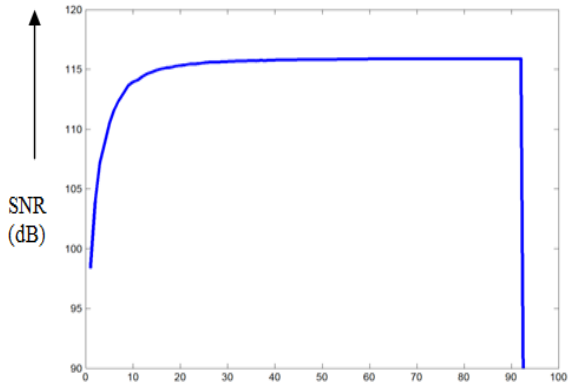


Fig. 5.2: Variation of SNR vs input amplitude (cascaded stage)

References

[1] Schrier R & Temes GC, *Understanding Delta-Sigma Data Converters*. John Wiley and Sons Inc., (2005).
[2] Johns DA & Martin K, *Analog Integrated Circuit Design*, John Wiley and Sons Inc., (1997).
[3] Pervez M, Aziz HVS & Jan VD S, "An overview of sigma-delta converters", *IEEE Signal processing magazine*, Vol.13, No.1, (1996).
[4] Ki YN, Sang ML, David KS & Bruce AW, "A Low-Voltage Low-Power Sigma-Delta Modulator for Broad band analog-to-digital conversion", *IEEE journal of solid-state circuits*, Vol.40, No.9, (2006).
[5] Ahmed G & Johans DA, "On the implementation of input- feed forward Delta-sigma modulators", *IEEE Transactions on circuits and systems*, Vol.53, No.6, (2006).
[6] Baker RJ, Harry WL & David EB, *CMOS Circuit Design, Layout, and Simulation*, IEEE Press., (1998).
[7] Baker RJ, Harry WL & David EB, *CMOS Mixed-signal Circuit Design*, John Wiley and Sons Inc., (2003).