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Research paper

High performance turbo encoder using mealy FSM state encoding technique

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Abstract

Error-correction Coding plays a vital role to obtain efficient and high quality data transmission, in today's high speed wireless communication system. Considering the requirement of using high data rates by Long Term Evolution (LTE) system, parallel concatenation of two convolutional encoders were used to design turbo encoder. In this research task a high speed turbo encoder, which is a key component in the transmitter of wireless communication System, with memory based interleaver has been designed and implemented on FPGA for 3rd Generation Partnership Project (3GPP) defined Long Term Evolution – Advanced (LTE-A) standard using Finite state Machine(FSM) encoding technique. Memory based quadratic permutation polynomial (QPP) interleaver shuffles a sequence of binary data and supports any of the 188 block sizes from N= 40 to N= 6144. The proposed turbo encoder is implemented using 28nm CMOS technology and achieved 300 Mbps data rate by using 1% of available total hardware logic. By using the proposed technique, encoded data can be released continuously with the help of two parallel memories to write/read the input using pipelining concept.

Keywords: *LTE-A Standard; Turbo Encoder; QPP Interleaver; FSM Technique; Look Up Table (LUT); Parallel Architecture.*

1. Introduction

The ever increasing demand for faster data rates, the recent mobile telecommunication system LTE, defined by 3GPP [1]-[2], has been come to existence by the invention of turbo codes [3]-[4], whose BER performance is near to Shannon limit. In today's state-of-the-art iterative channel codes such as low-density parity check, turbo and polar codes achieve the high diversity, reliable data transmission and possible high coding gain in fading channels. Turbo code is one of the high performance error-correction coding schemes in a noisy environment and is a standardized coding scheme from Universal Mobile Telecommunications System (UMTS) technology, since 1999.

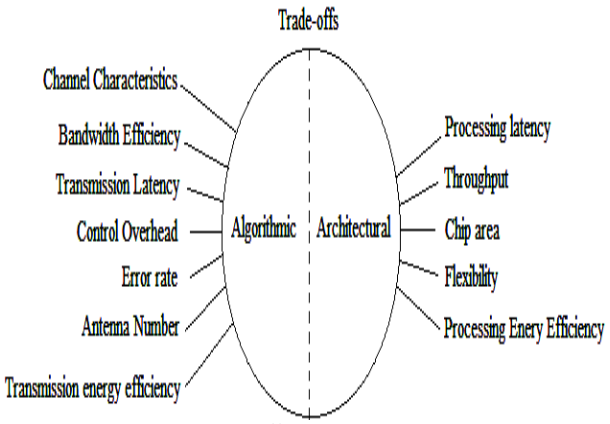

Fig. 1: Design Trade-Offs in a Communication System.

The interrelation between efficient channel coding schemes and their hardware architectures with underlying silicon technologies were demonstrated in [5]. There are design trade-offs as listed in Fig. 1. [6], in both algorithm and architectural level. Turbo codes are better suited for bit error probabilities above the error floor. Turbo codes offer a lower BER without increased energy consumption, thus they have been extensively used in energy constrained applications like Internet of Things (IoT), wireless sensor networks and in space constrained applications like wireless local area network, cellular telephony and broadcast systems [6]. Holistic design methodologies minimize the energy consumption as compared to conventional methods. Turbo Encoder is constructed using two identical RSC encoders linked parallel with an interleaver and corresponding decoder using a feedback decoding rule in pipelined structure. Interleaver is a pivotal component in turbo encoder/decoder and its hardware logic design is crucial for high performance. Various investigators developed numerous approaches in the logic design and hardware implementation of turbo encoder/decoder. Ferrari [7], in which multiple numbers of input lines used to obtain rate variability from 1/2 to 7/8, proposed the rate variable coding scheme. The rate variability is achieved by shortening the high data rate rather than puncturing it. An optimized 8-level parallel algorithm was used to increase the hardware implementation performance [8]. Dual RAM was used in interleaver to reduce clock latency and recursive pair wise matching for reduced arithmetic computations. An optimized PCC Turbo code was proposed [9] for significant enhancement in BER performance in high, moderate and low values of SNR by augmenting d_{free}, N_{free}, w_{free} applying harmony search algorithm. A memory efficient, low power and scalable turbo encoder [10] was proposed for all turbo encoder applications, supports parallel encoding with scalable memory requirement. A novel Parallel Concatenated Convolution Turbo code (PCCTC) was proposed [11] to

enhance BER performance by providing optimum power than uniform power distribution in systematic and parity bits using flower pollination algorithm FPA [12]. A class of interleavers was proposed in [13] for turbo codes formed on permutation polynomials, which were algebraically formulated to fit for a given component code, where simple arithmetic operations were used to interleave/de-interleave the sequence of data.
Further contents regarding design and implementation of turbo encoder are discussed in section II through section IV. In addition, results are discussed in detail in section V.

2. System model

Turbo encoder design for LTE system is a parallel concatenation of two recursive systematic convolutional encoders connected through an interleaver, based on 3GPP standard as shown in Fig. 1.2.

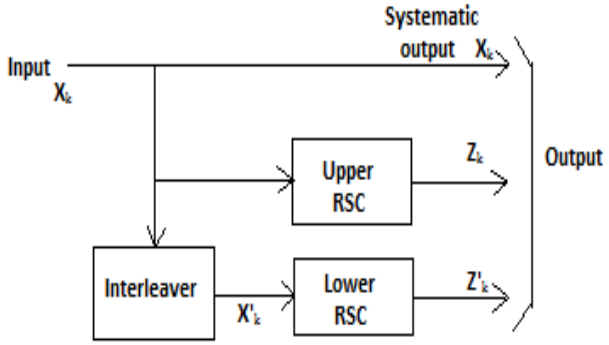

Fig. 2: Block Diagram of Turbo Encoder.

The lower encoder is connected to input through an interleaver, where interleaver shuffles the positions of input data. This parallel structure is accommodated to reduce the clock latency of the system; thereby the bit rate is increased. Design of PCC Code [14], which is also termed as turbo code, is a 1/3 rated code obtained from two equal rate 8-state recursive systematic convolutional (RSC) coders as shown in Fig. 3. The input data block X_k is sent as systematic bits obtained at the output, as it is X_k, where k represents the number of input bits. At the same time, the same information sequence X_k is processed through upper recursive systematic convolutional encoder and it generates the parity bit stream Z_k. Concurrently, the input X_k is reorganized by going through the internal interleaver and rearranged as X'_k. The lower recursive systematic convolutional encoder, resulting parity bit stream Z'k, processes the X'k information sequence. The structure of 1/3 code rate turbo encoder is shown in Fig 3.

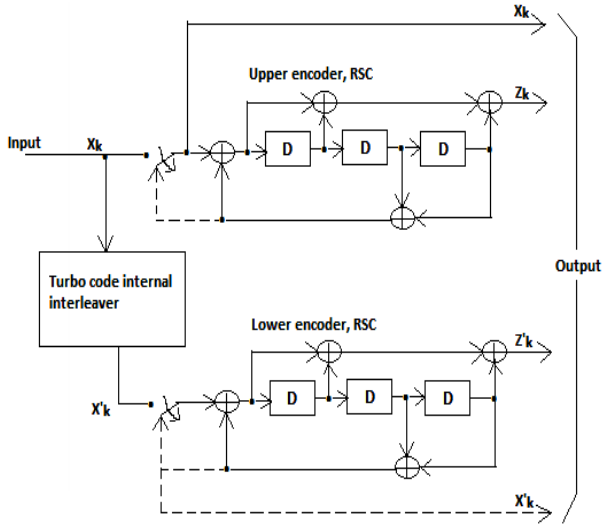

Fig. 3: Structure of 1/3 Rate Turbo Code Encoder.

2.1. Turbo code interleaver

The relation of input to output of interleaver as per 3GPP LTE system can be expressed in a simple algebraic equation as mentioned below.

$$X_i^{'} = X_{\pi(i)} \quad (1)$$

Where i = index, ranges 0 to k-1 and

$$\pi(i) = (f_1 i + f_2 i^2)\ mod k \quad (2)$$

Where, the parameters f_1 and f_2 depends on size of k and are mentioned in Reference [2]. The complexity of QPP interleaver lies in calculation of polynomials.

3. Proposed LUT based QPP interleaver

The structure of QPP interleaver is constructed based on algebraic permutation polynomials. As defined by 3GPP in [2], quadratic permutation polynomial structure produces contention-free interleavers. The interleaved data can be mathematically described as shown in equation 1 and 2. Look up Table (LuT) based QPP pseudo random interleaver is proposed for LTE-A standards of turbo encoder. The parameters f1 and f2 are interleaver internal parameters, the value of which depends on length of code-block k, in the polynomial equation. In the proposed QPP interleaver, f1 and f2 values are directly accessed by the locations of LuT for calculations. Instead of using multiplier, an array structure is used for polynomial Calculations. Address-computation for QPP interleaver is carried out according to the equation 2.
Clock latency can be reduced further by direct manipulation as the Eq.2 is derived into [5] level parallelization according to length of code block k,
If (block length < 512)

Index = 13'd0 + (block length - 32) - 13'd1;

Else if (block length < 1024)

Index = 60 + (block length - 512) - 13'd1;

Else if (length < 2048)

Index <= 92 + (block length - 1024) - 13'd1;

Else if (length < 4096)

Index <= 124 + (block length - 2048) -13'd1;

Else

Index <= 156 + (block length - 4096) -13'd1;

The values of f1, f2, i, i^2 are arranged in an array type of structure for polynomial calculation to improve the hardware performance. The parameters f_1, f_2 values will be accessed by address locations of LUT and index will be calculated with the help of logic defined as above defined [five] level parallelization.

4. Proposed turbo encoder

4.1. FSM encoding technique

Finite state machine (FSM) method is proposed here to design turbo encoder for reducing the logic complexity as compared to that involved in the design using X-OR logic gates in Fig. 1.3, in convolutional designs. FSM state encoding technique works according to predefined next states for appropriate input sequence.

The 8-state RSC code with its state transition table is specified in the Table 2. The output bit stream depends not only on input but also on previous state. This technique is proposed for both upper and lower RSC encoders in turbo encoder to reduce the logic complexity, thereby reducing clock latency.

Table 1: State Transition Table

Input bit Stream	Current State	Next State	Output Out1 Out2
0	000	000	0 0
1	000	100	1 1
0	001	100	0 0
1	001	000	1 1
0	010	101	0 1
1	010	001	1 0
0	011	001	0 1
1	011	101	1 0
0	100	010	0 1
1	100	110	1 0
0	101	110	0 1
1	101	010	1 0
0	110	111	0 0
1	110	011	1 1
0	111	011	0 0
1	111	111	1

4.2. Proposed data synchronization

The pipelining concept is used to the proposed turbo encoder architecture, the design consist of two generic dual port RAM memories, termed ping and pong , used as code block buffers to write the input sequence and read by RSC encoder through 2x1 multiplexer as shown in Fig. 1.4. The pong memory will be loaded if the ping memory loaded and started to read by encoder. This parallel loading and reading is proposed to avoid the delay between the information sequences thereby increasing the data rate. The data from ping and pong memories will be sent through a 2X1 MUX to RSC encoder. Here, 2X1 MUX is operated by turbo control logic. The turbo control logic will decide that the date from ping or pong memory to be given to RSC encoders, alternatively, depending on READ/WRITE operation.

Table 2: Current LTE Data rates

	Channel Bandwidth	1.4MHz	3MHz	5MHz	10Mhz	15MHz	20MHz
	Resourse Blocks in the Frequency domain	6	15	25	50	75	100
Normal Cyclic Prefix	OFDMA symbols per 1 ms	14					
	Modulation symbol rate (Msps)	1	2.5	4.2	8.4	12.6	16.8
	QPSK Bit Rate (Mbps)	2	5	8.4	16.8	25.2	33.6
	16 QAM Bit Rate (Mbps)	4	10.1	16.8	33.6	50.4	67.2
	64 QAM Bit Rate (Mbps)	6.1	15.1	25.2	50.4	75.6	100.8
	2X2 MIMO 64QAM Bit Rate (Mbps)	12.1	30.2	50.4	100.8	151.2	201.6
	4X4 MIMO 64QAM Bit Rate (Mbps)	24.2	60.5	100.8	201.6	302.4	403.2

In the proposed design, the input is applied continuously to the encoder structure by the support of proposed data synchronization unit using pipelining concept, consists of two dual port RAMs, control logic and a 2X1 multiplexer.

5. Results & discussions

Turbo encoder design is implemented using Finite State Machine technique for two 8-state RSC encoders with LUT based QPP interleaver and the simulation results are shown in Fig. 1.5 (a) & (b).

The proposed FSM based Turbo encoder is implemented using 28nm CMOS technology and achieved 300 mbps data rate. RTL design and FPGA verification of simulation results of proposed turbo encoder with 28nm CMOS technology has been done on Vertex'7 FPGA evaluation board.

The table 1.2. Shows theoretical absolute maximum physical layer throughputs if all the resource elements (bandwidth, normal to extended cyclic prefix and overheads generated by other physical signals and physical channels) were allotted to the physical downlink shared channel (PDSCH).

The proposed design which is compatible to 2X2 MIMO 64 QAM is giving the bit rate 300Mbps at 20MHz channel bandwidth. The result shows that the best case achievable total delay, device utilization summary and bit rate as shown in Fig.1.7.

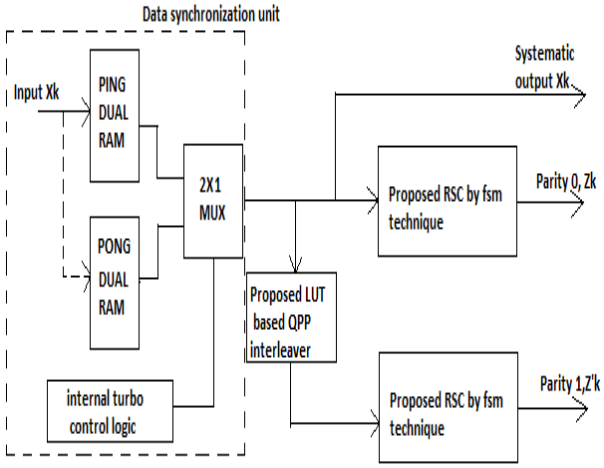

Fig. 4:. Block Diagram of Proposed Turbo Encoder Architecture.

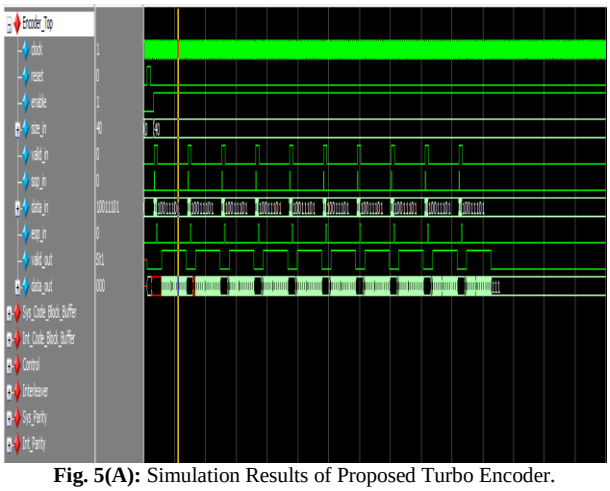

Fig. 5(A): Simulation Results of Proposed Turbo Encoder.

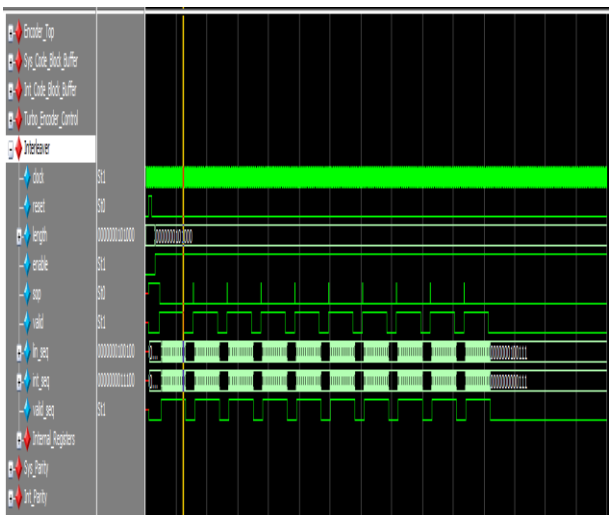

Fig. 5 (B): Simulation Results of Proposed QPP Interleave.

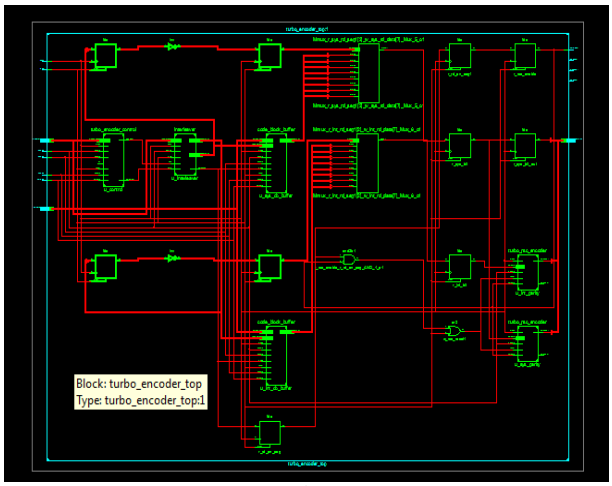

Fig. 6:.RTL Schematic of Proposed Turbo Encoder

```
Data Path: r_rsc_enable to valid_out
                                   Gate     Net
  Cell:in->out       fanout       Delay    Delay
  ---------------------------------------------
   FDC:C->Q             3         0.232    0.289
   OBUF:I->O                      0.000
  ---------------------------------------------
  Total                          0.521ns (0.232n
                                         (44.5%
```

Device Utilization Summary				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	258	408,000	1%	
Number used as Flip Flops	258			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	1,244	204,000	1%	
Number used as logic	474	204,000	1%	

Met	Constraint	Check	Worst Case Slack	Best Case Achievable	Timing Errors	Timing Score
Yes	TS_clock = PERIOD TIMEGRP "clock" 3.333 ns HIGH 50% INPUT JITTER 0.1 ns	SETUP	0.016ns	3.317ns	0	0
		HOLD	0.025ns		0	0

Fig. 7: Total Delay, Device Utilization Summary and Best Case Bit Rate

The proposed logical design has been analyzed for its trade-offs in terms of data rate achieved, total delay, total device utilization and it is shown that the proposed design achieves the best performance. In addition, the total delay is combination of gate delay, net delay is 0.521 ns achieved, and providing 300Mbps data speed at 20 MHz bandwidth.

6. Summary

In this paper, a high performance turbo encoder with memory based QPP interleaver was discussed. The proposed architecture has been designed, verified on Vertex'7 FPGA evaluation board with 28nm CMOS technology and analyzed improvement in terms of increased data rate 300Mbps , less number of slice registers used, 258 out of 408,000 (only 1%) and reduced clock latency than conventional methods. The clock latency is reduced by parallelization in QPP interleaver. The proposed work finds application in advanced wireless communications like 4G and 5G, Satellite Communications- Consultative Committee for Space Data Systems (CCSDS) Telemetry standard and Digital Video Broadcasting (DVB).

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