International Journal of Engineering & Technology, 7 (4) (2018) 2747-2752

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET
doi: 10.14419/ijet.v7i4.14141
Research paper

Symmetric stacked fast binary counters based on reversible logic

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Abstract

A Symmetric Stacked Fast Binary counter design is proposed in this paper. In the circuit design, the first phase is occupied by 3-bit stacking circuits, which are further followed by combining circuits. The resultant novel circuit thus becomes a 6-bit stacker. A 6:3 counter has been chosen as an example to demonstrate the working of the proposed circuit. The proposed circuit is further implemented by using reversible logic gates. Heat dissipation is a major problem in the designing of a digital circuit. Rolf Landauer has proved that the information loss in a digital circuit is directly proportional to the energy dissipation. The proposed modified Symmetric Stacking counter is implemented using reversible logic gates thus reducing the power dissipation of the circuit.

Keywords: *Use about five key words or phrases in alphabetical order, Separated by Semicolon.*

1. Introduction

The technology called reversible computing is the solution to the heat problem being faced by the electronics industry in the current era. For example, today's laptops produce much heat coming out of it. The reason behind this phenomena is that today's computing uses irreversible computing methods. Heat dissipation is a major problem in the designing of a digital circuit. Rolf Landauer has proved that the information loss in a digital circuit is directly proportional to the energy dissipation. the mathematical formulation of the above statement is that if a bit is lost in a digital system, the amount of energy lost is either equal or greater than KTln2 joules in the form of heat. To provide a solution to this problem statement, reversible computing was introduced. In reversible computing, the input count is equal to the output count. There is a one to one relation between the inputs and outputs in a circuit. As reversible computing does not discard any of the bits, the energy last in the form of heat, is proclaimed to be zero.

To illustrate this further, take an AND gate with two inputs. If there's a voltage on the first input and the second input, an output voltage is produced. But if one of the inputs has zero volts, the output produced is zero volts. So this confers that the gate produces an output only if both of the inputs have a voltage. Right now, an 'and' gate is not reversible. Reversible means that, if the output signal can be sent back into the circuit, the original inputs are produced at the input end. To have a reversible circuit, the circuit must have the same number of ports. According to the literature [1], if the number of inputs is equal to the number of outputs, then the circuit refrains from generating any heat. This is one of the most significant discoveries in computer science of the 20th century because this would imply that there's no heat problem. One can have massive three-dimensional circuitry in everyday electronics.

Christopher Fritz and Adly T. Fam [2] presented a fast binary counter using 3-bit stacking circuits. The collected [1] bits are grouped together and then the circuit is followed by 6:3 counter without xor gates. This is done to increase the speed of the circuit operation. Xiaoping Cui [3] presented a hybrid parallel decimal multiplier by analyzing the properties of three different circuits, namely, overloaded decimal digit set (ODDS), excess [3] code and BCD 4221/5211.

C. S. Wallace [4] proposed a multiplier design for fast numerical calculations. Here the entire circuitry was purely formed with conventional combinational logic. The time of calculations was reduced drastically by using the diode transistor logic. L. Dadda [5] presented binary multipliers using parallel counters for combinatorial circuits. The final result was obtained in two stages. In the first stage, the product of the operands was produced without a carry. Then in the second stage, the result was updated with carry propagation.

Jonathan Scarlett [6] researched the memoryless binary input channels. The field of study was the mismatched decoding problem. This method was proved to be better than the conventional optimal decoder on the grounds of implementation limitations and channel uncertainty. Kwang-Chun Choi [7] proposed an error correction scheme for circuits with a multiphase clock in time to digital converters.

In this paper, the section I gives a description of the current challenges faced by the electronics industry and the literature proposed by various authors in this domain. Section II explains the concept of symmetric bit stacking. The reversible logic is presented in section III.

2. Symmetric bit stacking

A Symmetric Stacked Fast Binary counter design is proposed in this paper. In the circuit design, the first phase is occupied by 3-bit stacking circuits, which are further followed by combining circuits. The first step used here is, small 3-bit stack circuits are used to form the 3-bit stacks. These 3-bit stacks are combined together

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to form a 6-bit stack. The technique used here is symmetric technique, this adds an extra layer of logic.

a) Three-Bit Stacking Circuits

The inputs considered are Y_0, Y_1, Y_2, there are 3 outputs for the 3-bit circuits, Z_0, Z_1, Z_2, measurements are taken in such a way that the number of "1" bits in the outputs is equal to the number of "1" bits in the input, the "1" are grouped together to the left which is followed by the "0". The outputs then formed are,

$$Z_0 = Y_0 + Y_1 + Y_2 \quad (1)$$

$$Z_1 = Y_0\,Y_1 + Y_0\,Y_2 + Y_1\,Y_2 \quad (2)$$

$$Z_2 = Y_0\,Y_1\,Y_2 \quad (3)$$

From the above equations, the first output from equation 1 will be "1" if any of the input is one, from the 2nd equation it is clear that the output will be "1" if any two of the inputs are one, from the 3rd equation the output will be "1" if all the inputs are one. Since Y_1 is having a majority function it can be implemented using one CMOS gate. Fig 1 shows the 3-bit stacking circuit.

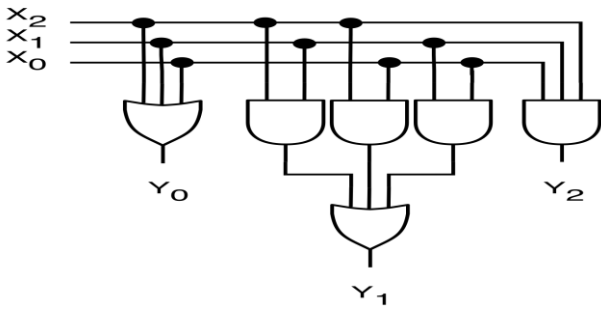


Fig. 1: Three-Bit Stacking Circuit.

b) Converting Bit Stack to Binary Number

For implementing a 6:3 counter circuit, the 6-bit stack discussed in Section II must be converted to a binary number. In order to get a faster and more efficient count, intermediate values such as M, N, O, are used to compute quickly the output bits without the need of the bottom layer of the stackers. The binary representation of the "1" input bits is C_2, C_1, S. These are called for the output bits.

In order to compute S, it should be noted that the determination of parity bits of the outputs from the 1st layer of 3-bit stackers is easy. Parity might occur in H if zero or two "1" bits appear in X_0, X_1, and X_2. The even parity bits of M and N bits are denoted as M_e and N_e, they are shown below,

$$M_e = \overline{M_0} + M_1\overline{M_2} \quad (4)$$

$$I_e = \overline{I_0} + I_1\overline{I_2} \quad (5)$$

For all the input bits S indicates the odd parity. The sum between the two different parities is odd we can compute

$$S = M_e \oplus N_e \quad (6)$$

Even though there is an XOR gate delay, it is not present in the critical path. When the count is [2-3] or [6] then we note that C_1 = 1. Two cases arise in this. First, we need to see that we have at least two inputs but not more than [3] inputs in total. For this, the intermediate vectors M, N, P can be used. Checking of at least two inputs, we need to see the length of the stack which is two from either top-level stacker or two stacks having length one, which produces $M_1 + N_1 + M_0\,N_0$. To check for the input set, not having more than three inputs, we need to see to that no K bits are set as K vector. We get

$$\overline{(P_0 + P_1 + P_2)} \quad (7)$$

Secondly, we need to see if all the 6 inputs as "1". This can be done by checking all the sets from both M and N are set. We know that these bits are in a stack, so we can just check the rightmost bit of the stack in this case, which yields $M_2\,N_2$. On the whole this yields,

$$C1 = (M1 + N1 + M0\,N0)\,(P0 + P1 + P2) + H2\,I2 \quad (8)$$

C_2 can easily be calculated as it is set when we have at least 4-bit set

$$C_2 = K_0 + K_1 + K_2 \quad (9)$$

The construction of the 6:3 counter circuit can be done by using the equation (4)-(9). The 6:3 counter circuit is shown in Fig 2.

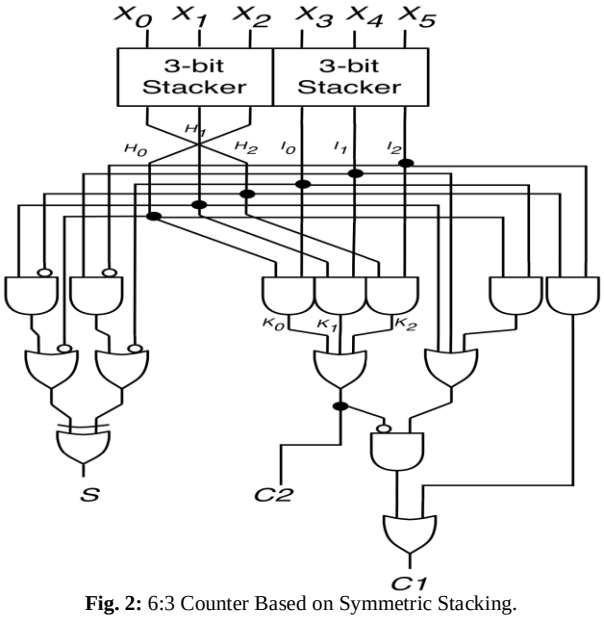


Fig. 2: 6:3 Counter Based on Symmetric Stacking.

The critical path delay is reduced to seven basic gates by using larger CMOS gates. This 6:3 counter performs better than the existing design as there are no XOR gates in the critical path. There is one drawback of this counter that is the wiring complexity. On comparing this with the traditional counters, the Symmetric approaches, as shown in Fig 1 and 2, signals cross after the first layer of the stackers.

3. Reversible logic

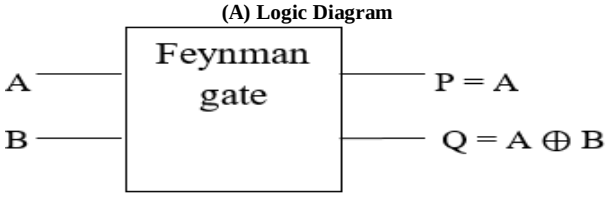
The Fundamental motivation of reversible logic comes from energy concerns. Computers use a lot of energy. There are more than 3 billion personal computers in use and in excess of 30 million servers running constantly around the world. All of these some up to use a tremendous amount of energy. More than two and a half percent of the entire energy budget of the world. In the 1940s with the advent of electronic computers, physicists started to ask themselves this question why did their house-sized computer use so much energy. But it wasn't until the early 60s that Philander, a German physicist with IBM came up with a surprising answer he found that it is irreversibility that places a lower limit on what we can do with respect to energy. So this is codified in what's known as Landauer's principle which says that for every irreversible operation, one has to dissipate a minimal amount of energy.

For the last 40 years, the semiconductor industry on which the computers are built, have been able to exponentially decrease the amount of energy used per bit operation. So even though the limit placed by Landa was principal which is very tiny, it's been the case that has been able to decrease the energy with an order of magnitude every one and a half two years.

As the advent of multi-core processors and so on that heat is actually becoming a serious problem now the key insight here is that this applies only to irreversible computations. if the reversible computations are used then this barrier disappears and energy consumption per operation should be lowered, basically without limit but of course this particular limit is a very tiny amount and in fact it's been it's so tiny that it took 50 years from the from the establishment of the theoretical principle to experimental validation.

Now on trying to add something to the output of the machine sufficient enough to make it reversible, so in this case an additional output is added so that it is not just a plus machine but a plus-minus machine such that when we give it X, Y it returns both their sum and their difference, now if this 3:1 is given it results in foreign. Now when the machine is run backwards and optional inputs such as 8 and 2 are given then it's not difficult to see that these actually uniquely define the inputs 5 & 3 okay so this machine now has the property of reversibility so it can be seen that it's not actually the same as having performed with the plus machine which means that somehow reversible computations are fundamentally different.

(A) Logic Diagram

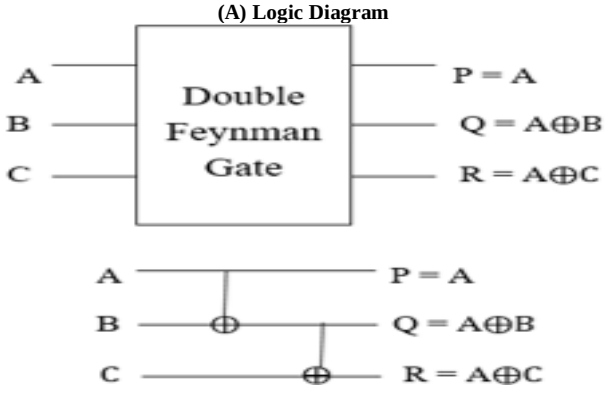


(B) Truth Table

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fig. 3: Feynman Gate.

(A) Logic Diagram

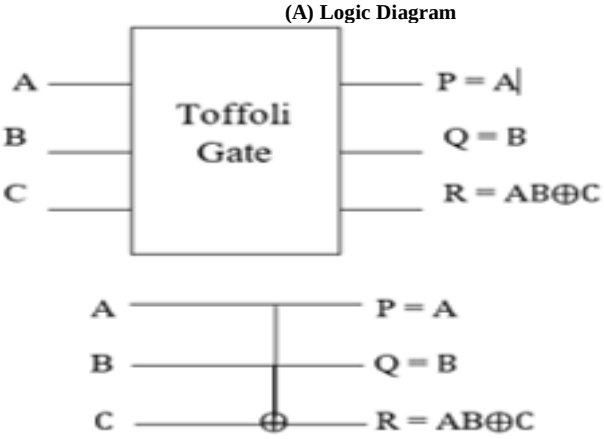


(B) Truth Table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Fig. 4: Double Feynman Gate.

(A) Logic Diagram

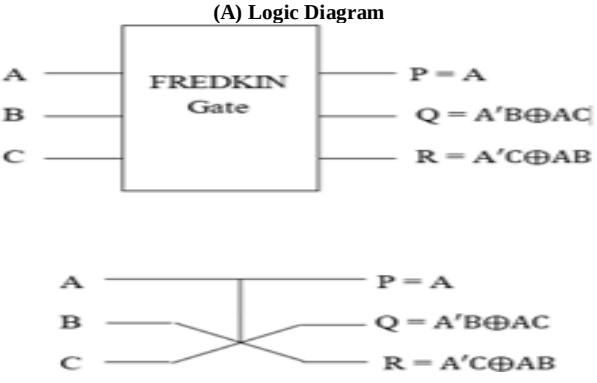


(B)Truth Table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	0

Fig. 5: Toffoli Gate.

(A) Logic Diagram

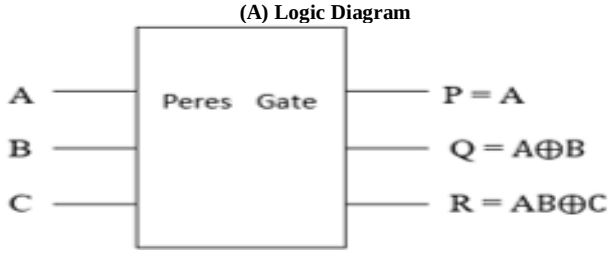


(B) Truth Table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Fig. 6: Fredkin Gate.

(A) Logic Diagram



(B) Truth Table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig. 7: Peres Gate.

The power dissipation of each of the gates is listed in the table below.

Table 1: Average Power

S. No.	Gate	Average Power
1	Feynman Gate	3.6817E-06
2	Double Feynman gate	6.0256E-06
3	Toffoli gate	4.4939E-06
4	Fredkin Gate	8.1265E-06
5	Peres Gate	1.4538E-05

4. Reversible logic representation of three-bit stacker circuit

As discussed in the sections II and III, adapting reversible logic technology to the existing circuits balances the fan out of the circuits. The circuit presented in figure1 is implemented using the reversible logic gates. The gates used are Fredkin and Peres, whose individual gate level functionality us presented in figures 6 and 7.

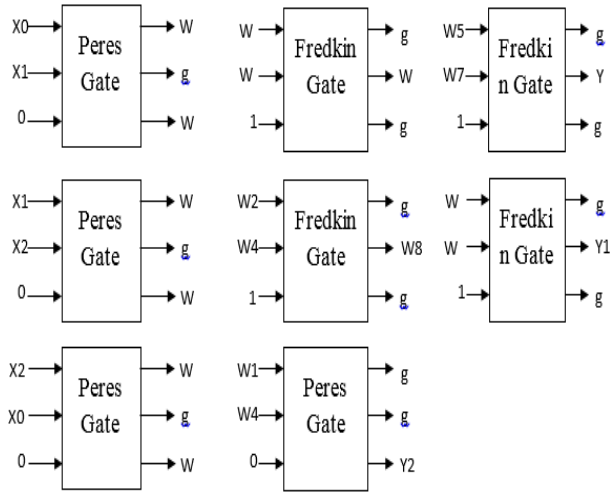


Fig. 8: Reversible Logic 3-Bit Stacker Circuit.

Here, X0, X1 and X2 are the inputs and Y1, Y2 and Y3 are the outputs. The intermediate connections are given the labels W1, W2, W3 and so on. As discussed earlier, each gate produces garbage results which are denoted by 'g'. The output of the proposed circuit exactly matches with the conventional circuit and is depicted in figure 9.

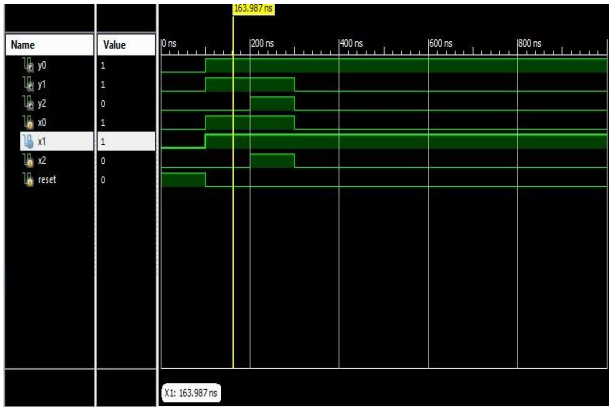
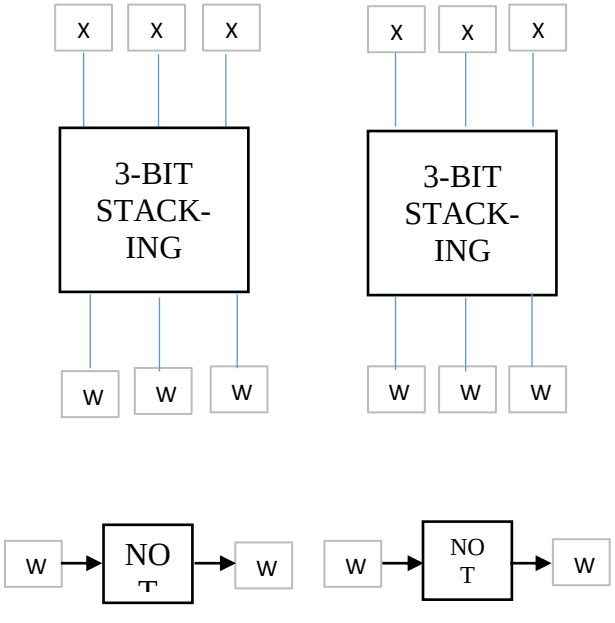


Fig. 9: Simulation Result of Reversible Logic 3-Bit Stacker Circuit.

The implementation of the stacked symmetric counter using reversible logic gate involves the substitution of the gates without disrupting the signal flow and the preserving the truth table.



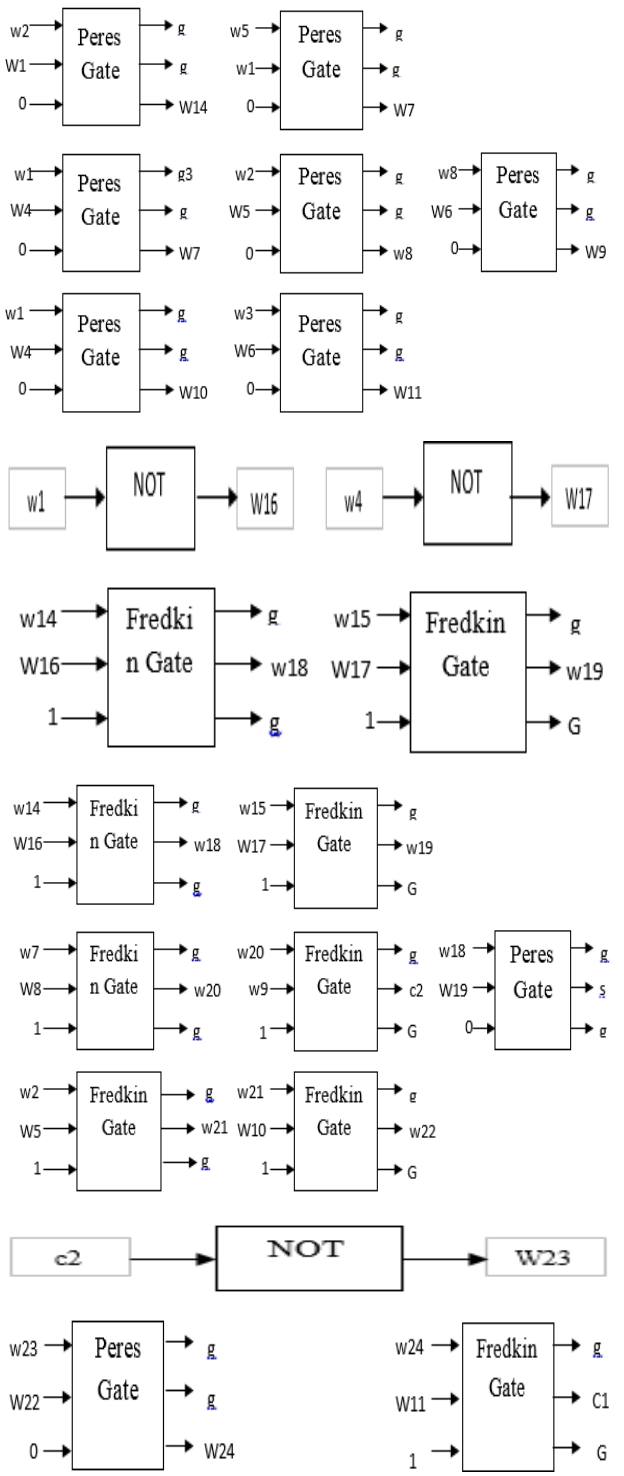
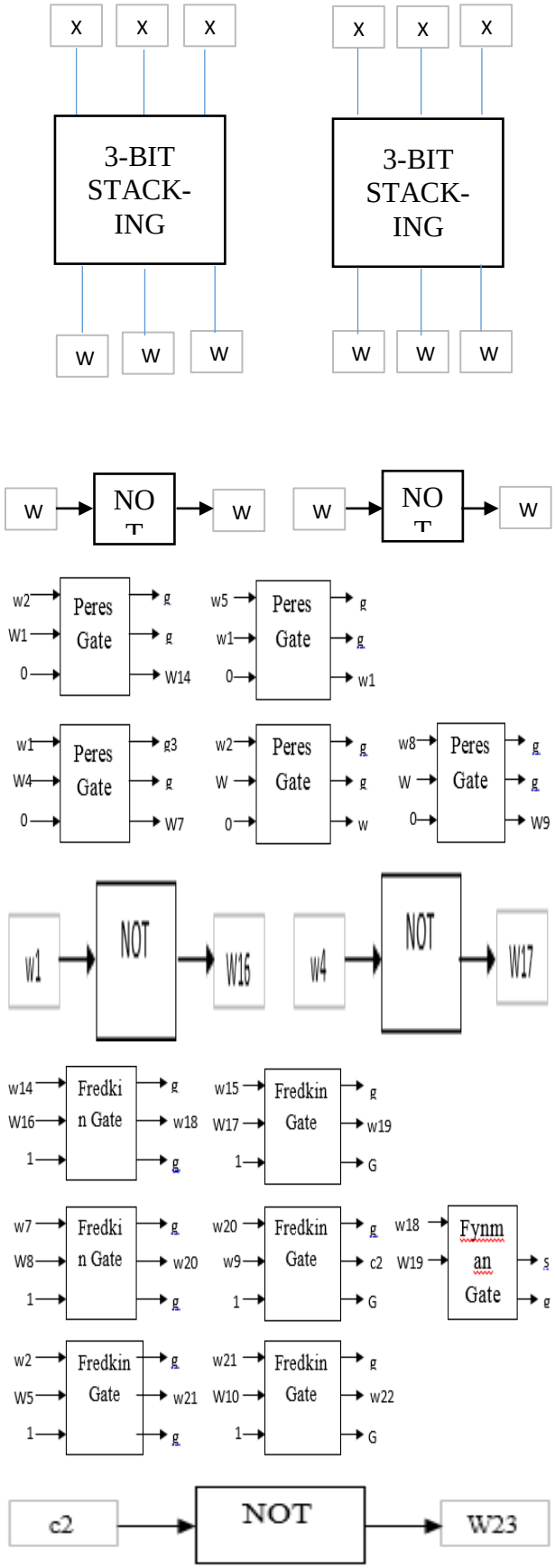


Fig. 10: 6:3 Counter Based on Symmetric Stacking Using Reversible Logic.

The proposed counter circuit uses a total of 37 gates with combinations of Peres, Fredkin and not gates. The total power consumed by the circuit is 3.6904e-04 W. the circuit has been further optimized by replacing Peres gates with Fynman gate.



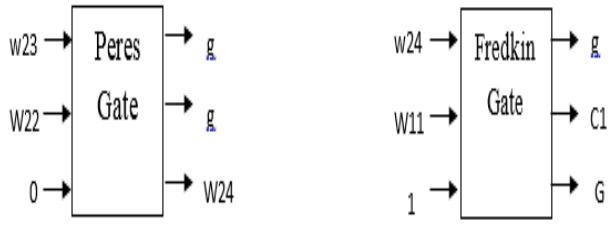


Fig. 11: Optimized 6:3 Counter Based on Symmetric Stacking Using Reversible Logic.

The resultant optimized circuit consumes less power and is also area efficient. The comparison of the power of the circuits mentioned in figures 10 and 11 is depicted below.

Table 2: Average Power Comparison

S. No.	Circuit	Power
1	6:3 Counter based on symmetric stacking using reversible logic (fig. 10)	3.6904e-04
2	Optimized 6:3 Counter based on symmetric stacking using reversible logic (fig. 11)	3.2911e-04

The simulation result of the proposed circuit is shown in figure 12.

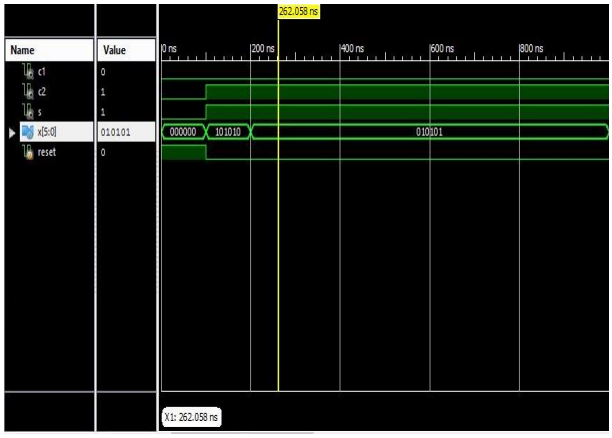


Fig. 12: Simulation Result of the Optimized 6:3 Counter Based On Symmetric Stacking Using Reversible Logic.

5. Conclusion

In this brief, a new binary counter based reversible logic is proposed. We showed that this counting method can be used to implement 6:3 counters, which can be used in any binary multiplier circuit to add the partial products. Heat dissipation is a major problem in the designing of a digital circuit. Rolf Landauer has proved that the information loss in a digital circuit is directly proportional to the energy dissipation. The mathematical formulation of the above statement is that if a bit is lost in a digital system, the amount of energy lost is either equal to or greater than KTln2 joules in the form of heat. To provide a solution to this problem statement, reversible computing was introduced. The proposed 6:3 symmetric staked counters produced expected results and the addition of reversible logic formulation further increased the efficiency.

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