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Research paper

Low leakage SRAM cell for ULP applications

Tripti Tripathi [1] *, D. S. Chauhan [2], S. K. Singh [3]

[1] Inderprastha Engineering College, Ghaziabad
[2] GLA University, Mathura
[3] ABES Engineering College, Ghaziabad
**Corresponding author E-mail: tripti.armaan@gmail.com*

Abstract

Leakage power is becoming a major concern in battery operated and hand held devices. With the ever reducing size of electronic devices and the use of memory in most of them, the need for low power devices is vastly increasing. These devices are either in active or standby mode of operation. Leakage power in standby mode of operation is of major concern and various methods to minimize it have been proposed at various stages of design cycle. This paper proposes fingering technique that can be used in 6T SRAM cell to reduce leakage power. Leakage power is calculated for 6T SRAM cell designed using two fingers in access transistors and on comparison with conventional 6T SRAM cell, significant reduction in leakage current is obtained. The layout has been designed in UMC 55nm technology using Cadence Virtuoso tool and it has been shown that the leakage power and delay can be reduced.

Keywords: *SRAM; Low Power; Leakage Current; Fingering; CMOS.*

1. Introduction

The device size of portable and hand held devices is day by day shrinking which makes the leakage power and battery life a very crucial aspect of electronic devices. Leakage power has been a major issue of concern and will continue to be an important research area as smaller the device size more prominent is the contribution of leakage power in total power dissipation. The requirement is not only of smaller size but also of higher speed, as the speed of microprocessor based devices increases large quantity of data is to be fetched at a very high speed. This makes the design of cache memory an issue of major concern. Mainly Static Random Access Memory (SRAM) is needed for cache memory design. SRAM using Complementary Metal Oxide Semiconductor (CMOS) technology is the preferred choice for cache memory design. There are various configuration of SRAM cell, of which 6T SRAM cell is the most preferred choice due to robustness, low power and low voltage operation [1]. In electronic devices vast majority of memory cells remain in standby mode for large fraction of time [2] so static power becomes more critical for SRAMs. As reported in International Technical Roadmap for Semiconductors (ITRS), transistors devoted to memory structures in microprocessor based system is about 70% today and is expected to increase to 80% in near future [3]. SRAM cell consumes energy in active as well as in standby mode, however standby leakage power becomes more significant for lower technologies. To reduce standby leakage power several techniques have been incorporated in SRAM cell. This paper proposes a modified 6T SRAM cell which has lower leakage current than conventional 6T SRAM cell. Section II describes the various components of leakage current MOS transistor and 6T SRAM cell, section III overviews various leakage current reduction techniques already proposed for 6T SRAM cell, section IV describes proposed technique and finally results are discussed in section V.

2. Leakage components in bulk CMOS and 6T SRAM cell

There are mainly three main components of leakage current when the transistor is in non- conducting state. They are: Sub-threshold leakage current (I_{sub}), gate induced drain lowering current (I_{GIDL}) and punch through leakage current (I_{punch}).Apart from these there are two other components of leakage current which are indepenent of the conduction of device, they are, gate tunneling current and junction reverse bias leakage current due to band to band tunneling.

As the technology scales down, the device parameters like threshold voltage, oxide thickness and channel length are also reduced. Fig. 1 shows the different components of leakage current in MOS transistor.

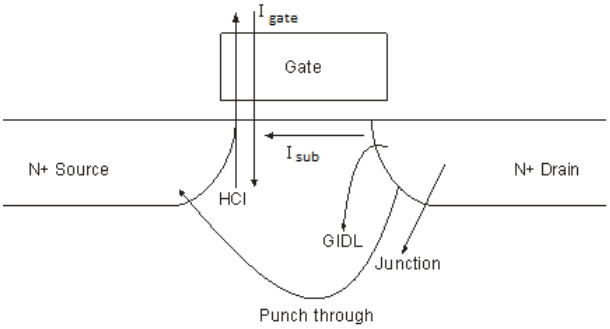


Fig. 1: Leakage Current Components in MOS Transistor.

2.1. Sub threshold leakage current

When the gate voltage of device is lower than its threshold voltage, weak inversion region exists between drain and source region. The

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current flow in this region due to diffusion of minority carriers constitutes sub-threshold leakage current. The reduction in threshold voltage (V_{th}) increases the sub-threshold leakage current exponentially. It increases ten times for every 0.1v reduction in V_{th}.

2.2. Gate leakage current

When the device size is scaled down, the gate oxide this is also reduced, this increases the electric field across the oxide. This high electric field increases the tunneling probability of electron through the oxide hence gate leakage current increases.

2.3. Junction leakage current

The reverse biased junctions are formed between body-drain and body-source junction. These constitute leakage current due to electron hole pair generation and minority carrier diffusion near the edge of depletion region.

Device material technology has managed to keep gate leakage under control by use of high k-dielectrics. Also the junction leakage current is critical mainly for strong reverse biased junctions and reverse biasing is used selectively and with moderate amount of bias for performance reasons, so the major relevant component of leakage current to be considered is sub threshold leakage.

The various leakage current components for 6T SRAM cell are shown in Fig. 2, leakage current occurs when the transistor is off but the drain to source current is non-zero.

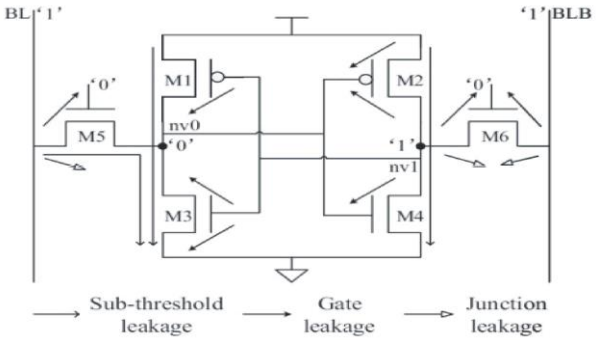


Fig. 2: Leakage Currents in 6T SRAM Cell [5].

6T SRAM cell consists of two inverters connected back to back and two NMOS access transistors, M5 and M6 as shown in Fig.2

The leakage current in SRAM cell depends on

1) the value stored in the cell
2) operation being performed
3) the data value on word line (gate voltage of M5 and M6)

The total leakage current through the cell is sum of sub threshold, gate leakage and junction leakage current.

3. Leakage reduction techniques in 6T SRAM cell

Various techniques for reducing the leakage current have been proposed at different stages of design cycle. Our work is focused on reducing leakage current for core cell during standby mode. Following are few of the existing leakage reduction techniques.

Biasing Techniques: It can be of two types: Reverse body biasing (RBB) or forward body biasing (FBB)[6]. In RBB method, the substrate of PMOS transistor is connected to the voltage higher than supply voltage and the substrate of NMOS is connected to voltage lower than ground voltage, this increases the depletion region width, thereby increasing the threshold voltage. Similarly in FBB, the substrate of PMOS transistor is connected to the voltage lower than supply voltage and the substrate of NMOS is connected to voltage higher than ground voltage, this reduces the depletion region width, thereby decreasing the threshold voltage. RBB reduces leakage current due to increase in threshold voltage. But, the effectiveness of the reverse body-biasing scheme decreases with technology scaling, due to aggravating of the body effect caused by the shorter channel length. In addition, source- bulk, drain-bulk leakage current, band-to-band tunneling current exponentially increase at the source-bulk and drain-bulk PN junctions. Apart from these two, source biasing can also be used to achieve significant reduction in leakage energy without compromising on performance [7].

Dynamic V_{DD}: Leakage current in standby mode can be reduced by reduction in supply voltage. But this may increase delay of the cell so to overcome this normal supply voltage can be used in read/write operation during active mode. However this increases soft error rate and introduces latency in the cell [8].

MTCMOS method: Auto back gate controlled MTCMOS [9] has been presented for low power SRAM design. In this technique circuit is designed using low threshold voltage transistors and in standby mode, high threshold voltage transistors virtually cut off the path for leakage current to flow from the cell hence leakage current is reduced.

Dual V_T and dual t_{OX} technique: In this method, transistors in critical path use low threshold voltage transistors while others are high threshold voltage transistors [10]. So leakage current is reduced and performance of the circuit is also improved.

PP SRAM Bit Cell structure has been presented, where the two high-VT PMOS access transistors [11] replace with NMOS access transistors of 6T SRAM cell. It is based on the view that the gate leakage (gate oxide direct tunneling) current will be lower than that of the leakage offered by the NMOS transistors in the ideal mode of the bit-cell.

Transistor stacking and zig-zag approach: [12]. Stacking of transistors breaks existing transistor into two equal sized transistors thereby introducing reverse bias between them when they are turned off together. This results in sub threshold leakage current reduction.

Fingering technique [13] has been proposed in MOS transistor to reduce leakage current. This technique when used in various transistors of 6T SRAM cell helps to achieve leakage reduction in the memory cell, however if fingering is applied in all six transistors of the memory cell, area will be increased.

This paper proposes the memory cell where two-finger transistors are used only for access NMOS transistors.

4. Proposed SRAM cell

This paper proposes two fingered 6T SRAM cell which can be used for leakage reduction in standby mode of operation. Fingering is layout technique where a single transistor is split into number of parallel transistors having same channel length but reduced width so the gate resistance reduces. It also helps to improve upon noise and delay. It helps to reduce drain and source area and thereby reduce parasitic capacitance. But it may lead to increase in source and drain side wall capacitance. Fig. 3 shows the layout of fingered MOS.

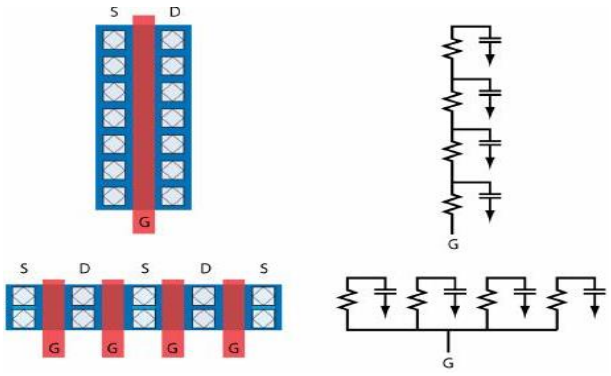


Fig. 3: Layout of [4] Fingered MOS.

The transistor with a width of 20um and a length of 0.2um is similar to having two transistors having length 0.2um and width 10um connected in parallel. So transistor is said to have 2 fingers and if the original transistor is replaced by four transistors having length 0.2um and width 5um connected in parallel, the transistor is said to have 4 fingers. In this paper, two- finger technique has been used in only access transistors of 6T SRAM cell, where as other four transistors that form back to back connected inverters do not use fingered transistors, this is done so as to avoid increase in area of the cell. Leakage current for the cell is calculated and layout has been designed for the proposed SRAM cell and compared with the layout of conventional cell. The use of two finger access transistors helps to greatly reduce leakage current without significant increase in area of the cell.

5. Results and discussion

The schematic for conventional 6T SRAM cell is shown in Fig. 4. It is designed in 55nm UMC technology using cadence virtuoso tool for V_{dd}= 0.6V

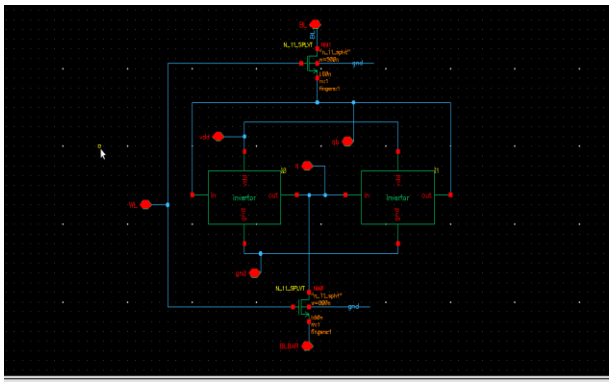


Fig. 4: Schematic for 6T SRAM Cell.

Then the layout for the same is generated and is shown in Fig.5.

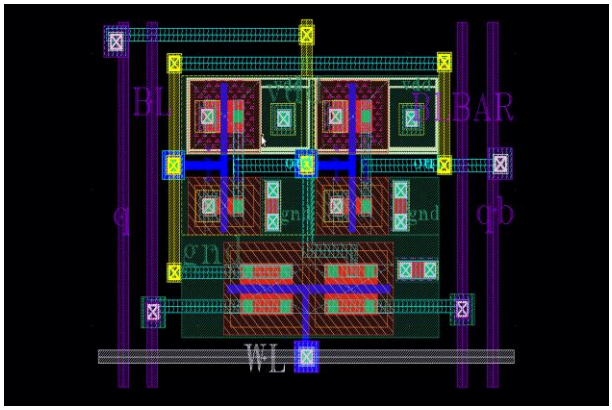


Fig. 5: Layout for 6T SRAM Cell.

In the proposed SRAM cell only access transistors (i.e. M5 and M6) of 6T SRAM cell are replaced with two finger transistors and the layout has been generated. Fig.5 shows the layout for proposed 6T SRAM cell.

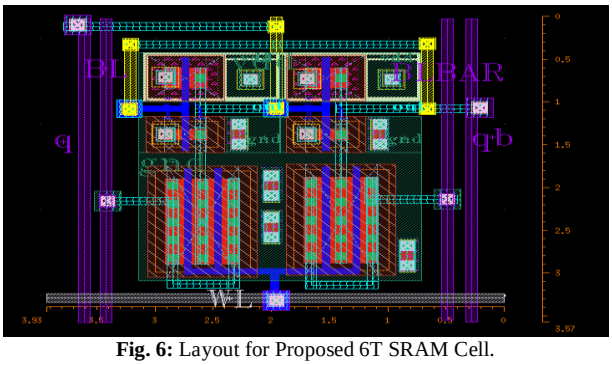


Fig. 6: Layout for Proposed 6T SRAM Cell.

The leakage currents for the conventional 6T SRAM cell and proposed cell are calculated for V_{dd}=0.6V using 55nm UMC technology and significant reduction in leakage current has been obtained. The proposed cell modifies only two NMOS transistors so that leakage current can be reduced without much area overhead. The results obtained are shown in table 1 and they indicate improvement in leakage currents for memory cell designed in 55nm UMC technology

Table 1 shows the comparison of leakage currents and Fig.7 shows the graphical comparison for obtained results.

Table 1: Leakage Current Comparison Table

Technology	55nm UMC technology	
	Conventional SRAM cell	Proposed SRAM cell
Leakage Current	185.57pA	158.33pA
Delay	900.76ns	800.02ns
Area	2.66*3.79u	3.57*3.93u
Vdd	0.6V	0.6V

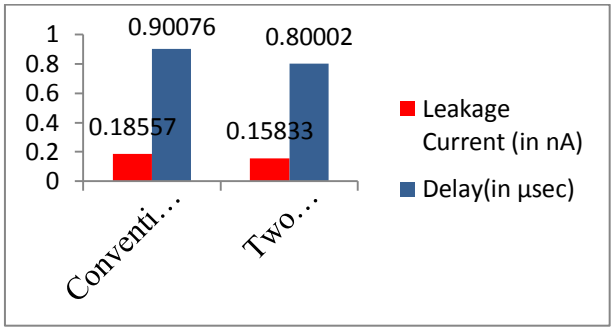


Fig. 7: Comparison of Leakage Current and Delay for Conventional and Proposed 6T SRAM Cell.

6. Conclusion

This paper presents leakage reduction technique for SRAM cell. Leakage current is a cause for major concern in deep submicron technologies and becomes more critical for memory cells. Low leakage current is a major requirement for most of the battery operated and hand held devices so extensive research is being carried to minimize this component of total power consumption. This paper proposes 6T SRAM cell which is designed and simulated using UMC 55nm technology and on comparison with conventional 6T SRAM cell, it has been shown that leakage current can be reduced by 15% while delay is improved by 13%.

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