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Research paper

Survey: Performance Analysis of FIR Filter Design Using Modified Truncation Multiplier with SQRT based Carry Select Adder

U Penchalaiah[#1], Siva Kumar VG[*2]

[1]*Department of ECE, Sathyabama Institute of Science and Technology, Chennai, Tamil Nadu-600119, India;*
[2]*Department of ECE, Vidya Joythi Institute of Technology, Hyderabad, Telengana-5000759, India;*

Abstract

A recent years of technology development in Signal processing application a FIR (Finite impulse response) filter design will have a highly compactable with high performance and low power in all digital signal processing application, such as audio processing, signal processing, software define radio and so on. Now a days in our environment will have more signal noises, and fluctuation due to technology development, here the Filter design is mainly configuring the priority to reduce the signal noises and fluctuation in all type of gadgets. In this project, the design contains Transpose form of high performance and high speed filter design using finite impulse response (FIR) filter with technique of pipelined inherently and supported multiple constant multiplication (MCM) in significant with saving power computation. In digital signal processing, the multiplier is a highly required thing, the example of parallel multiplier provide a high-speed and highly reliable method for multiplication, but this parallel multiplier will take large area and also power consumption. In the FIR filter design, multiplier and adders is the maximum priority will take to give the performance, but this MCM multiplier and Adders tree architecture will take large area and maximum power consumption in signal processing. So our Proposed approach of this work, will have replace the MCM multiplier to Truncated Multiplier and using the technique of Truncated based both Signed and Unsigned Operation with SQRT based Carry Select Adder (CSLA), and also replace the normal adders in FIR Filter to SQRT based Carry Select Adder (CSLA). In the proposed system of FIR Filter design results to be analysis with signed and unsigned Truncation using modified technique of HSCG-SCS based SQRT-CSLA and hence proved its more efficient than existing design, such as FIR filter for Truncation multiplier with SQRT-CSLA based Adders, FIR filter for Truncation multiplier with BEC based Adders, FIR filter for Truncation multiplier with RCA, and FIR filter for Truncation multiplier with Common Boolean logic based RCA, and finally implemented this design on VHDL with help of Xilinx FPGA-S6LX9 and shown the performance of proposed design in terms of delay, area, and power.
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Keywords: *FIR (Finite impulse response), MCM (Multiple Constant Multiplication), CSLA (Carry Select Adder), BEC (Binary Excess Converter), RCA (Ripple Carry Adder), HSCG (Half-Sum Carry Generation), SCS(Sum Carry Selection).*

1. Introduction

In recent digital signal processing applications a FIR Filter design will have a more priority in all the application to meet the efficiency, less area and less power consumption. FIR filter will have highly compactable with high performance in gadgets applications, such as audio and video signal processing, software define radio, telecommunication and so on. In this FIR filter is very often and need to support in digital signal processing to high sampling range, impulse response based filtering order and cut-off frequency. In this FIR filter design, will have number of adders, multipliers and delayed element required to response filter output. An FIR filter is not required a feedback based inputs, which means, this filter is not computed any rounding errors in summing and multiplication.An FIR Filter is inherently stable to produce output values and it can be no maximum value impulse response Nth order times, it can easily design and also easily configure sequence of linear phase coefficient, it will also applicable to detect and also easily configure sequence of linear phase coefficient, it will also applicable to detect the phase sensitive application such as crossover filter design, mastering, seismology and data communications. In this filter to meet the coefficient specification in certain things, which can be suitable with time domain and frequency domain. The main disadvantages of FIR filter design and more power consumption and larger area size is required for multipliers, adders and delayed element in number of Nth order.

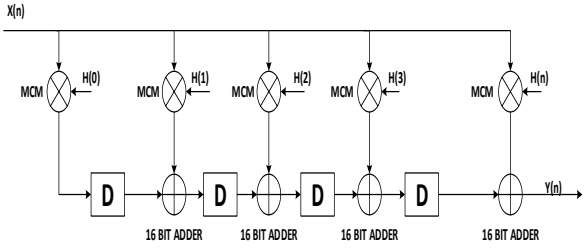


Figure 1: FIR Filter Design with MCM and 16-Bit Adder

In the High performance FIR Filter architecture will have MCM multiplication and normal adders will perform inherently pipelined and also produced the results on significant way with save computation results. In the FIR Filter design will take large area and also take the stringent order to meet frequency range with high performance. In the Fig.1 architecture will have to used

MCM(Multiple constant multiplication), adders and delayed element, here the MCM multiplier will not identified the method of signed and unsigned operation, this multiplier will configure either signed or unsigned. In the FIR filter Nth order of the filter increases, a efficiency of FIR will increases, then the number of addition and multiplication required get increased. For the efficient realization of FIR filter i) Distributed Arithmetic (DA) and ii) Multiple Constant Multiplication (MCM) methods are used. In DA-design, to reduce the computation lookup tables are used for the storage of pre-computed results. In MCM method, the additions required for computation get reduce and it is more effective because it uses common sub-expression sharing [1]. This method of blocks is formed only in transpose form and it is suitable for large order filter implementation with fixed co-efficient.

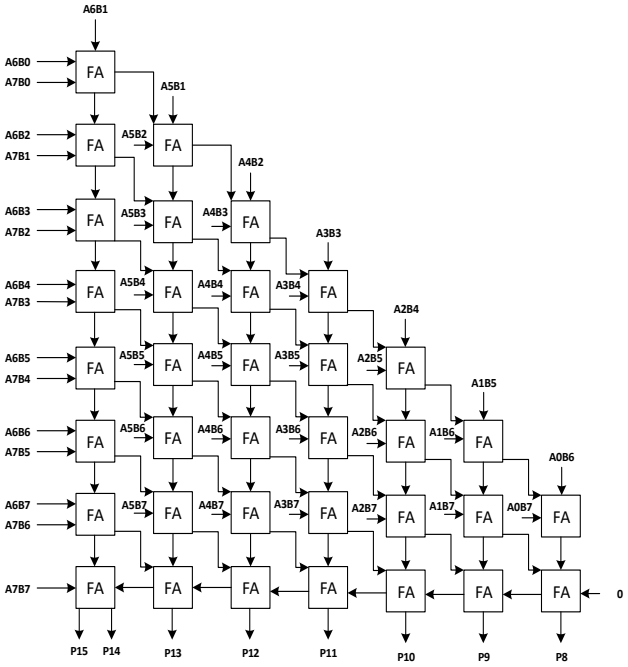


Figure 2: Architecture of Truncated 8x8 Multiplier

Fig.2 shown Full adder based Truncation Multiplier design its contain the architecture after the operations of Unnecessary, Partial Product, Deleted and Rounding from the partial product multiplier of 8x8bits, after the truncated partial products value only given as a input of this architecture, and these operation is based upon full adder, it will separate group by group, the truncated partial produce the design will make this kind of architecture, P8, P9, P10, P11, P12, P13, P14, P15 is the output of this architecture, this output is based upon the MSB bits of normal multipliers.

In the Proposed work of this paper, a modified new adder design is required, it will consume less area and less power consumption and also it will take more efficiency compare to previous adders using Truncation multiplier. The drawback of FIR filter design is large area and more power consumption, because it uses impulse response of Nth order based circuit, its contain multiplier, adder and delayed element, here the proposed thing is modified this adders, multiplier using HSCG-SCS Unit based SQRT method of Carry select adder with the technique of truncated and partial product reduction method. This proposed work to be analyze to multiple of adder with this Truncated FIR Filter, finally choose, the best proposed truncated adder, with low area and less power consumption, the list of possible comparison adder is provided below,

1. Common Boolean logic Based Carry Select Adder
2. Conventional RCA based Carry Select Adder
3. Conventional RCA with BEC based Carry Select Adder
4. SQRT based Carry Select Adder

In this paper, our aim to reduced the area size and power consumption of adder design and to be implement on Fig.2 architecture of Truncated multiplier and replace the number of full adders and finally shown the efficiency and comparison of all adder designs. Section II presents details survey of adder. Section III presents a proposed adder design and comparison of all adders. Section IV describe the existing and proposed Truncated Multiplier, and provide the detailed architecture of modified Truncation architecture. Section V presents a results of area, power and delay. Finally the conclusion in drawn in Section VI.

2. Survey of CSLA Adder Designs

Any digital systems are meant to perform a wide variety of functions or tasks. Among those several functions or tasks, addition is one of the most basic and primary operation of any digital systems, or any digital signal processing unit (DSP) or any control system. The swift and absolute operations of any digitally controlled system is vastly influenced by the type of adders used in the design. Adder are the most crucial component in all digital signal processing design in present days we have various kinds of adders such as Ripple carry adder, carry look ahead adder, carry bypass adder, carry select adder and still many more. Therefore adders are very much required an forms a unavoidable component in almost each and every digital system because of their overall usage in other basic digital operations such as -division, multiplication and subtraction.

A. Basic Adder design:

Addition is one of the most basic and primary arithmetic operation which adds the two binary (1,0) digits. A circuit is said to be combinational circuit when it adds the two binary bits, according to the example demonstrated below, is called a half adder. A circuit that sums three bits, the third bit generated from the summation of previous least significant bit(LSB), these type of circuits are known as full adder circuits. Full adders circuits are constructed by making use of two half adders circuit for its implementation. Full adder is the fundamental unit of addition employed in all the adders discussed here.

B. Binary Addition:

The Binary adder design starts by considering the process of summation in base 2 and is as demonstrated in the below example, the two numbers are taken to be added are 11 and 9 in decimal whose binary representation are given as 1011 and 1001 respectively. When the two binary numbers are added. The carry generated from the least significant bit are written on the top of the next corresponding bit. The final result we obtained is the 5-bit binary number 10100 which is equivalent to 20 in decimal representation. From demonstration, we notice that the issue of summing the two 4-bit numbers can be minimized by adding a column of as many number of bits present and passing the carry (if generated) to the next of the problem of adding a column of two or three bits and passing the carry to the next corresponding column.

(10111011 = 11) + (1001 =09) = (10100 = 20)

C. Basic 1-Bit Half adder design:

A half adder is a very simple and basic combinational architecture circuit. A half adder is a circuit which sums two bit. A half adder executes an operation of addition on two 1-bit binary numbers. The half adder produces the outputs which is a sum of the two input bits along with its carry if generated. A half adder circuit contains two bits as an input which are usually denoted as A and B and two bits as output known as sum and carry which are usually denoted by S and C respectively. The output Sum(S) is a two bit XOR of input bit A and input bit B. The output Carry(C) is a AND of input bit A and input bit B. Necessarily the half adder produces an output which is the sum of the two 1-bit numbers and the carry(C) is obtained at the most significant bit(MSB) if the sum of each individual bit produces a carry. Half adder circuits are fairly

very easy and simple to construct but it has its limitations, the drawback is cannot hold on or to include a carry when a multi-bit operation needs to performed. The Boolean equations for half adder are as given below.

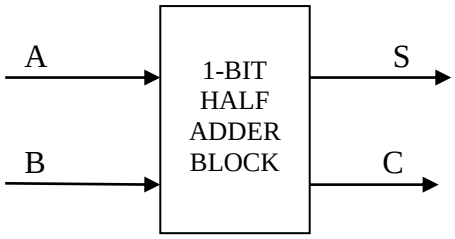


Figure 3: 1-bit Half adder

bit A and input bit B. The output Carry(C) is a AND of input bit A and input bit B. Necessarily the half adder produces an output which is the sum of the two 1-bit numbers and the carry(C) is obtained at the most significant bit(MSB) if the sum of each individual bit produces a carry. Half adder circuits are fairly very easy and simple to construct but it has its limitations, the drawback is cannot hold on or to include a carry when a multi-bit operation needs to performed. The Boolean equations for half adder are as given below.

S = A XOR B
C= A AND B

The half added circuit diagram along with its truth table are shown in below Fig.5, Table.1.

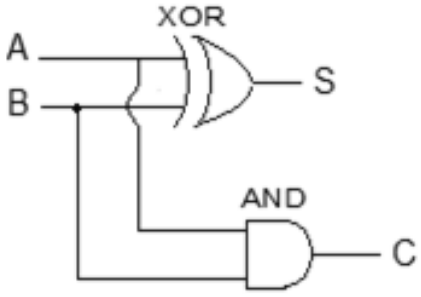


Figure 4: Circuit design of 1-Bit Half Adder

Table 1: Truth table of 1-Bit Half adder

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

D. Basic 1-Bit Full adder design:

The full adder circuits are employed to overcome the drawback associated with half adder circuit. The full adder circuit is a combinational arithmetic circuit which is used to carry out the summation of three bits (A, B and CIN). The full adder generated the corresponding output as Sum(S) and Carry(COUT) which is as similar to the half adder circuit. The full adder may be constructed by cascading two half adders which is as shown in Fig.5. The summation of input bits A and B are give directly to the second half adder, where first summation output adds a carry CIN if a carry is generated from the previous summation of LSB operation and then finally its generates a output sum value. The carry-out is obtained from the results of an OR operation derived from the carry output from the both half adders. Both at the gate level and the transistor level there are plenty of adders architecture each one exhibits different parameters. The Boolean equations for half adder are as given below.

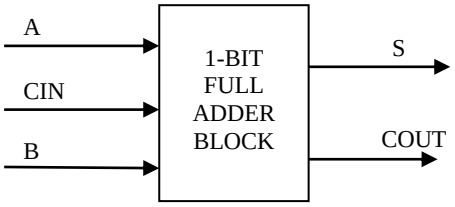


Figure 5: 1-bit Full adder Block

S = CIN XOR (A XOR B)
COUT = (A AND B) OR (CIN AND S)

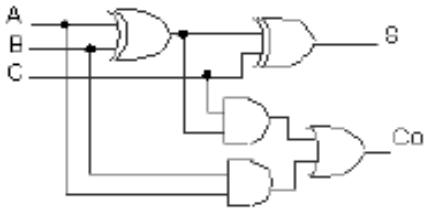


Figure 6: Circuit design of 1-Bit Full adder

The full adder circuit diagram along with its truth table are shown in below Fig.6, Table.2.

Table 2: Truth table of 1-Bit Full Adders

Inputs			Outputs	
A	B	CIN	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

E. Types of Adders:

There are various kind of adders are available in today's technology and main category of two adder will take a decision in digital signal processing application such as,

- Conventional or parallel adders
- Parallel Pre-fix adders

The classification of conventional or parallel adders are given below,

- Ripple carry adder (RCA)
- Carry Select Adder(CSLA)
- Carry look ahead adder (CLA)
- Carry by-pass adder(CBA)
- Carry Save Adder(CSA)

The classification of parallel prefix adder are widely classified as follows,

- Konge stone adder (KSA)
- Brent-Kung adder(BKA)
- Lander-Fischer adder(LFA)

In this work, we mainly focus on the Carry select adder in Conventional or parallel adders with different operation such as.

- Conventional RCA based Carry Select Adder
- Conventional RCA with BEC Based Carry Select Adder
- Common Boolean logic based Carry Select Adder
- SQRT based Carry Select Adder

The detailed explanation of these Carry select adders are given along with their characteristics and performance parameters. For the same size of binary bit, each and every above mentioned adder has unique performance characteristic in terms of its power, delay and area.

1) Conventional RCA Based Carry Select Adder:

In Fig.7 Shown the architecture of Single bit Conventional RCA based Carry Select Adder design, this structure will have two RCA blocks, a first block will used to add inputs value of a, b, c, d, a second block will used to add the carry bit of '1'. Multiplexer to be used to switch the output of'0' carry addition and '1' carry addition based upon input CIN, if CIN='0' the output will present on '0' carry addition, if CIN='1' the output will present on '1' carry addition.

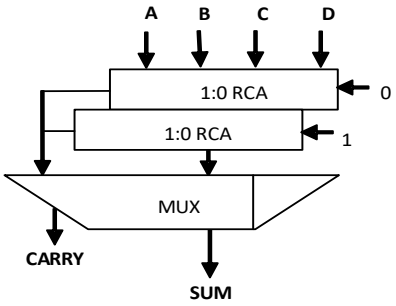


Figure 7: RCA Based CSLA Design

A Gate level structure of Conventional RCA Based Carry select adder design will shown in Fig.8. In this Fig Shown XOR, AND, OR gate based structure, it will take totally 10 logic gate and 1 multiplexer. The truth table of Conventional RCA Based Carry select adder will shown in Table.3.

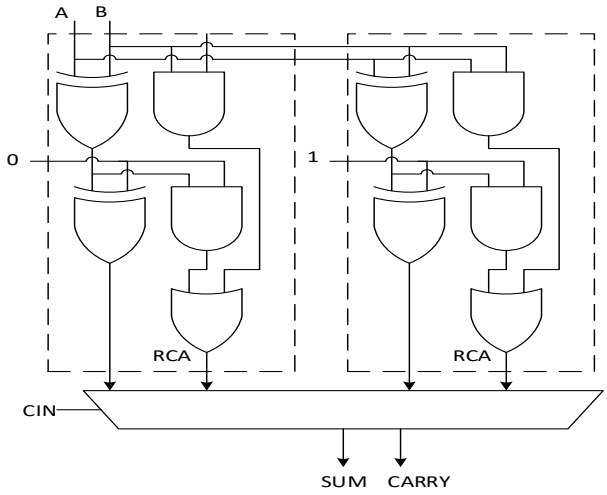


Figure 8: Gate level Structure of RCA Based CSLA

Table 3: Truth Table for RCA Based CSLA

RCA CIN	RCA CIN	A	B	RCA1 CARRY	RCA1 SUM	RCA2 CARRY	RCA2 SUM	CARRY	SUM
0	1	0	0	0	0	0	1	0	0
0	1	0	1	0	1	1	0	0	1
0	1	1	0	0	1	1	0	0	1
0	1	1	1	1	0	1	1	1	0
0	1	0	0	0	0	0	1	0	1
0	1	0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	0	1	0
0	1	1	1	1	0	1	1	1	1

2) Conventional RCA with BEC Based Carry Select Adder:

In Fig.9 Shown the architecture of Single bit Conventional RCA with BEC based Carry Select adder design, this structure will have RCA and BEC blocks and Multiplexer, a RCA block will used to add the inputs value of a, b, c, d, and a BEC block will used to add the sum of RCA and carry '1' bits, the output of BEC and RCA will present as a input of Multiplexer, a Multiplier will switch a signal based upon input CIN, if CIN='0' the output will present on RCA, if CIN='1' the output will present on BEC.

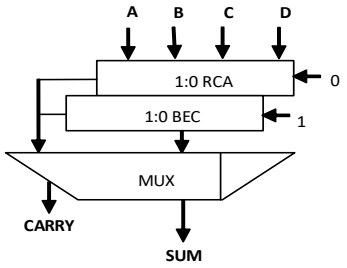


Figure 9: RCA and BEC Based CSLA Design

A Gate level structure of Conventional RCA with BECadder design will shown in Fig.10. In this Fig Shown XOR, AND, OR , NOT gate based structure, it will take totally 7 logic gate and 1 multiplexer. The truth table of Conventional RCA Based Carry select adder will shown in Table.4.

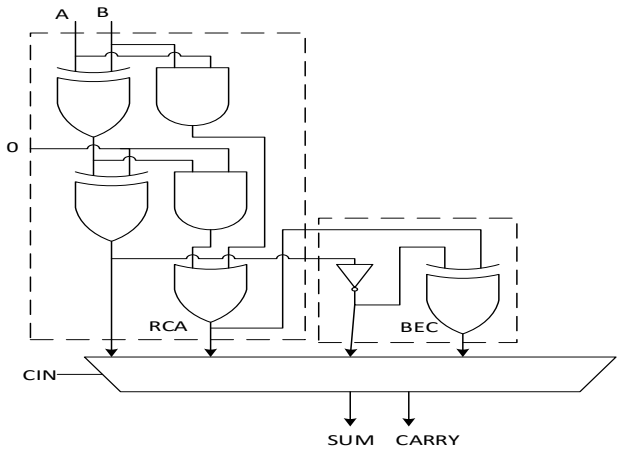


Figure 10: Gate level design of RCA with BEC CSLA

Table 4: Truth table for RCA with BEC CSLA

RCA CIN	BEC CIN	A	B	RCA CY	RCA SUM	BEC CY	BEC SUM	CARRY	SUM
0	1	0	0	0	0	0	1	0	0
0	1	0	1	0	1	1	0	0	1
0	1	1	0	0	1	1	0	0	1
0	1	1	1	1	0	1	1	1	0
0	1	0	0	0	0	0	1	0	1
0	1	0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	0	1	0
0	1	1	1	1	0	1	1	1	1

3) Common Boolean Logic based Carry Select Adder:

In Fig.11 Shown the architecture of Single bit Common Boolean logic based Carry Select adder design, this structure will have RCA and CBL blocks and Multiplexer, a RCA block will used to add the inputs value of a, b, c, d, and a CBL block will used to add the sum of RCA and carry '1' bits, the output of CBL and RCA will present as a input of Multiplexer, a Multiplier will switch a signal based upon input CIN, if CIN='0' the output will present on RCA, if CIN='1' the output will present on CBL.

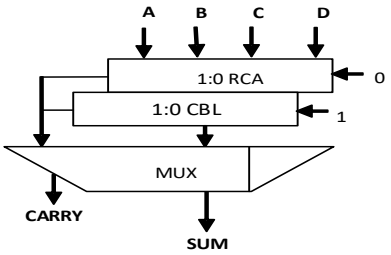


Figure 11: CBL Based CSLA Design

A Gate level structure ofCommon Boolean logic based Carry Select adder design will shown in Fig.12. In this Fig Shown XOR, AND, OR, NOT gate based structure, it will take totally 9 logic gate and 3 multiplexer. The truth table of Common Boolean logic Based Carry select adder will shown in Table.5.

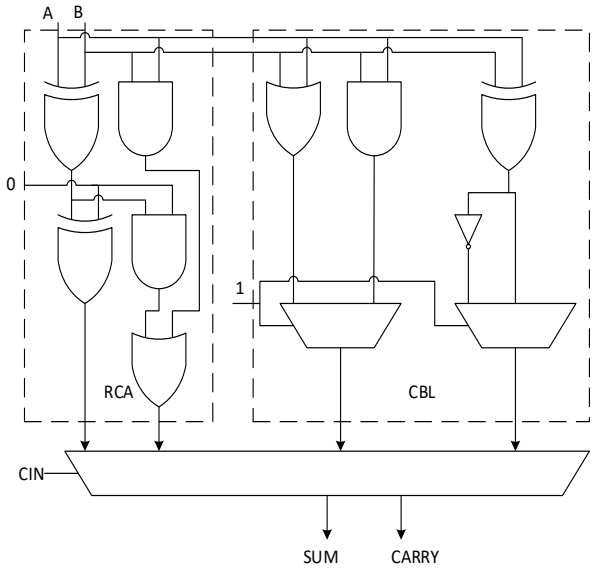


Figure 12: Gate level Design of CBL based CSLA

Table 5: Truth table for CBL based CSLA

RCA CIN	CBL CIN	A	B	RCA CY	RCA SUM	CBL CY	CBL SUM	CARRY	SUM
0	1	0	0	0	0	0	1	0	0
0	1	0	1	0	1	1	0	0	1
0	1	1	0	0	1	1	0	0	1
0	1	1	1	1	0	1	1	1	0
0	1	0	0	0	0	0	1	0	1
0	1	0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	0	1	0
0	1	1	1	1	0	1	1	1	1

4) SQRT-HSG Based Carry Select Adder:

In Fig.13 Shown the architecture of SQRT-HSG Based Carry Select adder design, this structure will have HSG Unit (Half sum generation), CG, CS, FSG Unit (Full sum generation). The HSG unit will have a functionality of Half adder design it will add the inputs of a, b, c, d. The CG unit will have a two modules is receive s0 and c0 output from HSG unit the CG module will have CG0 and CG1 its corresponding to add input carry '0' and '1'. The CS unit will select one final carry from CG0 and CG1 as its inputs line using the control signal CIN. FSG unit will have a functionality of Full adder design it will add the inputs of CIN and output of CS unit.

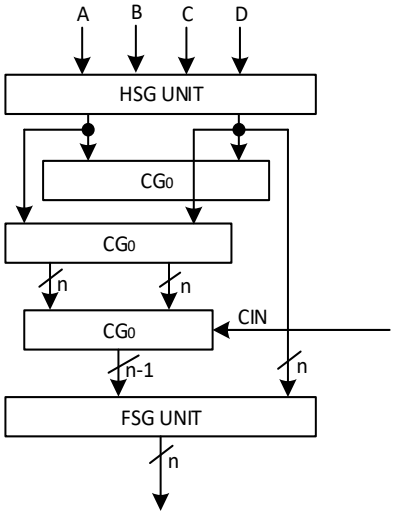


Figure 13: SQRT Based CSLA Design

A Gate level structure ofSQRT based Carry Select adder design will shown in Fig.14. In this Fig Shown XOR, AND, OR, NOT gate based structure, it will take totally 7 logic gate. The truth table of SQRT Based Carry select adder will shown in Table.6.

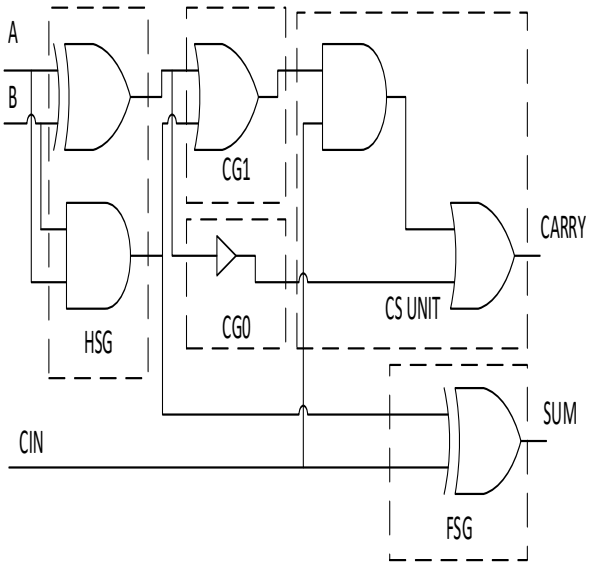


Figure 14: Gate level design of SQRT Based CSLA

Table 6: Truth table for SQRT based CSLA

CIN	A	B	HSG CARRY	HSG SUM	CG0	CG1	CS	FSG
0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0	1
0	1	0	0	1	0	1	0	1
0	1	1	1	0	1	1	1	0
1	0	0	0	0	0	0	0	1
1	0	1	0	1	0	1	1	0
1	1	0	0	1	0	1	1	0
1	1	1	1	0	1	1	1	1

2. Proposed Adder Design

A Modified Structure of Proposed SQRT Carry select adder design will have a HSCG Unit (Half Sum Carry Generation) and SCS Unit (Sum carry generation), it will help to process N number of addition, using XOR, AND, OR Gate's. These design will reduction of number of logic gate's will have compared to Ripple carry addition, and existing SQRT CSLA Design. Here HSG will provide the three outputs, such as operation of XOR, AND, OR Gates, the input CIN will select the Sum and Carry using Multiplexer. Here CIN=0 the multiplexer will select Sum of XOR outputs, and Carry of AND outputs, if CIN=1 the multiplexer will select Sum of Inverted XOR outputs, and Carry of OR Gate outputs. The architecture of Proposed SQRT based Carry select adder design will shown in Fig.15.

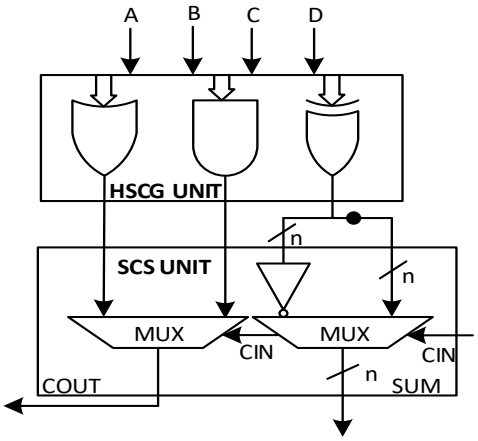


Figure 15: Proposed SQRT-CSLA Design

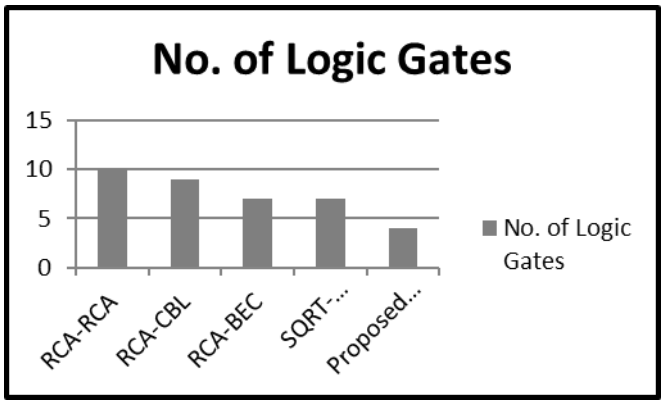
Table 7: Truth Table of Proposed SQRT CSLA

CIN	A	B	XOR	~XOR	OR	AND	SUM	CARRY
0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**0**	**1**	**0**	**1**	**0**
0	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**
0	**1**	**1**	**0**	**1**	**1**	**1**	**0**	**1**
1	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**
1	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**1**
1	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**
1	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**1**

Table 7, will have shown input and output values of SQRT CSLA using HSCG – SCG unit adder design. Here the Multiplier selection will have happened from input of CIN, If CIN = 0, the SUM Operation will get the input from XOR Gate, and Carry operation will get the input from AND Gate, Once the CIN will goes high, the Multiplexer will switch the inputs, the SUM Operation will get the input from inverted XOR Gate, and Carry operation will get the input from OR Gate, here sharing process will have happen based upon CIN Inputs. This Corresponding architecture gate count will take only Four logic gates and two multiplexers.

Table 8: Comparison of all CSLA Single Bit adders

Adders	No. of Logic Gates	No. of Multiplexer	LUT	Occupied Slices	IOB	Delay (ns)
RCA-RCA	10	1	1	1	5	6.11
RCA-CBL	9	3	1	1	5	6.11
RCA-BEC	7	1	1	1	5	6.11
SQRT-CSLA-HSG-CS-FSG	7	0	1	1	5	6.11
Proposed SQRT-HSCG	4	2	1	1	5	6.11



3. Proposed Truncation Multiplier

A Multiplier is more important in today technology such a application of digital signal processing, image processing and cryptography application method, since this all application is a most high priority in today technology such as 3G, LTE, Telecommunication, audio and video processing and so on. In this DSP application, the multiplier is the main priority to reduce signal noise, fluctuation in all type of gadgets. In this method of truncated architecture is fully designed based on full adders, here carry operation is followed as per the same operation of sum, based upon this architecture it will take more critical path delay, propagation delay, and its perform slowest operation of arithmetic functions. A goal of this truncated multiplier is to reduce the large area in the internal and external architecture using rounded based technique, which computed the truncation multiplier will have summing the two n-bit partial products, this operation of two n-bits, the MSB of most significant rows and columns with truncated, deleted and rounding to correction in variable method. A normal multiplier of n x n bit computes and get the weighted sum of output of 2n bits. A multiplier in signal processing the output represented the MSB part of n bits is useful, because it's signed oriented outputs, example of this design such as digital signal based application.

A truncated multiplier is a hardware efficient multiplier, it will useful to increases the tradeoff accuracy and reduced the hardware cost, since this truncated multiplier will help to produce the output of n-bits form n x n bits of multiplication, it will take less significant, and some of the partial products are removed and also replace using the technique of deletion, reduction and truncation.In the partial products of this multiplier more number of columns are eliminated regarding the area and power consumption, in case the delay also decreases with compare to the normal operation of 2n outputs of n x n multiplier, but some drawbacks will have on this truncated multiplication, because this multiplier is not concentrated on carry operation, such as carry addition and carry skip operation, here used number of full adders for addition, but not implemented the simple and efficient gate level implementation with carry operation to significantly reduced the area, power and delay.

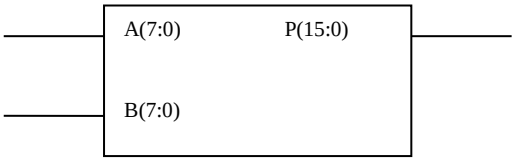


Figure 17: Block Diagram of Standard 8x8 Multiplier

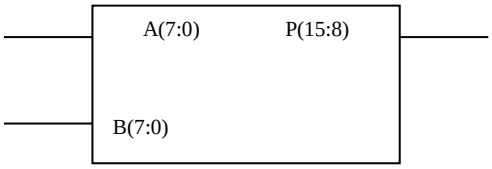


Figure 18: Block Diagram of Truncated 8x8 Multiplier

F. Proposed Structure of Truncated FIR filter design:

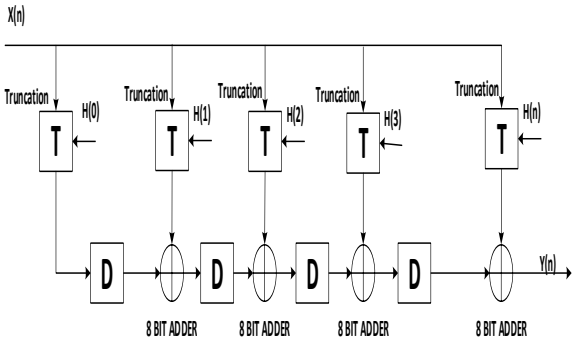


Figure 19: Proposed FIR Filter Design with Truncation Multiplier

An FIR filter it not required a feedback based inputs, which means, this filters is not computed any rounding errors in summing and multiplication. An FIR filter is inherently stable to produce output values and it can be no maximum value impulse response Nth order times, it can easily design and also easily configure sequence of linear phase coefficient, it will also applicable to detect the phase sensitive applications such as crossover filter design, mastering, seismology and data communications. In this filter to meet the coefficient specification in certain things, which can be suitable with time domain and frequency domain. The main disadvantages of FIR filter design are more power consumption and large area size is required for multipliers, adders and delayed element in number of Nth order based TAP. In the High performance FIR Filter architecture will have MCM multiplication and normal adders it will perform inherently pipelined and also produced the results on significant way with save computation results. This MCM multiplier will not identified the Signed and Unsigned operation of inputs, and not concentrate on Carry operation inside of Partial Product Addition. In the FIR filter design will take large area and also take the stringent order to meet frequency range with high performance.

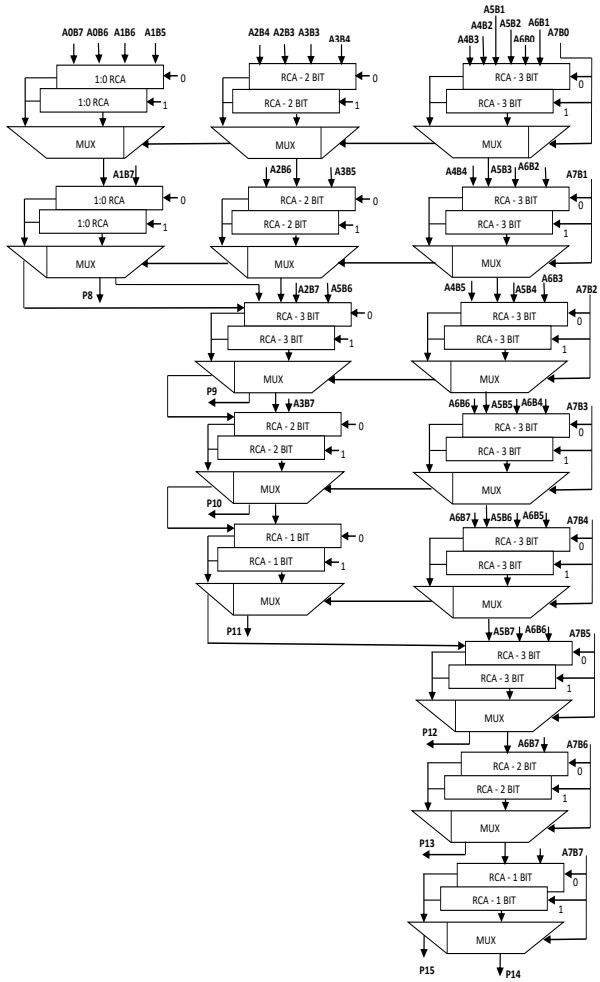


Figure 20: Truncation Multiplier architecture using Conventional RCA based CSLA

In Fig.19 of Truncation Multiplier will have RCA based CSLA design, normally the truncated will designed on full adder, based upon this modification conventional carry select adder will perform high speed operation in carry addition process, it will take less area and power consumption compared to normal full adders, so the overall process of FIR filter design with truncated will take high performance and better results. In the proposed system of FIR Filter design results to be analysis with Truncated conventional carry select adder is better than the regular FIR Filter design, and also shown the performance of proposed design in terms of delay, area, and power.

4. Results and Adder Implementation

A. Results of RCA Based CSLA Design

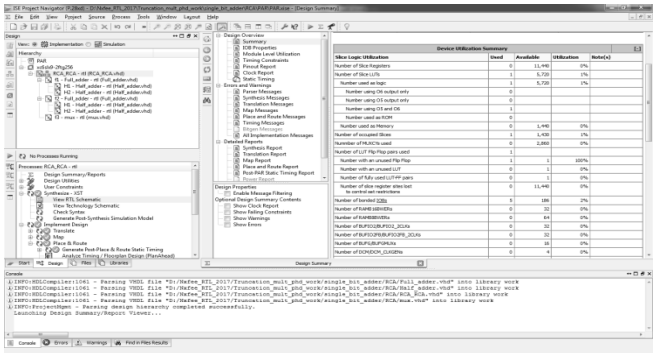


Figure 21: Synthesize report of RCA based CSLA

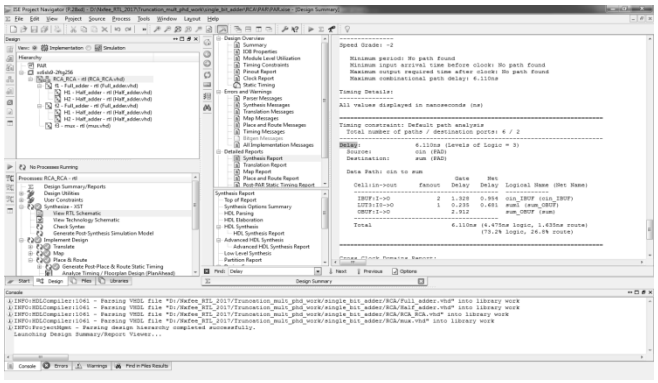


Figure 22: Delay report of RCA Based CSLA Design

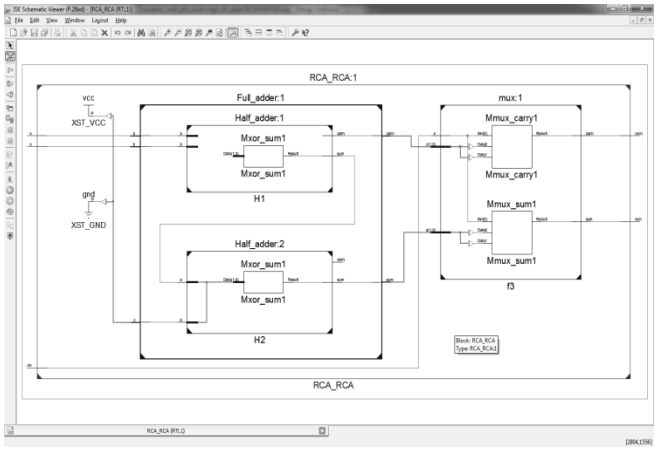


Figure 23: RTL Design of RCA Based CSLA Design

B. Results of RCA Based BEC Design

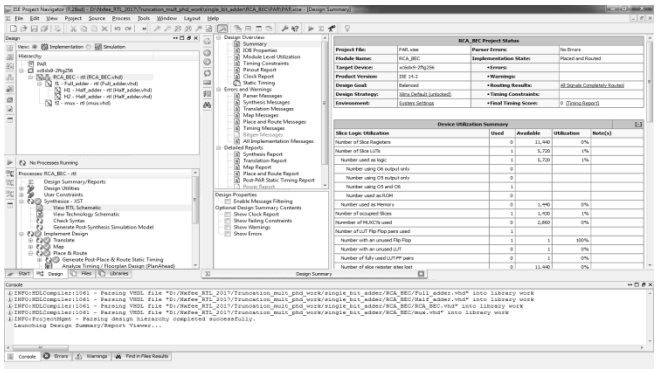


Figure 24: Synthesize report of RCA Based BEC

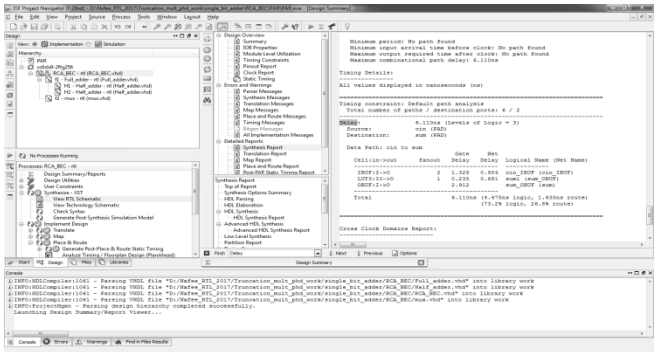


Figure 25: Delay report of RCA Based BEC

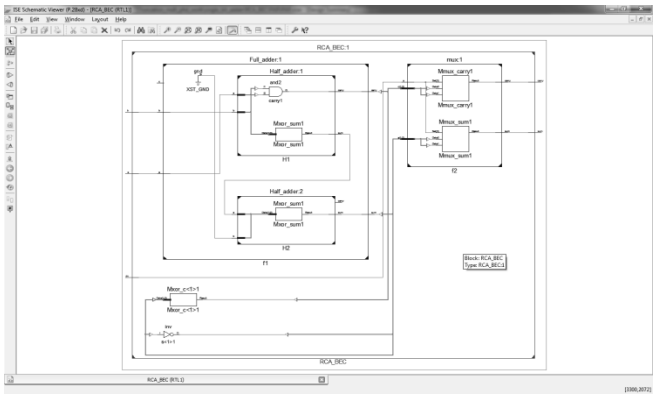


Figure 26: RTL Schematic for RCA Based BEC

C. Results of RCA Based CBL Design

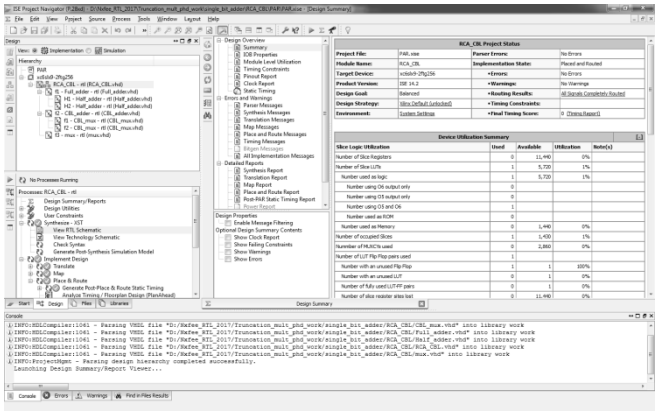


Figure 27: Synthesize report of RCA Based CBL

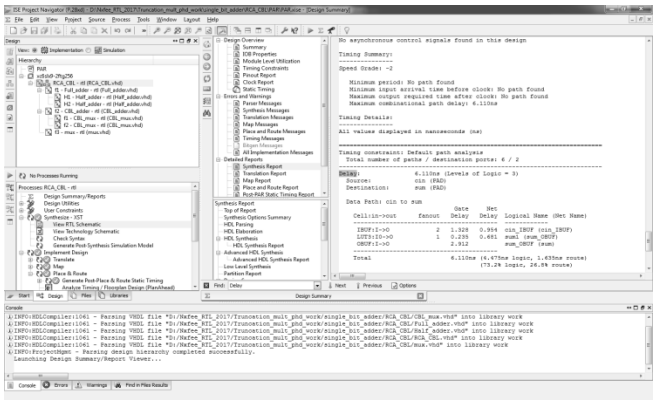


Figure 28: Delay report of RCA Based CBL

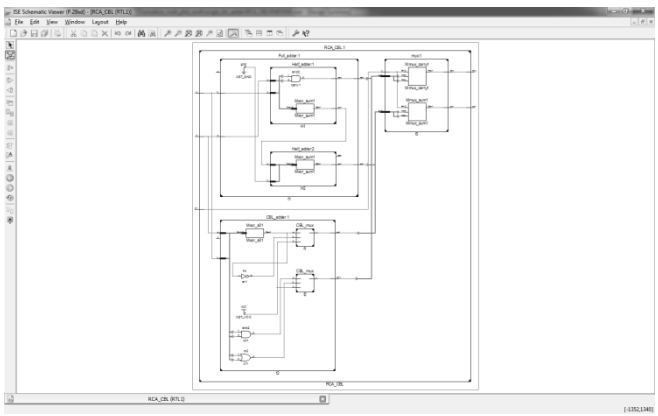


Figure 29: RTL Schematic of RCA Based CBL

D. Results of SQRT based CSLA Design

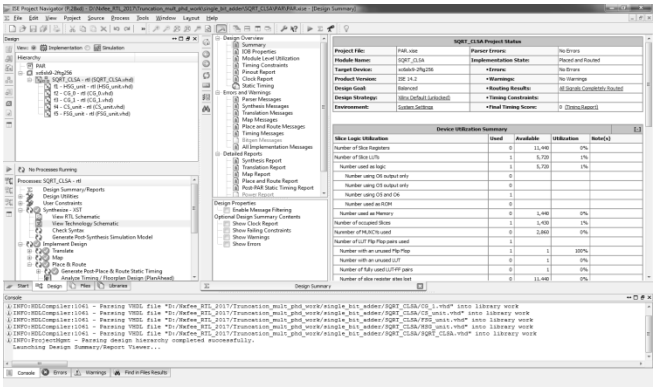


Figure 30: Synthesize report of SQRT based CSLA Design

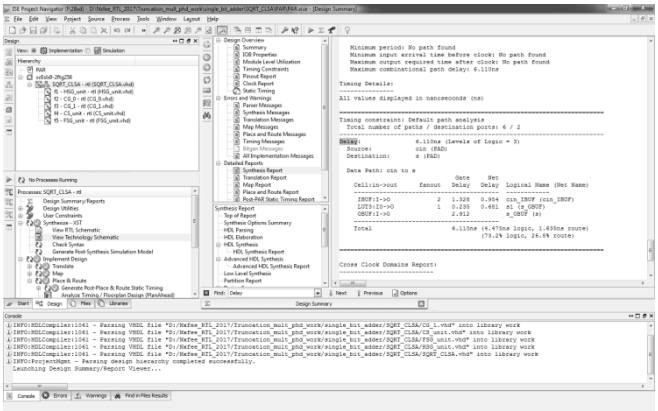


Figure 31: Delay report of SQRT Based CSLA

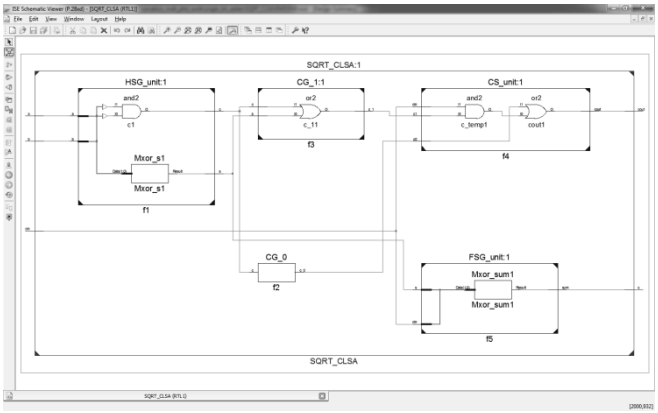


Figure 32: RTL Schematic of SQRT CSLA Design

A. Proposed design of SQRT CSLA-HSCG and SCG based adder design:

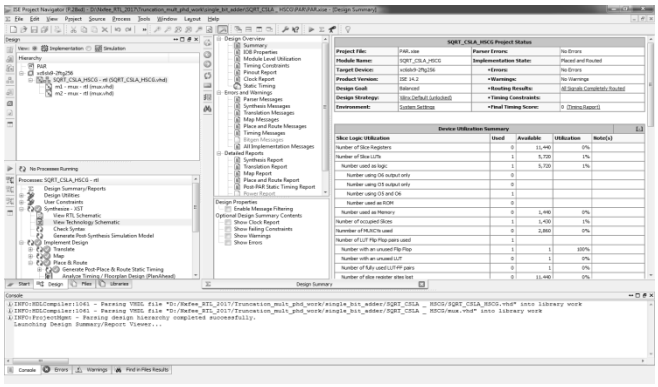


Figure 33: Synthesize report of Proposed adder design

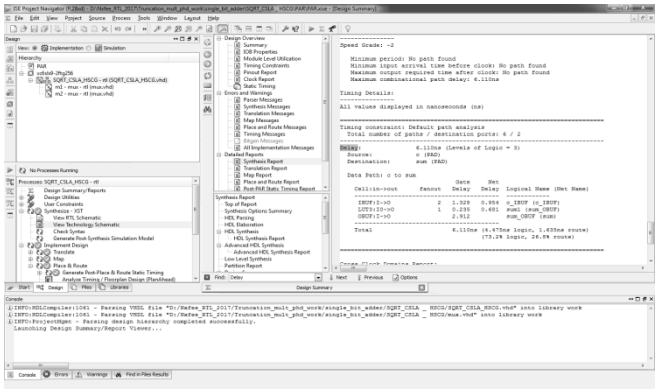


Figure 34: Delay report of Proposed adder design

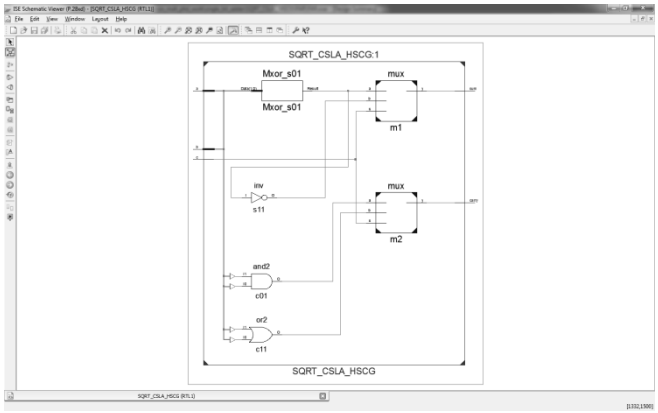


Figure 35: RTL Schematic of Proposed design

5. Conclusion

In this paper we have surveyed a multiple of CSLA adder design and finally proposed a modified structure of SQRT-CSLA-HSCG-SCG based adder design, this adder will compared to different types of CSLA and adder and hence proved the area, delay and power. This design will aim to reduced the area, delay and power size in all the digital signal processing application included with FIR filter design, the future work to be implement this proposed adder to implement a truncated multiplier and also replace a structure of FIR filter with this adder and multiplier, and proved the efficiency of this adder design. Here, this adder will implemented on VHDL, and synthesized on Xilinx S6lx9 FPGA, and finally proved with compression of reduced LUT size, Slice registers, delayand power of all adders.

6. Literature Survey

Survey -1

B. Ramkumar, Harish M Kittur, 2011 IEEE, discussed about the fast arithmetic operations using to design adders. In Carry select adder is a one of the design of fast arithmetic functions. In the Architecture of Carry select adder to significantly have large area to be reduced, and also power consumption. The proposed architecture of SQRT based CSLA will modified 8-, 16-, 32- and 64bit square root Carry Select adder architecture with compare to the regular Carry Select adder, it will show high performance in area, power and delay, this architecture of SQRT BEC based CSLA will design it will reduce the area, power and delay.

Survey -2

Suresh R.Rijal, Ms.Sharda, G. Mungale, 2013 discussed about the Multipliers is mostly required in DSP (digital signal processing) application. In the design of parallel multipliers to provide an efficient output high speed multiplication, but it will take large area and power consumption. In the recent technology of digital signal processing application, a partial product is rounded and also avoid the growth in the size of multiplier. In this proposed work of this paper, is reduced the area of partial product rounded truncated multiplier, and it computes the two n-bit numbers to produce n-bit outputs regarding summing MSB bits with variable correction methods. Its Significantly reduced the area and power consumption instead of standard multiplier.

Survey -3

Basant Kumar Mohanty, SujitKumarPatel, 2014 discussed about the operation of adder in the signal processing application, the carry select adder is mostly involved with data dependence and also to identify the arithmetic logic operation. In this Carry select adder will have lot of methods. In this proposed architecture of this design consider will approach different from of conventional approach, it will reduce and optimized logic units. The proposed SQRT based carry select adder will design using HSG (Half Sum Generation), FSG (Full Sum Generation), CG (Carry Generation), CS (Carry Selection) based design it will provide the performance of less area, and less delay and also less bit widths.

Survey -4

Basant Kumar Mohanty, Pramod Kumar Meher, 2015 discussed about the FIR Filter design in Fixed and Reconfigurable method of application, this FIR filters are support inherently pipelined multiplication, such as Multiplier constant multiplication (MCM) technique it will save the hardware area size and power consumption. In this Proposed work of this paper will realization oflow complexity in area of design and less energy per sample, and in this design using coefficient from the h(x), to reduce the impulse noise, with Nth order structure.

Survey -5

Balasubramanian, Nikos E. Mastorakis, Padmanabhan, 2009, is discussed about the work of Full Adder Design with High Speed Gate level of design using gate with XNOR, AND, Inverter, Multiplexer and complex gates, this work present a design of 32bit Carry ripple adder implementation with compare the three process of voltage, temperature and power using CMOS Technology of 65nm. Finally found the comparison of best delay reduction in proposed work.

Survey -6

V.Kamalakannan, Ravi.H.N, Shilpakala.V, 2013 is discussed about the work of Reversible gate design of full adder in quantum computing and it has to possible design logic of extensive application, they study about the technology aimed at implementing to improve the energy efficiency in Quantum Computing, using TG-Gate, here the design will contain the full adder design of TG-Gate will compare the all reversible gate design, hence proved this TG-gate will produce the better results in area, delay and power consumption. Finally design a Carry skip adder design using this TG Gate and shown the performance and better results compare to the all reversible gate design.

Survey -7

Ms. Anagha U P, Mr. Pramod P, 2015, is discussed and proved a new approach of Carry Select adder design using SQRT method, this design will have new gate design of HSG (Haft Sum Generation), FSG (Full Sum Generation), CS (Carry Select), CG (Carry Generation) based technique. Logic optimization of SQRT CSLA providing a separate carry generator operation in the final sum of ever operation, and this design will has taken less area and power consumption.

Survey -8

Yi-Sheng Lin, I-Chyn Wey, Chien-Chang Peng and Cheng-Chen Ho,2012 is discussed about adder design of Carry Select adder with Common Boolean logic term. Using the logic gate design of XOR gate with inverter, AND gate with inverter to design this operation. The mux operation will decide the full adder output using the selection bit of first sum of addition. The output of this architecture will design 32bit addition, moreover it will reduce the area and also power consumption compare to the existing method.

Survey -9

Himanshu Thapliyal and A.P Vinod, 2007 is discussed about the design of online testable gate in Reversible logic method. Using this Online Testable gate to improve the efficiency in Reversible gate adders of 4x4 it produced the suitable online testability. The proposed design of this method to design a Ripple carry adder, Carry skip adder and BCD adder with Reversible logic design of Feynman gate design. Finally test this reversible logic design using Feynman gate compared to the Online testable gate method, and hence proved the better results in Area, unit delay, garbage outputs and power consumption.

Survey -10

Athira Prasad, Robin Abraham, 2014 is discussed about the work of Multiplier is advance technology of DSP (Digital Signal Processing Application), with High speed, low power and layout with reduction in area, time and unit delay in the Design. In the recent multiplier of n x n will produce the output in 2n bits, so it will take more area, of internal and external design of architecture. In this proposed work of this paper, a new approach of Truncated multiplier will design using the 3 type of method, such as rounding, deleting, and unnecessary bits, this truncated multiplier will produce the n bit output from the n x n bits of input. Finally shown the comparison of area, power and delay with better results.

Survey -11

C.S.Manikandababu, R. Devarani, 2013 is discussed about the work of Truncated Multipliers with precision improvements, this multiplier will reduce the significant parameters of area, power and delay. The proposed method of this truncated precision multiplier will design using number of full adders and half adders, the MSB part of the partial product will be used, and LSB part of partial product will reduced using the three method of rounding, deleting and truncating in the final part of addition and also provide the output on n bit from the input of n x n bits. Finally shown the comparison of area, delay and power with better results.

Survey -12

Theo Drane, George A and Thomas Rose, 2013, is discussed about the project of Truncated multiplier with faithfully rounded method, it is the modified method of normal truncated method will better results, and also reduced the method of partial product with the technique of rounded, deleted and truncated method. This design presents the 32bit multiplier using Monte carlo simulation method and shown the better results compare to the normal truncated operation with maintaining faithfully rounding with arbitrary array.

Survey -13

Kanchana Bhaaskaran V S,Bhuvana B P, 2016 is discussed about the Gate design of BKG with design of reversible full adders. In the method of quantum dot cellular automation with computation of logic gate in reversible method with shown the performance of area, delay and power reduction compare to the all quantum gate operations. In in proposed work to design a novel architecture full adder using to design with 4x4 BKG gate of reversible method. Finally shown the comparison of better results in computation of area, delay and power.

Survey -14

PravinK.Dakhole, Sujata S.Chiwande, 2012 is discussed about the work of Fredkin reversible gate design and TSG reversible gate design. In the design of 4bit Carry Skip adder will design using the forward and backward method of 4x4 TSG gate with Fredkin gate and shown the comparison of normal quantum computing technique of CMOS technology. Finally shown the comparison of this 4bit carry skip adder design in the CMOS technology of 65nm with better results.

References

[1] "Low-Power and Area-Efficient Carry Select Adder", B. Ramkumar and Harish M Kittur, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 1063-8210/$26.00 © 2011 IEEE.

[2] "Design and Implementation of 8X8 Truncated Multiplier on FPGA", Suresh R.Rijal (Asst. Prof. KITS, Ramtek), Ms.Sharda G. Mungale (Asst. Prof. PCEA, Nagpur), International Journal of Scientific and Research Publications, Volume 3, Issue 3, March 2013.

[3] "Area–Delay–Power Efficient Carry-Select Adder", Basant Kumar Mohanty, Senior Member, IEEE, and Sujit Kumar Patel, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 61, NO. 6, JUNE 2014.

[4] "A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications", Basant Kumar Mohanty, Senior Member, IEEE, and Pramod Kumar Meher, Senior Member, 1063-8210 © 2015 IEEE.

[5] "High Speed Gate Level Synchronous Full Adder Designs", WSEAS TRANSACTIONS on CIRCUITS and SYSTEMS, PADMANABHAN BALASUBRAMANIAN and NIKOS E. MASTORAKIS, Oxford Road, Manchester M13 9PL, UNITED KINGDOM.

[6] "DESIGN OF ADDER / SUBTRACTOR CIRCUITS BASED ON REVERSIBLE GATES", V.Kamalakannan, Shilpakala.V, Ravi.H.N, International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 2, Issue 8, August 2013.

[7] "Power and Area Efficient Carry Select Adder", 2015 IEEE Recent Advances in Intelligent Computational Systems (RAICS) | 10-12 December 2015 | Trivandrum.

[8] "An Area-Efficient Carry Select Adder Design by Sharing the Common Boolean Logic Term", I-Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin, and Chien-Chang Peng, Proceedings of the International Multi Conference of Engineers and Computer Science 2012 Vol II.

[9] "Designing Efficient Online Testable Reversible Adders With New Reversible Gate", HimanshuThapliyal and A.P Vinod School of

Computer Engineering, Nanyang Technological University, Singapore, 2007 IEEE.
[10] "Variable Truncated Multiplier with Low Power", AthiraPrasad , Robin Abraham, International Journal Of Engineering And Computer Science ISSN:2319-7242.
[11] "Design and implementation of truncated multipliers for precision improvement", 2013 International Conference on Computer Communication and Informatics (ICCCI -2013), Jan. 04 – 06, 2013, Coimbatore, INDIA.
[12] "On The Systematic Creation of Faithfully Rounded Truncated Multipliers and Arrays", Theo Drane, Thomas Rose and George A. Constantinides, 2013, IEEE TRANSACTIONS ON COMPUTERS.
[13] "Design of Reversible Adders Using A Novel Reversible BKG Gate", Bhuvana B, KanchanaBhaaskaran V S, 2016 Online International Conference on Green Engineering and Technologies (IC-GET).
[14] "A Novel Design of Compact Reversible SG Gate and its Applications", Payal Garg, Sandeep Saini, 2014 International Symposium on Communications and Information Technologies (ISCIT).
[15] SivakumarV.G.and RajendranV.(2013), "Comparison and analysis of verticalcoherenceintheshallowwateroftwooceanregion",AmericanJournalofAppliedSciencesVol. 10 No.6 542-548/ Apr-May2013.
[16] Romana Yousuf, Najeeb-ud-din,"Synthesis of Carry Select Adder in 65 nm FPGA", IEEE.
[17] Animulislam, M.W. Akram, S.D. pable, Mohd. Hasan, "Design and Analysis of Robust Dual Threshold CMOS Full Adder Circuit in 32 nm Technology", International Conference on Advanced in Recent Technologies in Communication and Computing, 2010.
[18] V. Kantabutra, "Accelerated two-level carry-skip adders-a type of very fast adders," *IEEE Transactions on Computers*, vol. 42, no. 11, pp. 1389–1393, 1993.
[19] K. Chirca, M. Schulte, J. Glossner, et al., "A static low-power, high-performance 32-bit carry skip adder," in *Proceedingsof the EUROMICRO Symposium on Digital System Design (DSD '04)*, pp. 615–619, Rennes, France, August-September 2004.
[20] K. Chirca*et al.*, "A static low-power, high-performance 32-bit carry skip adder," in *Proc. EuromicroSymp. Digit. Syst. Design (DSD)*, Aug./Sep. 2004, pp. 615–619.
[21] V. G. Oklobdzija, B. R. Zeydel, H. Dao, S. Mathew, and R. Krishnamurthy, "Energy-delay estimation technique for highperformance microprocessor VLSI adders," in Proc. 16th IEEE Symp. Comput. Arithmetic, Jun. 2003, pp. 272–279.
[22] R. Zlatanovici, S. Kao, and B. Nikolic, "Energy–delay optimization of 64-bit carry-lookahead adders with a 240 ps 90 nm CMOS design example," IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 569–583, Feb. 2009.