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Research paper

Realization of LTE physical layer baseband processing architecture for narrowband IOT

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Abstract

The 3GPP Long Term Evolution represents the major innovation in cellular technology. NB-IoT is the 3GPP standard for machine to machine communication finalized within LTE Release13. NB-IoT technology occupies frequency band of 180 kHz bandwidth which corresponds to one resource block in LTE transmission. The Long Term Evolution (LTE) supports higher data rates, higher bandwidth, Low latency, good Quality of Service whereas objective of Narrow Band Internet of Things (NB - IOT) is to achieve extended coverage, to support massive number of smart devices and have multi - year long battery life. So the main focus is linking LTE with IOT. The objective of this paper proposes transmitter architecture of PUCCH (Physical Uplink Control Channel) and PUSCH(Physical uplink Shared Channel) in SISO and SIMO configurations for physical uplink channels of LTE. The physical uplink and downlink channel processing involves scrambling, modulation, layer mapping, transform precoding, and resource element mapping at the transmitter and the receiver block to have demapping from the resource elements and detection of data. At present, the data for on-off control has been worked and the whole framework has been simulated using Modelsim and implemented in Spartan 6.

1. Introduction

THE 3GPP standardization LTE evolution is the key component in release 13. The features of LTE are expanding carrier aggregation, full dimensional MIMO and Narrowband IOT. NB-IoT also have new UE device category called Cat-NB1 [1]. LTE use two different frame structure namely Time Division Multiplexing(TDD), Frequency Division Multiplexing(FDD) and their illustrations are given in [2].In LTE standard FDD and TDD frame structures are represented as Type 1 and Type 2. In this paper FDD frame structure is followed. An early research mainly focuses on architecture for SISO, SIMO, MIMO of Physical downlink control channels of LTE [3]. LTE standard has six channel for downlink operation and three channels for uplink operations i.e. user equipment to the base station and base station to the user equipment. Information for the downlink channels are received from the higher layer [4]. The objective of this paper is to propose LTE physical layer baseband architecture for Narrowband IoT. A brief out line of LTE uplink channels is given in section II.System model and its processing steps are explained in section III and IV respectively. Implementation processes are illustrated in section V. Simulation and implemented results are explained in section VI.

2. Processing channels

LTE uplink physical channels include one control channel and two data channel. The control channel PUCCH is essential for successful transmission. The data channels are PUSCH and PRACH. These channels are described in the following sections

PUCCH (Physical Uplink Control Channel)

The physical uplink control channel, PUCCH, carries uplink control information (UCI). The physical uplink control channel supports multiple formats as shown in Table I with different number of bits per subframe. Each format use different modulation symbols and number of bits per subframe. The format 1a is used in this paper for transmission. The format 1a supports BPSK modulation scheme and number of bits per subframe is 2.

PUSCH (Physical Uplink Shared Channel)

This channel is used to carry RRC signalling messages and application data.LTE PUSCH channel contain user information data.PUSCH supports QPSK, 16QAM and 64QAM (optional).PUSCH carries the uplink user data signalling transport block from the MAC layer to the Physical layer.

Table I: Supported format for PUCCH

PUCCH	Modulation scheme	Number of bits per subframe
1	N/A	N/A
1a	BPSK	1
1b	QPSK	2
2	QPSK	20
2a	QPSK+BPSK	21
2b	QPSK+QPSK	22
3	QPSK	48
4	QPSK	$M_{RB}^{PUCCH}.N_{sc}^{PUCCH}(N_0^{PUCCH}+N_1^{PUCCH})$ .2
5	QPSK	$N_{sc}^{RB}.(N_0^{PUCCH}+N_1^{PUCCH})$

3. System model

Combined architectures for all the three uplink channels for transmitter and receiver are illustrated in Fig 1. The processing steps are explained in the following sections.

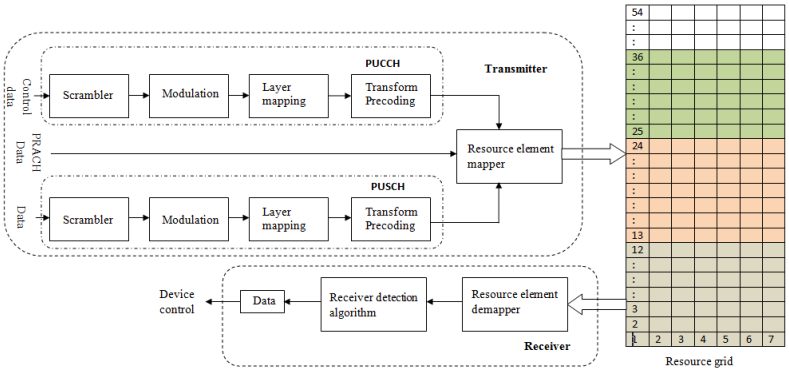

Fig. 1: Over all block diagram

4. Processing steps

Scrambling

Scrambling uses 8 bit LFSR at the transmitter side which is used to generate the pseudo random sequence continuously. A polynomial used for the LFSR operation is given by (1).The output from the scrambler block is given as one bit scrambled data. This is obtained bydoing 2 input EX-OR operation with one bit of incoming data from the upper layer and last bit of pseudo random sequence. To increase the speed of the scrambler, clock given to scrambler is upconverted for the various channels based on their modulation.

$$T = Y[6] \oplus Y[7] \oplus Y[1] \oplus Y[2] \quad (1)$$

Modulation

Physical uplink control channels (PUCCH) use two different types of modulation schemes. They are 1.BPSK (Binary phase shift keying) and 2.QPSK (Quadrature phase shift keying).Physical uplink shared channel (PUSCH) use two different types of modulation schemes. They are 1.QPSK (Quadrature phase shift keying) and 2.16 QAM (Quadrature Amplitude Modulation).Pre defined values are used for the different type of modulation. Pre defined values have both in phase and Quadrature phase component. These predefined values for different modulations are tabulated in Table II,III and IV.The scrambled bits are converted into complex symbols.

Table II: BPSK

S	I	Q
0	1/√2	1/√2
1	-1/√2	-1/√2

Table III: QPSK

S	I	Q
00	1/√2	1/√2
01	-1/√2	1/√2
10	1/√2	-1/√2
11	-1/√2	-1/√2

Table IV: 16QAM

S	I	Q
0000	1/√10	1/√10
0001	1/√10	3/√10
0010	3/√10	1/√10
0011	3/√10	3/√10
0100	1/√10	-1/√10
0101	1/√10	-3/√10
0110	3/√10	-1/√10
0111	3/√10	-3/√10
1000	-1/√10	1/√10
1001	-1/√10	3/√10
1010	-3/√10	1/√10
1011	-3/√10	3/√10
1100	-1/√10	-1/√10
1101	-1/√10	-3/√10
1110	-3/√10	-1/√10
1111	-3/√10	-3/√10

Layer mapping

Layer mapping, maps the modulation symbols to the antenna ports in the higher layers. The antennas may be single antenna or multi antenna. This single and two antennas are used to achieve SISO and MIMO architecture respectively. Transmit diversity is used

for mapping input symbols to one layer. The two layer mapping is done using spatial diversity. This spatial diversity used to increase the speed and avoid the failure of antennas. Mathematical equations are given in Table V. For the single antenna transmission, the mapping is defined by the expression (2).

$$x^{(0)} = d^{(0)} \quad With\ M_{symb}^{layer} = M_{symb}^{(0)} \qquad (2)$$

Transform precoding

In transform precoding, vector is created for the layer mapped data. For this process 8-point FFT is used to get the vector. The data from the layer mapping is stored in RAM. For the each eight layer mapped data, FFT operation is performed and gives the vector for the single and two antenna port. The equation for FFT is represented as (3).

Resource element mapping

The output from the transform precoding is mapped to the resource grid. The LTE resource grid structure is illustrated in Fig2.Each frame has ten subframes and each subframe has two slots. Each slot has 7 x 54 resource element i.e. 7 columns and 54 rows. One frame takes 10ms.So one slot takes 0.5 ms.

Processing steps at receiver side

To get the original data demapping from the resource grid, MMSE algorithm is used instead of using reverse operation of transmission such as decoding, delayer mapping, demodulation and descrambling. The received data is used for ON/OFF control of any device.

Table V: Layer Mapping

Number of layers	Number of code words	Code words to layer mapping i=0, 1, 2 ... M_{symb}^{layer}
1	1	$x^{(0)}(i) = d^{(0)}(i)\ M_{symb}^{layer} = M_{symb}^{(0)}$
2	1	$x^{(0)}(i) = d^{(0)}(2i)$ $M_{symb}^{layer} = M_{symb}^{(0)} / 2$ $x^{(0)}(i) = d^{(0)}(2i+1)$
2	2	$x^{(0)}(i) = d^{(0)}(i)$ $M_{symb}^{layer} = M_{symb}^{(0)} = M_{symb}^{(1)}$ $x^{(1)}(i) = d^{(1)}(i)$

$$X(l.M_{sc}^{pusch} + k) = \frac{1}{\sqrt{M_{sc}^{pusch}}} \sum_{i=0}^{M_{sc}^{pusch}-1} x(l.M_{sc}^{pusch} + i) \exp\left[\frac{-j2\pi ik}{M_{sc}^{pusch}}\right] \qquad (3)$$

$k=0, 1, 2... M_{sc}^{pusch}$ $l=0, 1, 2... M_{sym}^{layer}$

$12 \le M_{sc}^{pusch} \le 1200$- *(34 kinds are possible)*

M_{sc}^{pusch} - Number of subcarriers M_{sym}^{layer} - Number of modulation symbol

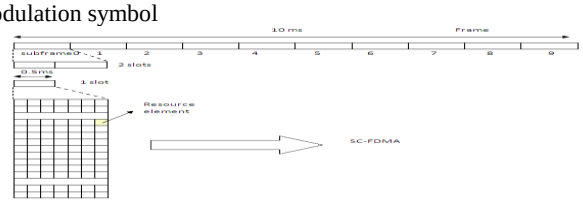

Fig. 2: LTE TDD diagram

5. Implementation

Scrambling

The input clock given for scrambler is 80 MHz If the channel selected is PUSCH and modulation are QPSK and QAM, then clock runs at frequency of 40MHz and 80MHz respectively. If the channel selected is PUCCH, then the modulation is BPSK and QPSK then clock runs at the frequency of 20MHz and 40MHz respectively. The operating clock frequency is mentioned in Table VI. The scrambler operation is illustrated in Fig 3.

Table VI: Clock Frequency

Channels	Modulation	Frequency(MHz)
PUSCH	QPSK	40
	16 QAM	80
PUCCH	BPSK	20
	QPSK	40

Modulation

Pre defined values are based on IEEE 754 single precision floating point representation. Actual In phase (I) and Quadrature (Q) phase are 32 bits and concatenated as single complex value as 64 bits. Assumptions made are 16 bit truncation in both in phase and Quadrature phase. Finally the scrambled bits are mapped to 32 bits complex value consist of in-phase and Quadrature of 16 bits each. IEEE 754 representation of pre defined values are mentioned in Table VII.The modulation operation is illustrated in Fig 4.

Table VII: IEEE 754 Representations of Symbols

Values	IEEE 754 representation
$1/\sqrt{2}$	00111111001101010000010010000001
$-1/\sqrt{2}$	10111111001101010000010010000001
$1/\sqrt{10}$	00111110101000011110011110010110
$-1/\sqrt{10}$	10111110101000011110011110010110
$3/\sqrt{10}$	00111111011100101101110010110001
$-3/\sqrt{10}$	10111111011100101101110010110001

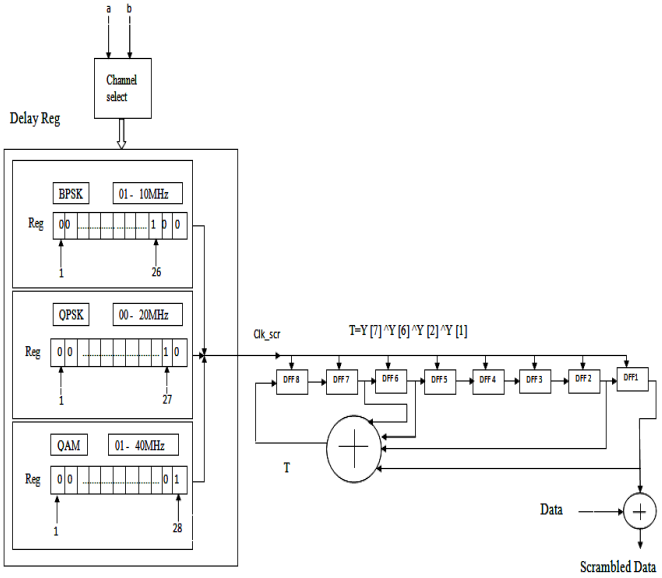

Fig.3: Scrambler operation

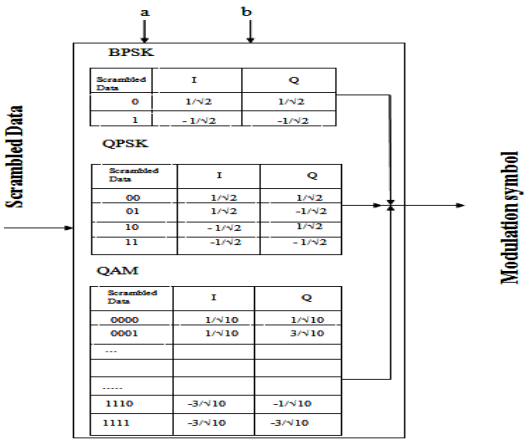

Fig.4: Modulation operation

Layer mapping

Assumptions are made by considering only single and two antennas. The two possible combinations are given as input. If the single port is chosen then 16 bit modulation symbols are mapped to one layer. If two layer mapping is chosen, one of the possibilities made is mapping 16 bits modulation symbols to both the antenna ports .Another possibility is splitting modulation symbols as odd and even. Then this separate odd and even symbols are mapped to antenna ports. This layer mapping operation for single and two antenna is illustrated in Fig5.

Table VIII: Values for Exponential Term IN FFT

Parameter	IEEE 754 representation
c0	00000000000000001000000000000000
c1	00111111001101001011111100110100
c2	00000000000000001000000000000000
c3	10111111001101010111111001101001
c4	10000000000000000000000000000000
c5	10111111001101000011111100110100
c6	00000000000000000000000000000000
c7	00111111001101000111111001101001

Transform precoding

Transform precoding is done using 8 point FFT. FFT implementation consists of 32 adders(32 bits) and 19 multipliers(32 bits). The result of the multiplier is 64 bits. In that 32 bit truncation is used. The layer mapped data are stored in RAM. After receiving eight layer mapped data FFT process takes place. The specifications are mentioned in the Table IX.The values for exponential term in FFT are tabulated in Table VIII. The FFT architecture diagram is illustrated in Fig 6. The equations used for FFT architecture are expressed as equations from (3) to (19).

Table IX: Specification Table

Parameter	Values
M_{sc}^{pusch}	12
M_{sym}^{layer}	2

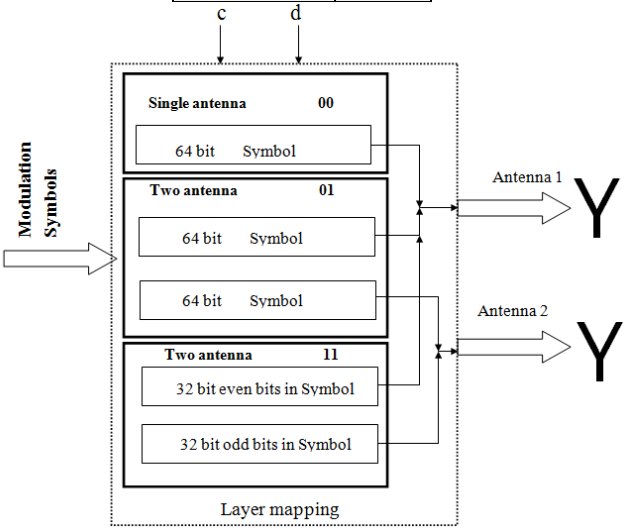

Fig.5: Layer mapping

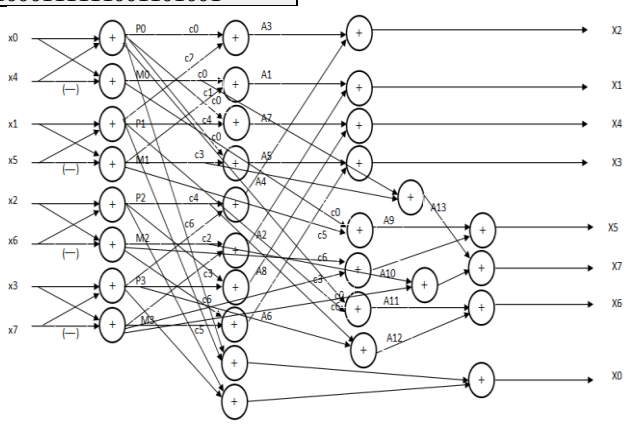

Fig.6: 8-pointFFT architecture diagram

$$X0 = c0(x0 + x1 + x2 + x3 + x4 + x5 + x6 + x7) \quad (4)$$

$$X1 = c0.M0 + c1.M1 + c2.M2 + c3.M3 \quad (5)$$

$$X2 = c0.P0 + c2.P1 + c4.P2 + c6.P3 \quad (6)$$

$$X3 = c0.M0 + c3.M1 + c5.(-M3) + c6.M2 \quad (7)$$

$$X4 = c0.P0 + c4.P1 + c0.P2 + c4P3 \quad (8)$$

$$X5 = c0.M0 + c5.M1 + c6.(-M2) + c3.(-M3) \quad (9)$$

$$X6 = c0.P0 + c6.P1 + c4.P2 + c2.P3 \quad (10)$$

$$X7 = c0.M0 + c3.(-M1) + c2.(-M2) + c1.(-M3) \quad (11)$$

$$M0 = x0 - x4 \quad (12)$$

$$M1 = x1 - x5 \quad (13)$$

$$M2 = x2 - x6 \quad (14)$$

$$M3 = x3 - x7 \quad (15)$$

$$P0 = x0 + x4 \quad (16)$$

$$P1 = x1 + x5 \quad (17)$$

$$P2 = x2 + x6 \quad (18)$$

$$P3 = x3 + x7 \quad (19)$$

Resource element mapping

The precoded data are mapped to LTE grid structure as illustrated in Fig 7. This grid structure consists of 54 rows and

7 columns. Resource gridis divided into three sections for three channels.1-12 rows for PUCCH and 13-24 for PUSCH and 25-36 for PRACH.The data. The data should be arranged in their

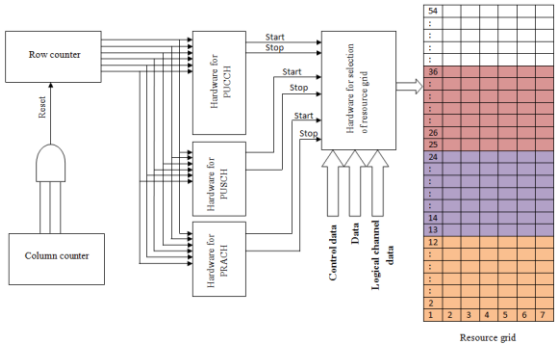

Fig.7: Resource element mapping architecture diagram

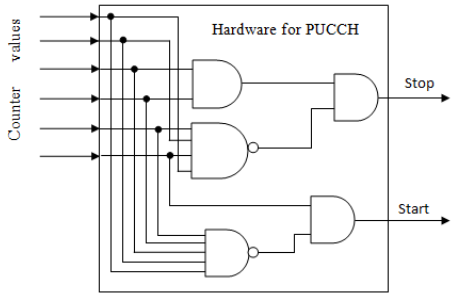

Fig.8: Counter value for PUCCH(1-12)

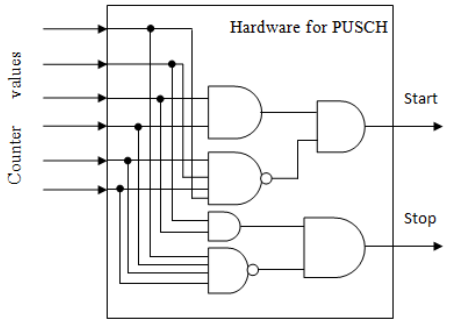

Fig.9: Counter value for PUSCH(13-24)

Demapping and detection of data

From the resource grid the processed data are demapped. The receiver algorithm, Minimum Mean Square Error is used for data detection from the processed data. This architecture is shown in Fig 10.

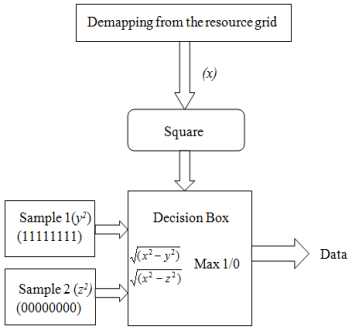

Fig.10: Receiver algorithm architecture

6. Simulation results

Scrambling

When the input i.e. the channel selection is “00” channel PUSCH is selected and QPSK modulation is selected. For QPSK clockspeed which is given to the scrambler is 40 kHz. When the input is “01” then channel PUSCH is selected and corresponding positions. This massive task is performed using counter in both rows and columns. The counter architecture for PUCCH and PUSCH are illustrated in Fig 8 and 9 respectively. 16QAM modulation is selected. For 16 QAM clock speed which is given to the scrambler is 80 kHz. When the input is “10” then channel PUCCH is selected and BPSK modulation is selected. For BPSK clock speed which is given to the scrambler is 20 kHz. When the input is 11 then channel PUCCH is selected and QPSK modulation is selected. For QPSK clock speed which is given to the scrambler is 40 kHz. This is illustrated in Fig11.

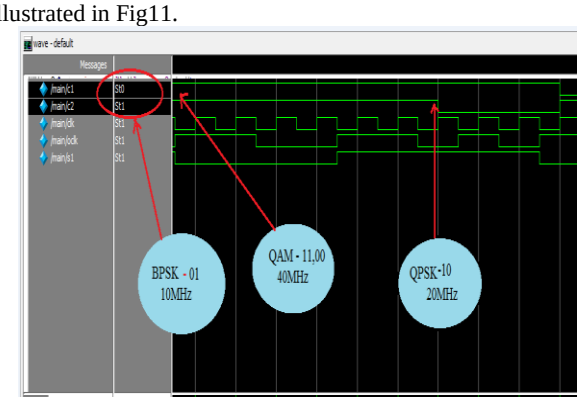

Fig.11: Scrambling result

Modulation

1. BPSK

When PUCCH and BPSK Modulation is selected for one clock (clock given to modulation) each scrambled bit is converted to modulation symbol. This conversion is illustrated in Fig12.

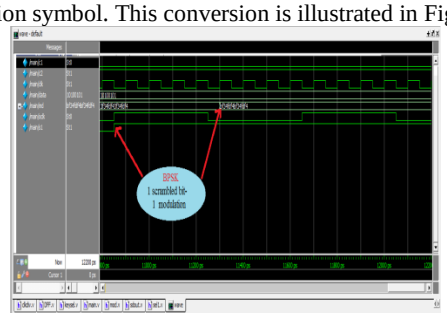

Fig.12: BPSK Modulation result

2. QPSK

When BPSK Modulation is selected for one clock (clock given to modulation) each two scrambled bits are converted to one modulation symbol. Because QPSK is dibit combination. This conversion is illustrated in Fig13.

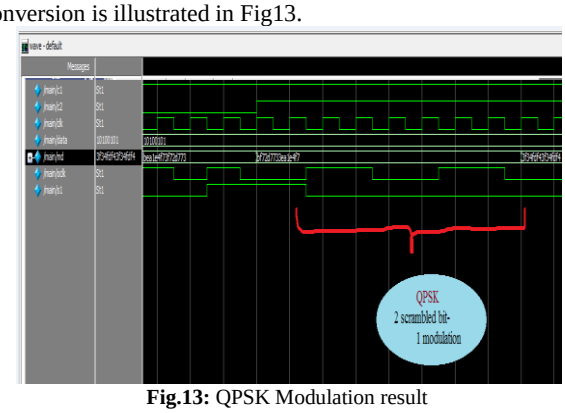

Fig.13: QPSK Modulation result

3. 16QAM

When 16QAM Modulation is selected for one clock (clock given to modulation) each four scrambled bits are converted to

one modulation symbol. This conversion is illustrated in Figure 13.

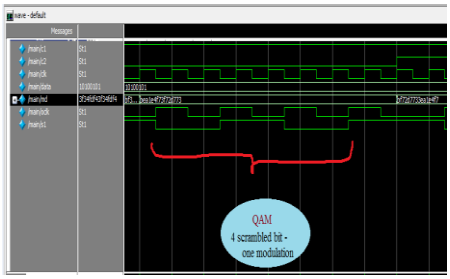

Fig.14: 16 QAM Modulation result

Layer mapping

1. Single antenna

When input is selected for single antenna port (i.e. "00") the modulated symbol is mapped to single antenna port. No symbol is mapped to another antenna port.The mapping to single antenna is given in Fig 15.

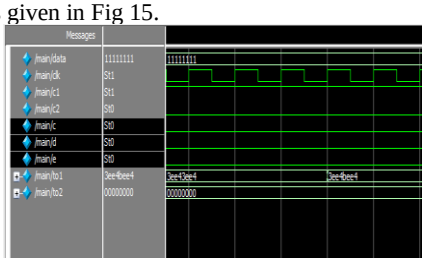

Fig.15: Single antenna layer mapping processing

2. Two antenna (transform diversity)

When input is selected for single antenna port (i.e."10") the same modulated symbol is mapped to the two antennas. If any antenna fails then another antenna helps to receive the data.This transform diversity is illustrated in Fig16.

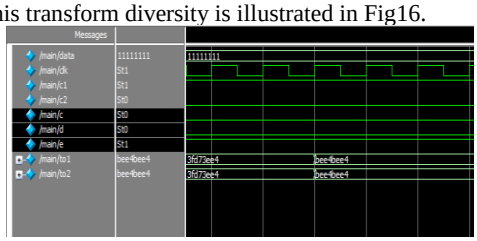

Fig.16: Two antenna with transform diversity

3. Two antenna(Spatial diversity)

When input is selected for single antenna port (i.e."11") the modulated symbol is splited into odd and even bits. Odd bits mapped to one antenna and the even bits mapped to another antenna port. This helps to increase the speed of the transmission. This spatial diversity is illustrated in Fig17.

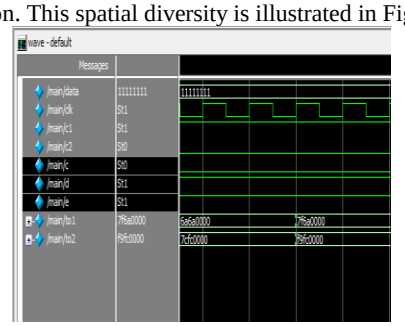

Fig.17: Two antenna with spatial diversity

Transform precoding

When the eight symbols received from the layer mapping antennas the transform block will perform fast fourier transform (FFT) and gives eight output data. The transform precoding operation is illustrated in Fig18.

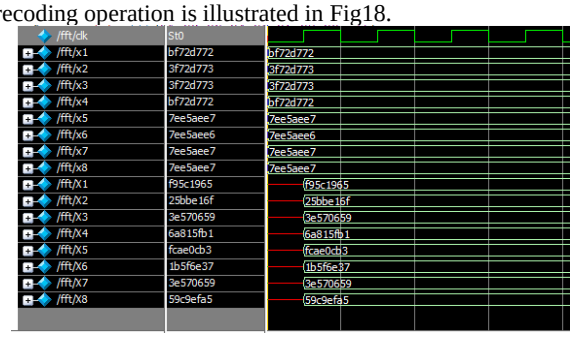

Fig.18: Transform precoding

Resource element mapping

The resource grid has three sections for PUCCH, PUSCH and PRACH. The data from the transform precoding block mapped in the resource grid in the respective sections based on the channel selection. This process is done as shown in the Fig19.

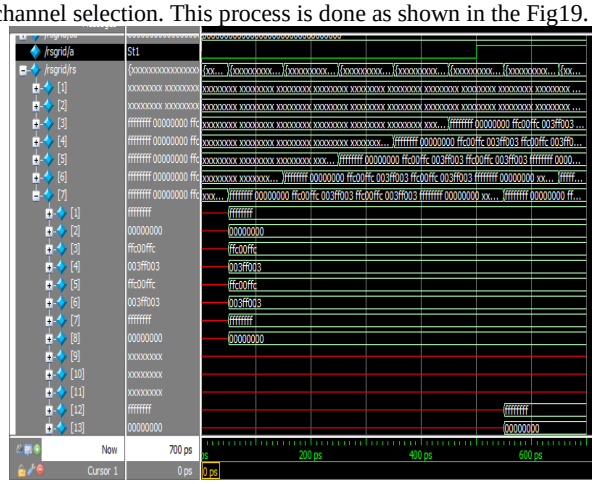

Fig.19: Resource element mapping

Combined output

The combined output of the designed architecture for the LTE baseband processing is shown in the Fig20.

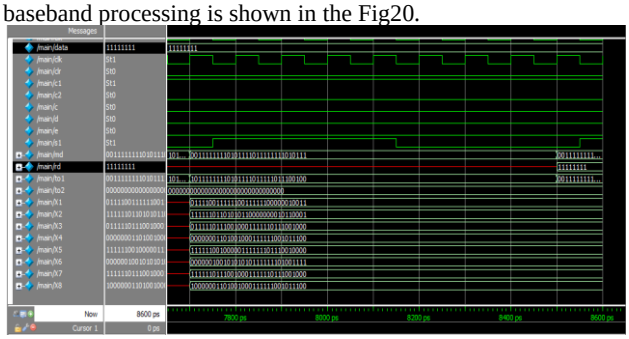

Fig.20: Combined result

7. Implementation results

FPGA editor

Using FPGA editor routing between input and output connections are shown in Fig 21. This figure gives an idea how various components are placed, mapped and routed in Spartan 6 device. This is done by using PlanAhead 14.6 tool from Xilinx.

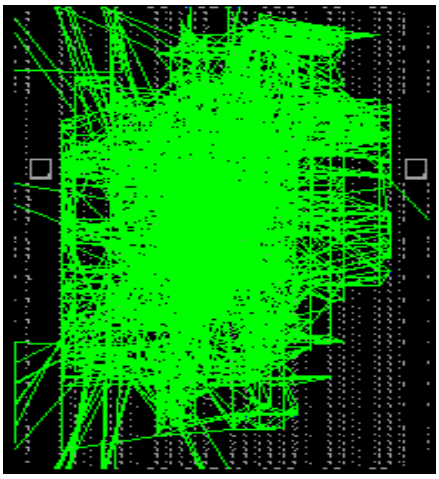

Fig.21: FPGA editor of transceiver

Design summary

Plan Ahead tool is used to estimate the utilization of I/O devices, Memories, LUTs and other resources. The summary of all devices are mentioned in the Table X.

Table X: Design Summary

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	2,593	18,224	14%
Number used as Flip Flops	2,437		
Number used as AND/OR logics	156		
Number of Slice LUTs	3,770	9,112	41%
Number used as logic	3,754	9,112	41%
Number using O6 output only	2,657		
Number using O5 output only	355		
Number using O5 and O6	742		
Number used exclusively as route-thrus	16		
Number with same-slice register load	1		
Number with same-slice carry load	15		
Number of occupied Slices	1,237	2,278	54%
Number of MUXCYs used	1,140	4,556	25%
Number of LUT Flip Flop pairs used	4,049		
Number with an unused Flip Flop	1,613	4,049	39%
Number with an unused LUT	279	4,049	6%
Number of fully used LUT-FF pairs	2,157	4,049	53%
Number of unique control sets	25		
Number of slice register sites lost to control set restrictions	115	18,224	1%
Number of bonded IOBs	55	186	29%
Number of LOCed IOBs	55	55	100%
Average Fanout of Non-Clock Nets	3.60		

Snapshot of FPGA implementation

In the transmitter side, the input data given is “11111111” after doing all the processing steps the data detected at the receiver side is “11111001”.Because of maximum 1’s in the receiver side it is used for ON control of the LED. This shown in the Fig 22.

Fig.22: FPGA implementation of transceiver

8. Conclusion

The architecture for LTE physical layer baseband processing which includes scrambling, modulation, layer mapping, Transform precoding, resource element mapping in the transmitter side and demapping from resource elements, detection of data by using maximum likelihood function in the receiver side areimplemented in Spartan 6 using Plan Ahead 14.6 tool. From the data obtained from the receiver side ON/OFF control of device is illustrated in this paper.

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