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Research paper



Grounded Impedance Simulator Topologies Employing Minimum Passive Elements

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Abstract

In this research three new grounded inductance simulators (GIS) are proposed. In addition, frequency dependent negative resistor (FDNR) and grounded capacitor (GC) simulators are also developed. The voltage differencing current conveyor (VDCC) is utilized in the design. All the developed simulator circuits need a single active block and only two grounded passive components. All the designed simulator circuits are perfectly tunable and did not suffer from passive component matching constraints. To demonstrate the performance of the inductor, FDNR and GC circuits they are employed in designing current mode parallel RLC multifunction filter, low pass third order Butterworth filter and RLC resonance circuits. The VDCC is designed in 0.18µm CMOS technology parameters from TSMC and simulated in P-Spice software to prove the theoretical predictions.

Keywords: *Current Mode; Capacitors; Current conveyor; Inductors; Simulators; Tunability*

1. Introduction

Inductor, capacitor and FDNR are crucial components in electronic circuits. The inductors, capacitors and FDNR are employed in designing active filters for communication systems. They are also employed in phase shifters, oscillators, for parasitic cancellation and impedance matching etc. [1-2]. The main drawback of the passive inductor is requirement of excessive chip area. In addition, passive inductors are vulnerable to process fluctuations and suffer from resistive losses [1]. The passive capacitors suffers from use of large silicon area, small capacitance value etc.

The requirement of low voltage low power operation (LVLP) put forward by the increased development of portable devices, bio medical systems, wireless sensor nodes and energy harvesting modules [3-6] have shifted the focus of research to current mode devices. The frequently used current mode active blocks [1-2, 6-7] for immittance simulation are the second generation current conveyor (CCII) [1, 2, 6], current feedback operational amplifier (CFOA) [7], fully differential current conveyor (FDCCII) [8], dual x current conveyor (DXCCII) [9], differential difference current conveyor (DDCC) [11], operational trans-resistance amplifier (OTRA) [12], voltage differencing buffered amplifier (VDBA) [13], inverting current conveyor (ICCII) [15] etc. The grounded simulators for realizing GI, GC and grounded FDNR (G-FDNR) can be compared on many basis like the number of active blocks employed, number of passive components required and capability of inbuilt tunability. The immittance simulators presented in [7, 8, 18, 20, 21] employ two or more active blocks and higher number of passive components. The simulator structures in [1, 7, 9, 12, 15, 16, 21, 22, 23] employ one active block but require passive elements in excess of two for implementation. The designs proposed in [1, 7, 8, 9, 12, 13, 15, 19, 21, 23] make use of floating passive components for realizing inductance. The circuit configurations in [9, 10, 13, 18, 19, 25] enjoy inbuilt tunability owning to transconductance variation or parasitic resistance variation with bias current. The literature review suggests that the majority of the proposed simulator circuits have one or more of the enlisted drawbacks. (i) use of more than one active block (ii) higher passive component count (ii) employment of floating capacitors (iii) non tunable structure (iv) components matching constraints.

This paper presents three topologies for realizing pure and lossy GIS including grounded parallel inductance simulators. In addition, two topologies for realizing G-FDNR and GC are also presented. The proposed structures make use of two grounded passive elements. The proposed simulators are tunable and are realizable without any matching constraints. To demonstrate the performance of the proposed active immittance simulators they are employed in designing a current mode multifunction filter, low pass Butterworth third order filter and RLC resonance circuit. Simulations are carried out using TSMC 0.18µm model to validate the theoretical predictions.

2. CMOS Implementation of VDCC

The voltage differencing current conveyor basically consists of an operational transconductance amplifier at the input stage and a second generation current conveyor as second stage. The block diagram of the VDCC is shown in Fig. 1 and the current voltage relations are given in matrix Equation 1. The input terminals P and N are high impedance while X is a low impedance current input

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terminal. The output terminals Z, W_P and W_N are all high impedance terminals.

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{W_P} \\ I_{W_N} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix} \quad (1)$$

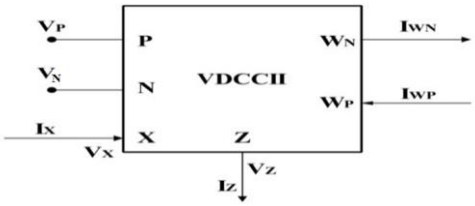


Fig. 1: Block diagram of VDCC

The CMOS realization of VDCC is shown in Fig. 2. The transconductance stage is realized by transistors M1-M8 and the current conveyor stage is realized by transistors M9-M22. Class AB stage (M13-M22) is used in the current conveyor owing to its wide dynamic range and low supply voltage requirement. Considering operation in saturation region and identical width to length ratio of transistors M1 and M2 the output current I_z of the OTA is given by Equation 2.

$$I_O = g_m(V_P - V_N) = \left(\sqrt{2I_{Bias}K_i}\right)(V_P - V_N) \quad (2)$$

Where, the transconductance parameter $K_i = \mu C_{ox} {}^{W}/_{2L}$, (i=1, 2), W is the effective channel width, L is the effective length of the channel, C_{ox} is the gate oxide capacitance per unit area and μ is the carrier mobility.

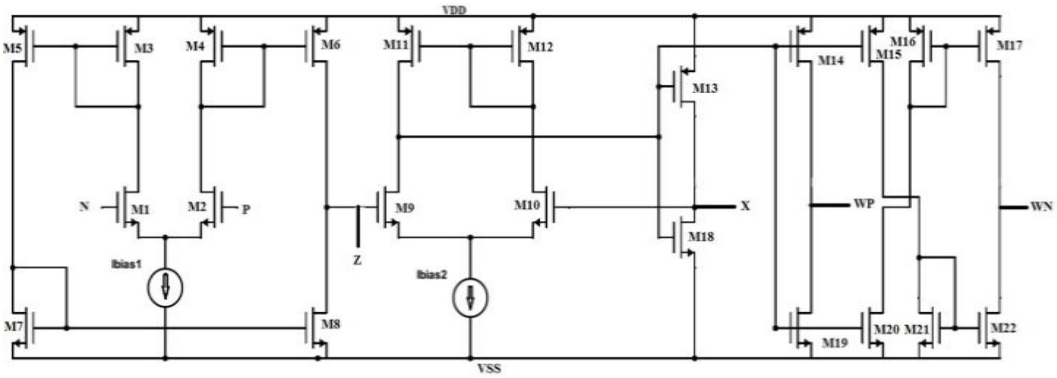


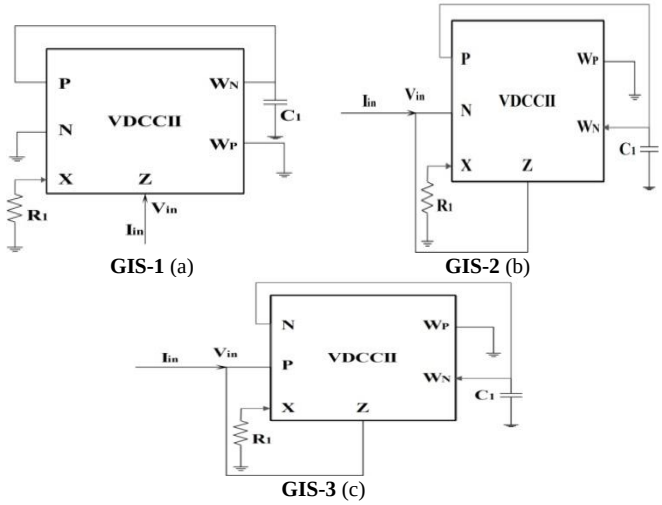
Fig. 2: CMOS implementation of VDCC

3. Proposed Grounded Simulators

The proposed grounded inductance simulators are shown in Fig. 3 (a-c). The inspection of the circuits shows that the GIS-1 realize pure positive inductance. The GIS-2 implements a positive inductance in parallel with a resistor while GIS-3 implements a negative inductance in parallel with a negative resistance. The impedance values of the proposed GIS are summarized in Table 1. In all the implementations the grounded capacitor is utilized which is advantageous for noise rejection and easy integrated circuit implementation.

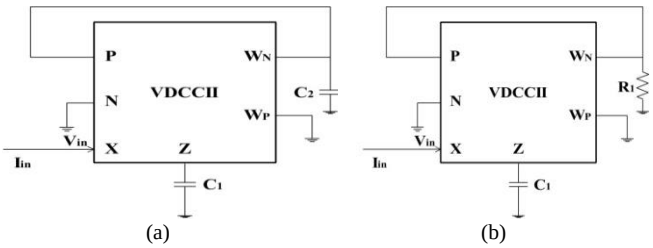
Table 1: Impedance of the Proposed Inductor Simulators

Simulator	Input Impedance	Inductance	Equivalent Resistance
GIS-1	$\frac{SC_1R_1}{g_m}$	$\frac{SC_1R_1}{g_m}$	-
GIS-2	$\frac{SC_1R_1}{g_m} + \frac{1}{g_m}$	$\frac{SC_1R_1}{g_m}$	$\frac{1}{g_m}$
GIS-3	$-\frac{SC_1R_1}{g_m} - \frac{1}{g_m}$	$-\frac{SC_1R_1}{g_m}$	$-\frac{1}{g_m}$



GIS-1 (a) **GIS-2** (b) **GIS-3** (c)

Fig. 3: Proposed grounded inductor simulators



(a) (b)

Fig. 4: Proposed (a) grounded FDNR (b) grounded capacitor simulator

The grounded FDNR and GC simulators are shown in Fig. 4 (a-b). The routine analysis of the circuits yield the expression for impedance as presented in Equations 3-4.

$$Z_{EqFDNR} = \frac{1}{D_{Eq}s^2} \quad (3)$$

Where, $D_{Eq} = \frac{C_1C_2}{g_m}$

$$Z_{EqCapacitor} = \frac{1}{C_{Eq}s} \quad (4)$$

Where, $C_{Eq} = \frac{C_2}{g_m R_1}$

4. Simulation Results

The voltage differencing current conveyor is designed in 0.18µm technology parameters from TSMC and simulated in P-Spice software to do the design verification. The supply voltages are selected equal to $V_{DD} = -V_{SS} = 0.9$V. The width to length ratios of the MOS transistors are as follows M1-M4 (3.6µm/1.8µm), M5-M6 (7.2µm/1.8µm), M7-M8 (2.4µm/1.8µm), M9-M10 (3.06µm/0.72µm), M11-M12(9µm/0.72µm), M13-M17 (14.4µm/0.72µm), M18-M22(0.72µm/0.72µm). The bias currents of the OTA and CCII are fixed at I_{bias1}=50µA and I_{bias2}=100µA.

At first, the lossless inductance simulator GIS-1 is tested. The GIS-1 is realized by selecting the component values as follows: C_1=50pF, R_1 = 2kΩ and I_{Bias}=20µA resulting in L_{Eq}=0.547mH. The Fig. 5 presents the simulated and ideal responses of the GIS-1. It can be inferred from the plot that the ideal and simulated values bear close resemblance.

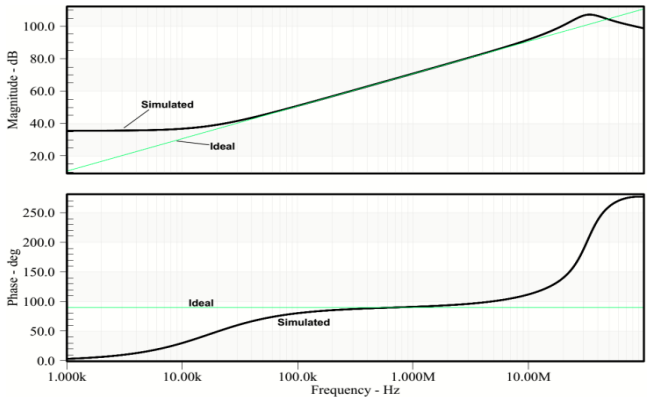


Fig. 5: The magnitude and Phase of the GIS-1 simulator

The tunability of the simulator is verified by plotting the phase and magnitude of the inductor for different values of OTA bias current ($\mathbf{I_{bias1}}$=10µA, 20µA, 30µA, 50µA) as shown in Fig. 6. Furthermore, to examine the effect of technological spread on the performance of the GIS-1 simulator Monte Carlo analysis is performed for 10% variation in the capacitance value. The result for 50 runs is presented in Fig. 7. It can be seen that the proposed topology performs well. Any deviation from the desired value can be easily cancelled by controlling the bias current of the OTA.

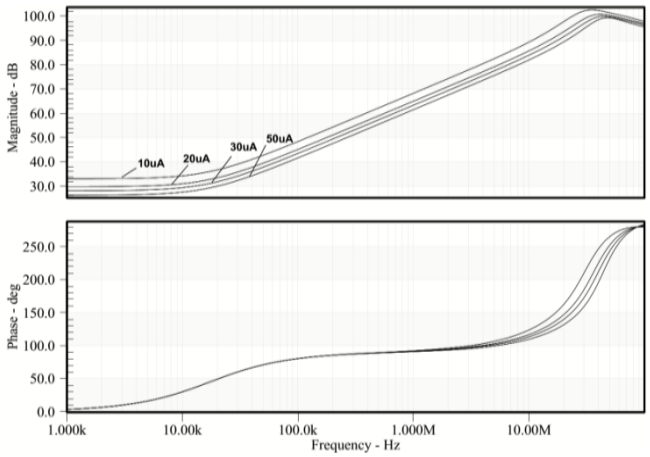


Fig. 6: The magnitude and Phase of the GIS-1 simulator for different bias currents of OTA

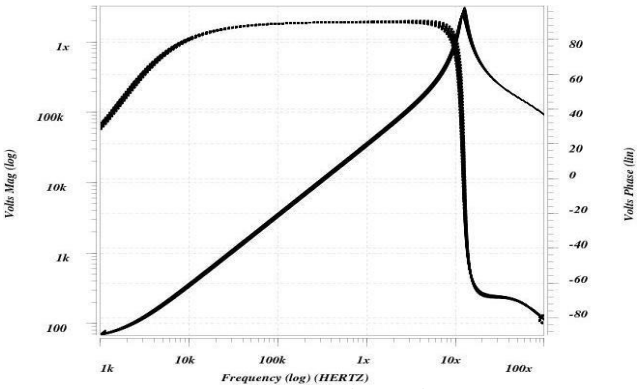


Fig. 7: The Monte Carlo analysis of GIS-1 for 10% variation in capacitance value

Next, the grounded FDNR circuit is examined by selecting C_1 = C_2=100pF and plotting the magnitude phase relationship for different bias current of (10µA, 30µA, 50µA) as shown in Fig. 8. It can be deduced the FDNR works well. The value of the D_{Eq} for a bias current of 50µA is found to be 54.171aF.

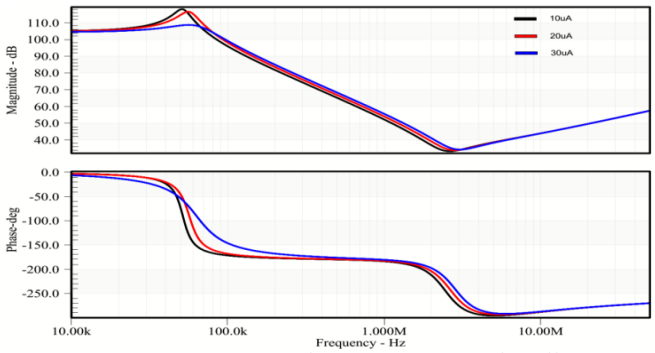


Fig. 8: The magnitude and Phase of the grounded FDNR for different bias currents

At last the grounded capacitor simulator is validated. By choosing R_1 = **2**kΩ, C_1=50pF and $\mathbf{I_{bias1}}$=20µA. The theoretical value of the capacitance is calculated to be 135.42pF. The ideal and simulated plot is shown in Fig. 9.

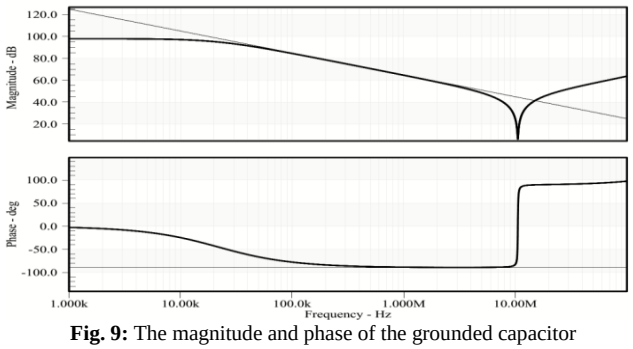


Fig. 9: The magnitude and phase of the grounded capacitor

The range of operation of all the simulators can be further extended by reducing the effects of VDCC parasitic elements by adopting the techniques described in [7, 17, 24].

In order to validate the functionality of the proposed impedance simulators they are employed in different filter applications. The GIS-1 is utilized in designing an RLC current mode filter structure [26] as presented in Fig. 10. The filter is designed for a frequency of 1.59MHz by selecting the passive components values as

L=1mH, C=10pF, R=10K. To get $\mathbf{L_{eq}}$=1mH for GIS-1, the values of passive components are set at $\mathbf{R_1}$ =5K and $\mathbf{C_1}$ =55pF and I_{bias1}=50µA. The ideal and simulated low pass (LP), band pass (BP) and high pass (HP) responses of the filter are shown in Fig. 11. It can be deduced from the figure that the ideal and simulated responses closely follow each other.

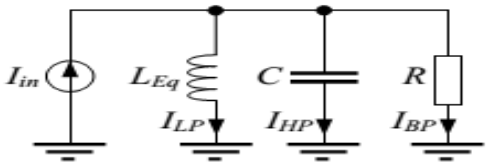


Fig. 10: Parallel RLC current mode filter [26]

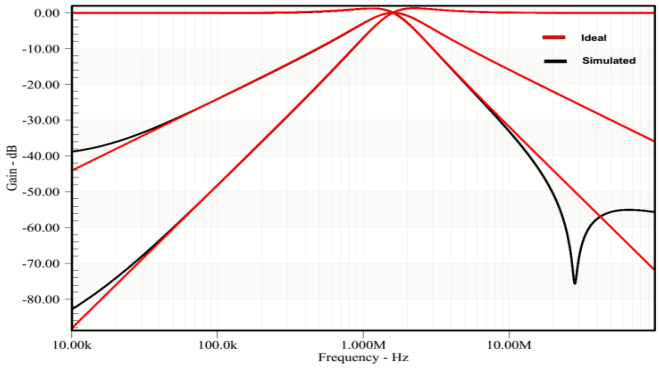


Fig. 11: Frequency response of the current mode RLC filter

An RLC resonance circuit configuration is given in Fig. 12. It is designed to validate the parallel RL simulator circuit GIS-2 and grounded capacitor simulator GC. The parallel RL in the passive circuit is replaced by the GIS-2 and capacitor is replaced by GC simulator. The expressions for input impedance and resonance frequency are calculated as given in Equations 5-6. The passives values are chosen as R=3.610 kΩ, L=0.722mH, $\boldsymbol{C_{eq} = 135.42}$pF which yielded a pole frequency of 508.991KHz. The simulated and ideal responses of the filter are presented in Fig. 13.

$$\mathbf{Z_{in}} = \frac{{}^{s}/_{C_{eq}}}{s^2+\left(\frac{s}{R_1 C_{eq}}\right)+\left(\frac{1}{L_1 C_{eq}}\right)} \quad (5)$$

$$\boldsymbol{\omega_o} = \frac{1}{\sqrt{L_1 C_{eq}}} \quad (6)$$

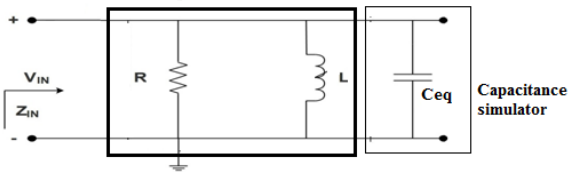


Fig. 12: RLC resonance circuit structure

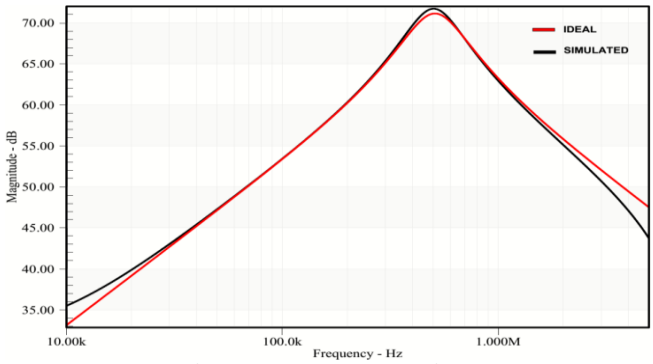


Fig. 13: Impedance–frequency characteristics of the parallel resonance circuit

To illustrate the feasibility of the FDNR it is used to design third order Butterworth low pass filter. The filter with passive components is presented in Fig. 14 (a). The component values are selected as follows: L_1=L_2=7.9577µH , $\boldsymbol{C_1 = 6.366}$ nF and $R_A = R_1 = \mathbf{50\Omega}$ to get a cutoff frequency of 1MHz. Bruton transformation with magnitude scaling constant of ($\mathbf{k_m = 10^9}$) is used to transform the passive RLC filter circuit into CRD filter. The transformed filter circuit is shown in Fig. 14 (b). where L is replaced by R, C by FDNR and R by C. The values of the components are $\boldsymbol{C_L = C_A = 20\,pF}$, R_1=R_2=7.9577k$\mathbf{\Omega}$ and D_1=$\mathbf{6.3662}$aF (by selecting C_1=23.50pF and C_2=50pF in FDNR simulator at $\mathbf{I_{bias1}}$=20µA). It is clear from the Fig. 15 that the theoretical results closely follow the simulation results.

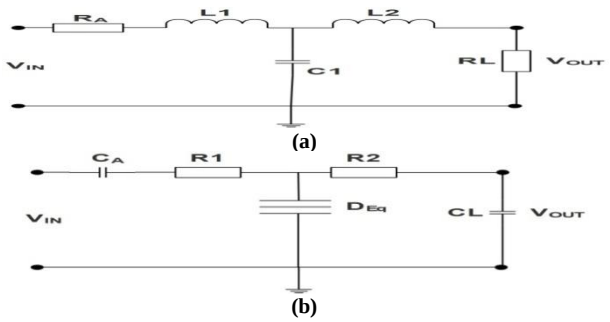


Fig. 14: The structure of the third order Butterworth low pass filter (a) using passive components (b) transformed structure using FDNR

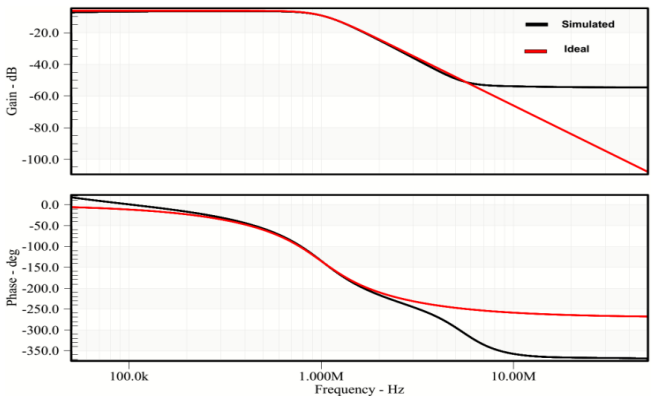


Fig. 15: The gain and Phase of the third order Butterworth low pass filter

5. Conclusion

In the presented research, three new circuit configurations for realizing lossless and lossy grounded inductance simulators are proposed. Also two topologies for realizing grounded FDNR and grounded capacitance simulators are developed. All the proposed simulators are minimum component implementation as they re-

quire only one VDCCII and two passive components. All the simulator structures use grounded capacitor which is advantageous in noise cancellation and fabrication. Moreover, all the designs are electronically tunable and none of the design requires components matching condition. Monte Carlo analysis is also performed to validate their stability. The proposed impedance simulators are validated by using them in design of voltage and current mode filters. The simulations in 0.18µm TSMC technology are performed to support the theoretical findings. Adequate number of simulation results are given to justify the feasibility of the proposed designs.

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