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Research paper

Design of low power and high speed implicit pulse flip-flop and its application

Kuruvilla John [1] *, Vinod Kumar R. S [1], Kumar S. S [2]

[1] Department of Electronics and Communication Engineering, Noorul Islam Centre for Higher Education, Thucklay, Tamil Nadu, 629180, India
[2] Department of Electronics and Instrumentation Engineering, Noorul Islam Centre for Higher Education, Thucklay, Tamil Nadu, 629180, India
**Corresponding author E-mail: kuruvilla08@gmail.com*

Abstract

In this paper, a new power efficient and high speed pulsed-triggered flip-flop in implicit style with conditional pulse enhancement and signal feed-through (CPESFTFF) is proposed. This novel architecture is presented for the pulse-triggered D-FF in the CMOS 90-nm technology. Two important features are embedded in this flip-flop architecture. Firstly, a conditional enhancement in width and height of the triggering pulses by using an additional pMOS transistor in the structure is done. Secondly, a modified signal feed-through mechanism which directly samples the input to output by using an nMOS pass transistor is introduced. The proposed design achieves better speed and power performance by successfully solving the longest discharging path problem. The simulation results show that the proposed architecture has improvement in terms of power consumption, D-to-Q delay, and Power Delay Product Performance (PDP) in comparison with other conventional P-FF architectures. A 3-bit up counter is also implemented using proposed P-FF.

Keywords: *High Speed; Implicit; Low Power; Pulse Flip-Flops; Signal Feed-Through.*

1. Introduction

Power efficient design is one of the most important concerns in today's electronics [1], [2]. This issue becomes more important when facing integrated circuits [4]. One of the basic elements used for storage purposes is Flip-Flops (FFs) [3], [4]. Studies proved that above 25% of total power generated by the system is consumed by the clock generator [5]. Pulse-triggered FFs (P-FFs) play a fundamental role in the performance of digital structures. In high speed applications, P-FF exhibits better performance than conventional master-slave FF designs [5], [6]. If the structure of P-FF designs with conventional master-slave FFs are compared, it can be observed that in P-FF, only single latch is present but in conventional FFs two latches are present, namely master and slave latch [7]. Therefore, the area will be less for P-FF designs and hence it can be used in low power applications [8], [9].

The two basic parts in the structure of a P-FF design are pulse generator and latches [5]. Pulse generator is responsible for generating the triggering pulses, which may be generated either at any edges of clock signals or at both edges of clock signals. The latch structure is responsible for latching or sampling the input data into the output according to the triggering pulses generated. Based on the triggering mechanism P-FFs are of single edge triggered and double edge triggered types [10].

P-FFs are classified as implicit and explicit types based on the connection of pulse generator and latch structure [5], [10]-[12], [22]. In former case, pulse generator is inbuilt in the latch structure and in latter it is external to the latch structure. It is estimated that implicit P-FFs are more power efficient than explicit types [5]. It is due to the fact that controlling of discharging path takes place in implicit P-FF but in explicit P-FF physical generation of the pulse needed [2], [20]. However, explicit P-FF has advantage of sharing of pulse generator among neighboring latches [5], [10]. This sharing reduces the power overhead of external pulse generator. Thus, explicit P-FFs become more energy efficient than implicit P-FFs. In explicit P-FF double edge, triggering can be implemented easily but it is very difficult to implement in implicit P-FF [5], [12]. Dynamic power consumption directly depends on the frequency of operation [13]. In double edge-triggered FFs, half of the frequency will be reduced due to sampling of data at both edges of clock signals. This frequency reduction leads to power saving [14]. In explicit P-FF the length of discharging path will be less than that of implicit P-FF. This leads to reduction in power consumption [10], [11]. Dynamic behavior of a P-FF causes lot of wastage in power due to unnecessary switching activities [16]-[19].

In this paper a new implicit type of pulse flip-flop is described which can be used in low power and high-speed applications. This P-FF is having the embedded features of conditional pulse enhancement [5] and signal feed-through [15]. These features are implemented by adding additional pMOS transistors and N-type pass transistor. When this latch and pulse generator combined together, a new P-FF design is formed with reduced power, improved speed and better power-delay-product (PDP) performances.

The paper is organized as follows: While Section 1 briefs an introduction of P-FFs; Section 2 describes various conventional P-FF designs. It includes signal feed-through flip-flop (SFTFF) [15], [21] and conditional pulse enhancement flip-flop (CPEFF) [5], [22]. Section 3 describes proposed implicit P-FF design. Section 4 compares the PFFs and presents the results after cadence simulation. The paper concluded in Section 5.

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2. Conventional pulse flip-flop designs

The operations of two conventional P-FFs are discussed in this section. It includes (i) signal feed-through FF (SFTFF), and (ii) conditional pulse enhancement FF (CPEFF).

2.1. Signal feed-through flip-flop

Fig.1 shows the circuit diagram of explicit pulsed signal feed-through flip-flop (SFTFF) [15], [21]. Inverters I1, I2, I3, I4 and NAND gate forms the explicit pulse generation unit. The true single-phase clock latch structure of this explicit P-FF is embedded with pseudo-nMOS logic and signal feed-through technique [15], [21]. In this P-FF, an N-type pass transistor N4 driven by clock pulse is used for direct feedthrough of input to output. The pass transistor N4 provides the path for discharging of the output node Q, and also provides additional driving power to output node Q during LOW to HIGH transitions of input data [15], [21].

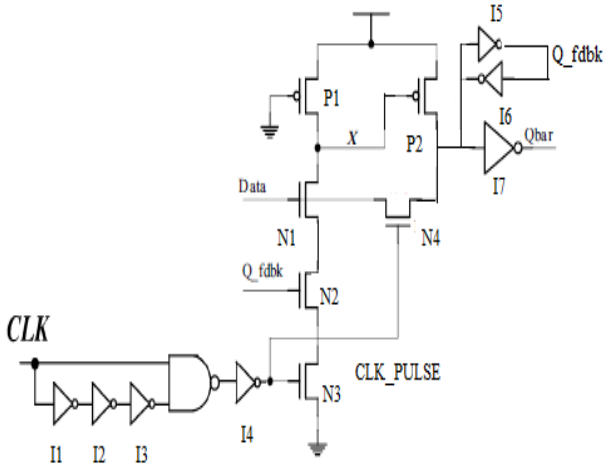


Fig. 1: Circuit Diagram of SFTFF.

2.2. Conditional pulse enhancement flip-flop

Conditional pulse enhancement flip-flop (CPEFF) [5] shown in Fig.2 over comes the drawbacks of SCCERFF design. In CPEFF transistors N2 and N3 forms a two input AND gate of N-type pass transistor logic (PTL) style [22]. An additional pMOS transistor P3 is used for enhancing the width and height of triggering pulses, when the input data makes a LOW to HIGH transition [5], [22].

The specialty of N-type PTL is that it transmits only weak ones, i.e. if VDD is the input then VDD-Vtn is the output. The value of pulse signal is zero at node Z in most of time other than transition edges of clock signals, because of the two complementary inputs of the AND gate [5]. When the clock signal falls to LOW value then the pulse at node Z reaches temporary floating state. Both transistors N2 and N3 are turned on at the rising edges of the clock signal. This passes a weak logic high value (VDD-Vtn) to node Z, which causes turning ON of transistor N1 by a time span inserted by the delay of inverter I1 [5].

In CPEFF the conditional enhancement in the width and height of triggering pulses at node Z occurs only when the output Q of the FF is subjected to a change from LOW to HIGH value [5]. The formation of longest discharging path occurs, when both input data and inverted output Qbar are HIGH. Transistor P3 is used to increase the speed of discharging. Turning ON of transistor P3 is not possible until the node X is discharged to LOW (Vtp) value. An additional boost in the value of triggering pulse at node Z from VDD-Vtn to VDD occurred when pMOS transistor P3 turns ON [5].

After the rising edge of the clock signal, the delay of inverter I1 drives the value of triggering pulse at node Z back to zero through nMOS transistor N3. This will turn OFF the discharging path. CPEFF is having better performance in power and speed than those conventional P-FFs schemes with pulse width control issue [5]. In this flip-flop also, unwanted switching activities takes place at sleep/idle mode of operation. This will increase the total power consumption and thus degrades the performance.

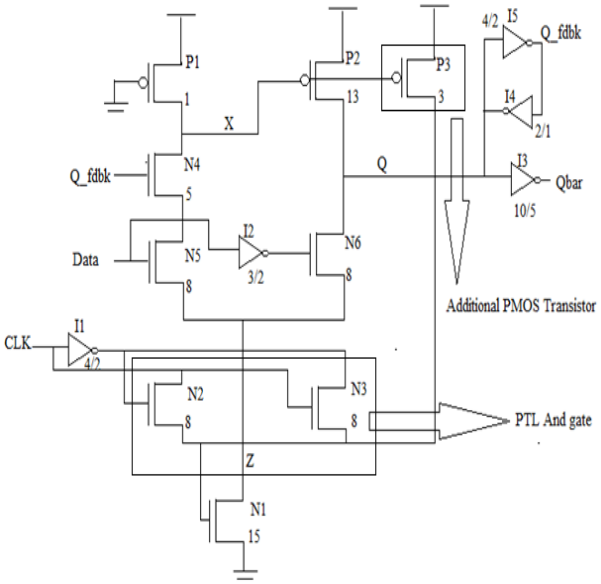


Fig. 2: Circuit Diagram of CPEFF.

3. Proposed pulse flip-flop design

The proposed implicit P-FF design is shown in Fig.3. This P-FF is having better performance in speed and power when compared with conventional FFs. This design is having the combined features of conditional pulse enhancement FF [5] and signal feed-through FF [15].

The enhancement in width and height of triggering pulse when output changes from LOW to HIGH value and the direct coupling of input to output are the key features of this P-FF. In the proposed design nMOS transistors N2 and N3 forms N-type pass transistor logic (PTL) based AND gate. The inverter I1, PTL AND gate and transistor N1 forms the pulse generation unit. The triggering pulses are generated at node Z during rising edges of clock signals. This P-FF act like a single edge triggered FF. The input data is transmitted to output Q through the nMOS pass transistor N6 during rising edges of clock signals. The transistor N6 is controlled by triggering pulses generated at node Z. The pMOS transistor P1 and nMOS transistor N4, N5 and N1 forms three input pseudo-nMOS NAND gate. This will save the charge keeper circuit for the internal node X. The pass transistor N6 provides the path for discharging of the output node Q, and also provides additional driving power to output node Q during LOW to HIGH transitions of input data.

When input data makes a LOW to HIGH transitions, then internal node X must discharge through the nMOS transistors N4, N5, and N1. This is the longest discharging path at latch structure. During normal conditions other than longest discharging path occurs, then node Z value produced by N type PTL AND gate is VDD-Vtn. The longest discharging path is formed when both input data and output are HIGH. When longest discharging path occurs, then transistor P3 is used to increase the speed of discharging. Transistor P3 is in the turned OFF state until node X is pulled down to LOW value. Turning ON of transistor P3 takes place when node X is discharged to Vtp (threshold voltage required to turn ON pMOS transistor) below the VDD. The turning ON of transistor P3 provides additional boost to triggering pulse at node Z from VDD-Vtn to VDD. This boosted pulse reaches the gate of transistor N6 and enhance the speed of operation.

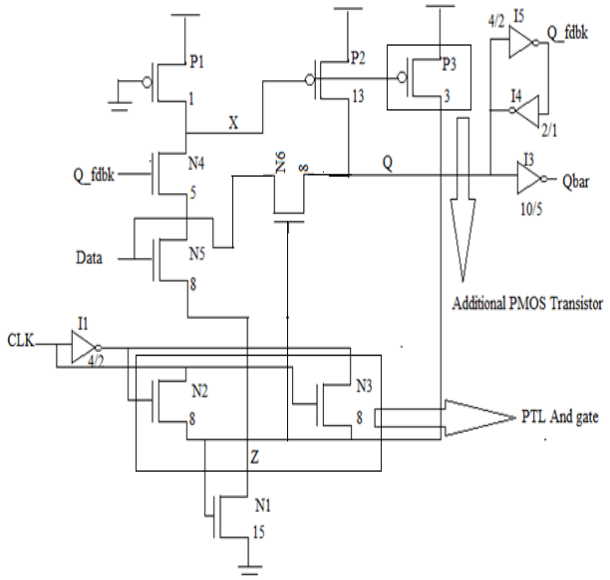


Fig. 3: Circuit Diagram of Proposed P-FF.

The shutdown of discharging path takes place after the rising edge of the clock signals. During this time, the delay of inverter I1 drives PTL AND gate output at node Z back to zero and closing of discharging path takes place. The node X voltage values increases above Vtp and turns OFF pMOS transistor P3. Thus, the embedded features like conditional enhancement in width and height of triggering pulses by using an additional pMOS transistor and a pulse-triggered structure with a modified signal feed-through mechanism which directly samples the input to output by using an nMOS pass transistor increases the speed and power performance of proposed design when compared with conventional implicit and explicit P-FFs.

As an application a 3-bit synchronous up counter [23], [24] is designed using proposed P-FF design and its power performance is compared with CPEFF based counter. This counter design requires three flip-flops and some logic gates. The expressions for the inputs to each flip-flop are represented as in equation (1), (2) and (3) [23], [24].

$$D0 = Q0' \quad (1)$$

$$D1 = Q1'Q0 + Q1\,Q0 \quad (2)$$

And

$$D2 = Q2'Q1Q0 + Q2Q1' + Q2\,Q0' \quad (3)$$

4. Experimental results and discussions

The proposed and conventional P-FFs are simulated in CMOS 90nm technology with the power supply of 1.5V and temperature of 298K. Cadence software is the simulation tool used to implement the various P-FF designs.

Fig.4 shows the simulation waveform of CPEFF. CPEFF acts like a single edge triggered FF design. The output Q is changed according to the data applied at the input during rising edges of clock signals. In CPEFF, conditional enhancement in width and height of triggering pulses takes place when the output Q makes a LOW to HIGH transition.

The simulation waveform and simulation model of proposed P-FF is shown in Fig.5 and Fig.6 respectively. Proposed P-FF is embedded with two techniques such as conditional pulse enhancement and signal feed-through mechanism. From the waveform it is clear that the triggering clock pulses at node Z will be generated at the rising edges of clock signal. The input data is detected at the output Q during rising edges of clock signal. This P-FF act like a single edge triggered FF.

Fig.7. shows the conditional enhancement in width and height of triggering pulses at node Z. In normal operation the pulse width and height at node Z are 0.74ns and 780mV respectively. When conditional pulse enhancement takes place then the enhanced width and height of triggering pulses at node Z are 1.14ns and 1V respectively. From the simulation results it is clear that the enhancement in width and height of triggering pulses are 35.08% and 22% respectively when compared with normal condition. This happens due to the additional voltage supplied by pMOS transistor P3.

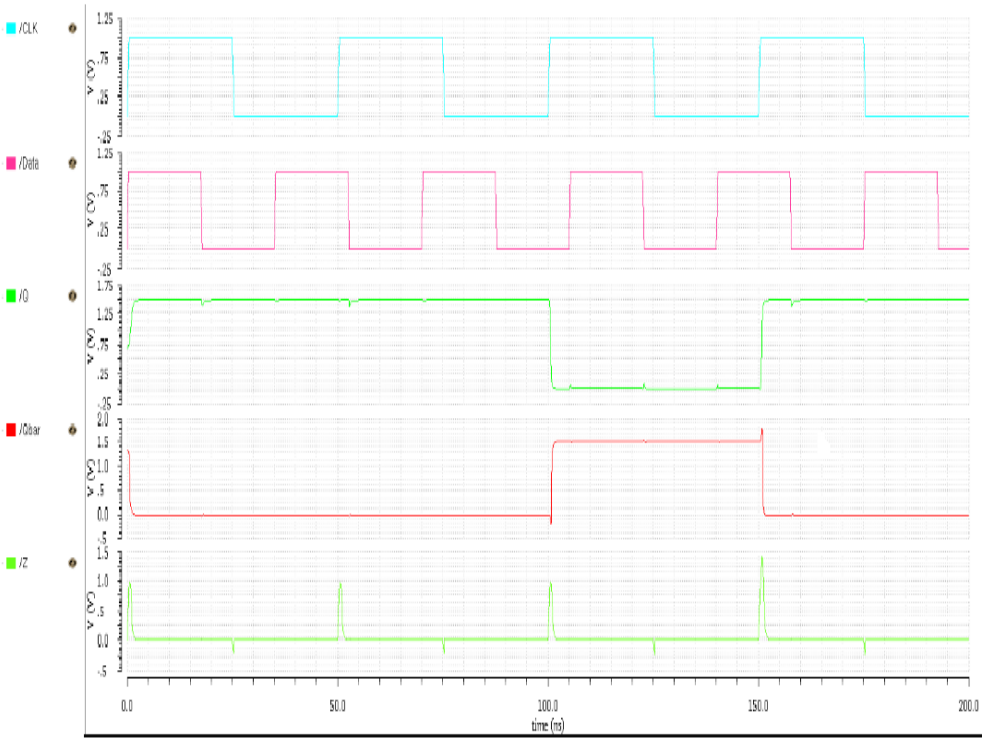


Fig. 4: Simulation Waveform of CPEFF.

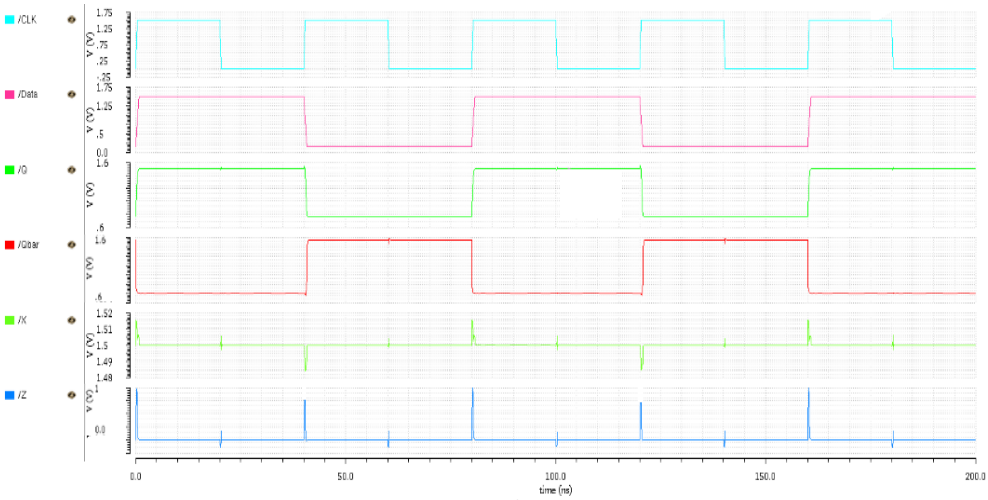


Fig. 5: Simulation Waveform Proposed P-FF.

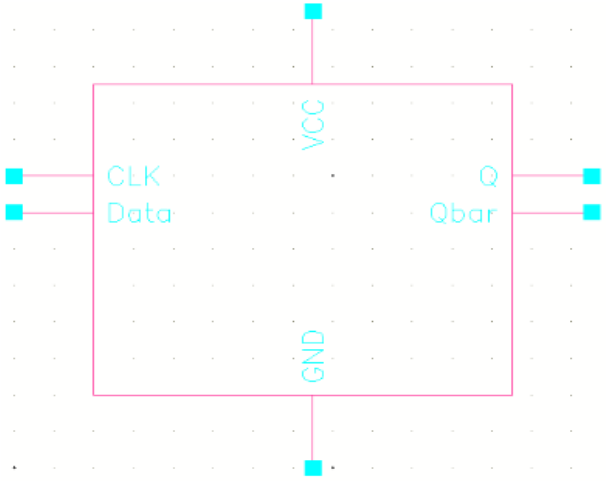


Fig. 6: Simulation Model of Proposed P-FF.

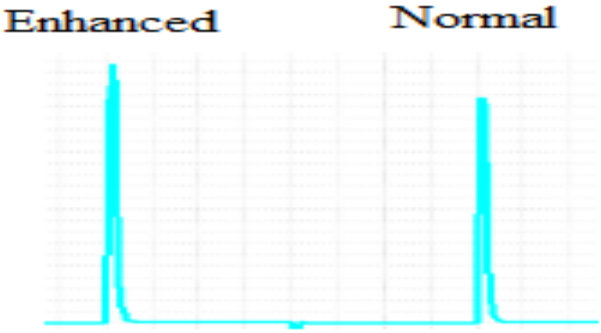


Fig. 7: Conditional Pulse Enhancement in Proposed P-FF.

4.1. Comparison with existing pulse-flip-flops

To assess the performance of proposed P-FF, other designs were simulated under similar conditions. Table 1. shows the comparison of various performance parameters of proposed P-FF with other conventional P-FF designs. It includes transistor count, power consumption, Data to Q delay, CLK to Q delay and power-delay product performance. From Table 1 it is clear that proposed P-FF have better power, speed and power-delay product performance than conventional P-FF designs.

Table 1: Observation of Design Parameters

P-FFs	SFTFF	CPEFF	Proposed
Number of transistors	24	19	17
Power Consumption (µW)	107.59	71.57	65.02
Data to Q Delay (ps)	300	331.24	174.28
CLK to Q Delay (ps)	129.36	142.83	75.14
Power-Delay Product (fJ)	32.27	23.70	11.33

Fig.8. shows the power comparison of various P-FFs. The proposed P-FF is having best power performance due to its signal feed-through feature and conditional pulse enhancement scheme. In proposed P-FF, the longest discharging path problem can be solved by directly coupling input data to output Q with the help of nMOS pass transistor controlled by triggering pulses generated at node Z. The conditional pulse enhancement scheme increases the speed of latching of data without increasing the delay of inverters and width of transistors used at the pulse generator. Thus, the proposed P-FF is having better power performance than conventional implicit P-FFs. The proposed P-FF is having 9.15% advantage in power consumption and 47.38% advantage in input to output delay when compared with CPEFF. Fig.9. shows Data to Q delay comparison of various P-FFs. Fig.10. shows power-delay product comparison of various P-FF designs. The proposed P-FF is having advantage of 52.19% in power-delay product performance when compared with CPEFF due to its reduced power and delay of operation.

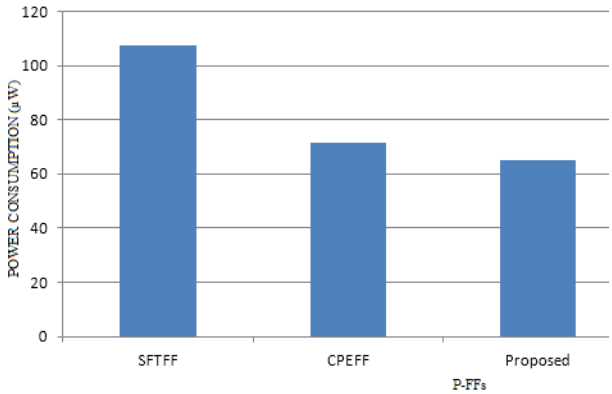


Fig. 8: Comparison of Power Consumption in P-FFS.

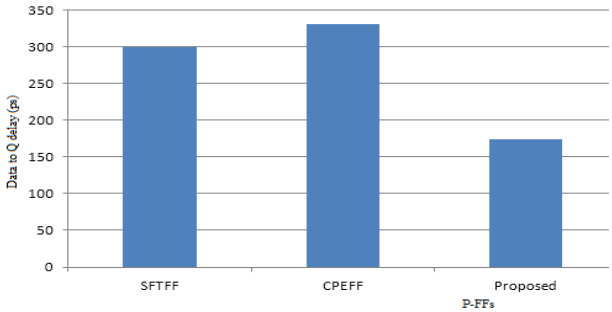


Fig. 9: Comparison of Data to Q Delay in P-FFS.

4.2. Application of proposed pulse flip-flop

Fig.11. and Fig.12. shows the simulation model and simulation waveform of a 3 bit synchronous up counter using proposed P-FF. The counter counts during rising edges of clock signals. Cadence simulation result shows that counter using proposed P-FF is having power consumption of 182.98µW. Counter using conventional CPEFF is having power consumption of 198.28µW. The proposed P-FF based counter is having an advantage of 7.17% in power when compared with that of CPEFF based counter. The proposed P-FF based counter is having an advantage of 42.17% in power delay product when compared with that of CPEFF based counter.

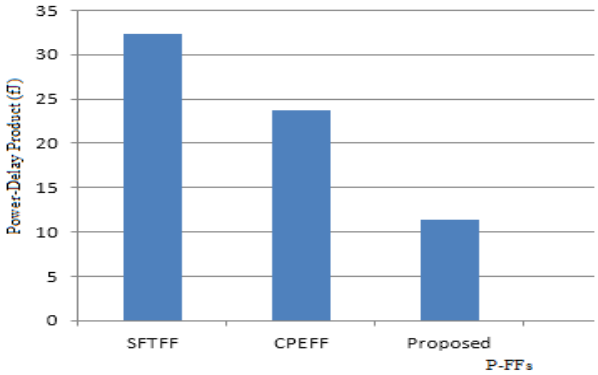


Fig. 10: Comparison of Power-Delay Product in P-FFS.

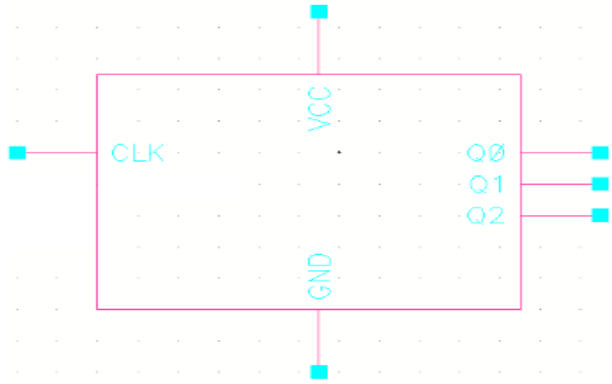


Fig. 11: Simulation Model of Proposed P-FF Based Counter.

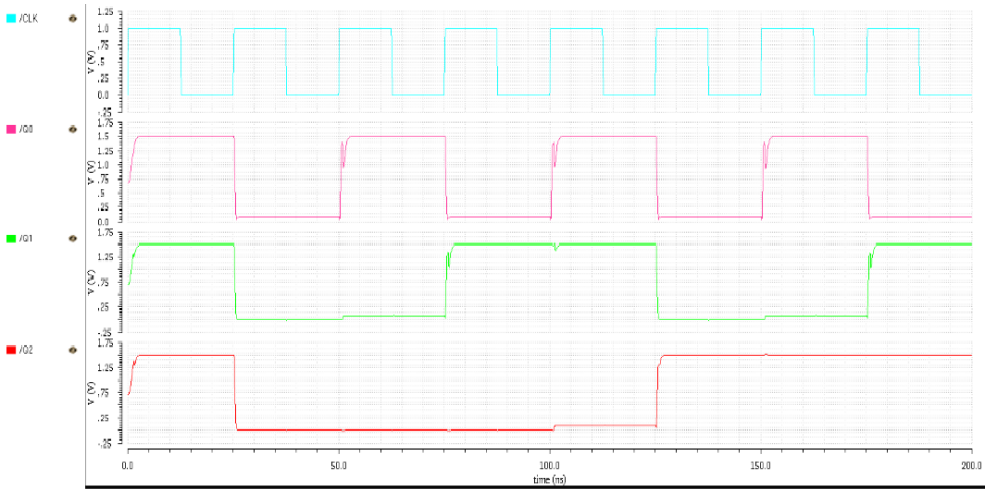


Fig. 12: Simulation Waveform of Counter Using Proposed P-FF.

5. Conclusions

In this, paper a novel low power and high speed implicit P-FF is presented with two key features. The first feature is conditional enhancement in the width and height of designs triggering pulse when output changes from LOW to HIGH value by using additional pMOS transistor. The second feature is directly coupling the input data to the output Q through an nMOS pass transistor. The conditional enhancement in triggering pulses and signal feed-through mechanism reduces longest discharging path problem and thereby reducing the power consumption and increasing the speed of operation. Cadence simulation results indicate that the proposed P-FF design is having better performance in power, Data to Q delay and power delay product (PDP) when compared with conventional P-FFs. Power reduction techniques such as Clock Gating concept, Multiple Threshold CMOS (MTCMOS) concept, etc can be applied to the proposed P-FF design for further reduction in power consumption.

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