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Research paper

Energy Efficient VLSI Architecture for Variable Iterative 4G LTE Turbo Decoder

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Abstract

The Long Term Evolution (LTE) networks main objective is to support the next generation wireless communication systems. But most of the LTE approaches are suffer from decoding latency. Hence results in drop of data rate and this is not supported by the 4G LTE standards. To overcome this few parallel architectures has been introduced with the cost of power and silicon chip area. One promising decoding algorithm to overcome the decoding latency is Maximum a Posteriori (MAP) algorithm. The MAP has two computationally challenging α and β units. These two units have critical path and are to be reduced. A novel architecture for Add-Compare-Select (ACS) is proposed with clock gating techniques to reduce the unnecessary power dissipation across the recursive computational units. The proposed technique is applied with max-log MAP algorithm to precise the approximation. The overall design in implemented in a 45nm CMOS technology and results in 179.2mW of power dissipation which results in 34.6% less power compared to reported design while monitoring the moderate or same throughput level.

Keywords:*Long Term Evolution (LTE); Add Compare Select (ACS); VLSI; Max-Log MAP Algorithm; Log- Likelihood Ratio (LLR).*

1. Introduction

In communication system the channel coding plays an important role providing the correction of transmission errors posed by the channels. The turbo codes [2] are capable of facilitating the near-capacity transmission throughputs, leading to state-of-art mobile telephony standards such as WiMAX [3] and LTE [4]. The turbo decoders show the bottleneck in near real time throughput of interactive communication system. The mobile telephone standards are dramatically increased in the throughput over the past two decades, from multi-Kbps-to-multi Gbps. To support the demands many turbo decoder architecture are proposed [5]-[9]. The current research is nearly fulfilling the need of throughput at high/ ultra-high speed with low latencies with respect to next generation wireless standards. But achieving the low power design with the required throughput is always challenging and it is missing.

The turbo decoders give better execution compared to the SOVA (Soft Output Viterbi Algorithm) in Bit Error Rate (BER) [10]. The parallel turbo decoder delivers the high throughput with the cost of large silicon area and the high decoding complexity with latencies [11]. Other design components of parallel turbo decoder architecture are two MAP decoder, deinterleaver and interleaver [12].The use of endless MAP decoders causes the expansion of the design and becomes versatile in nature, from now on only two MAP decoders are represented as an ideal.

In the proposed turbo decoder two approaches are so specific, variable number of iteration based on the error correction and decoding of the data and clock gating methodology. The clock gating framework is used across two MAP decoders. An individual decoder is in compiling and the other decoder becomes inactive, so that the clock of the latent decoder is gated to reduce the extra power dissipation.

Rest of the paper is framed as sections-II clears the structure of turbo decoder. Section III reveals the proposed technique and the low-power framework. Finally section IV shows the implementation on the CMOS technology followed by the demonstration of the results.

2. Turbo decoder structure and algorithm

Turbo codes are widely used in iterative decoding methods to parallel concatenated coding. The standard structure of the decoder is shown in Fig 1. The structure consists of two decoders, interleaver and deinterleaver. In log-MAP decoder shows four segments: a Branch Metric Unit (BMU) for calculation, a Forward State Metric Unit (FSMU) to check, a Backward State Metric Unit (BSMU) to figuring and log likelihood Ratio (LLR) for estimation. The process of computation of a log-MAP decoder is shown in the flowchart of Fig 2.

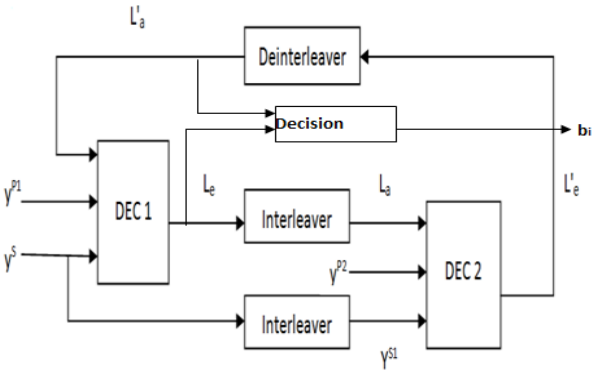


Fig. 1: Standard Decoding Structure of Turbo Codes [1].

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The received signal is quantized in order to scale the analog signal. Digitized signal is passed to branch metric unit for calculation, where the unit has Branch Metric Unit (BM) and FSMU storage. The stored branch metric values are computed through Backward State Metric Unit (BSMU) and probabilities are estimated.

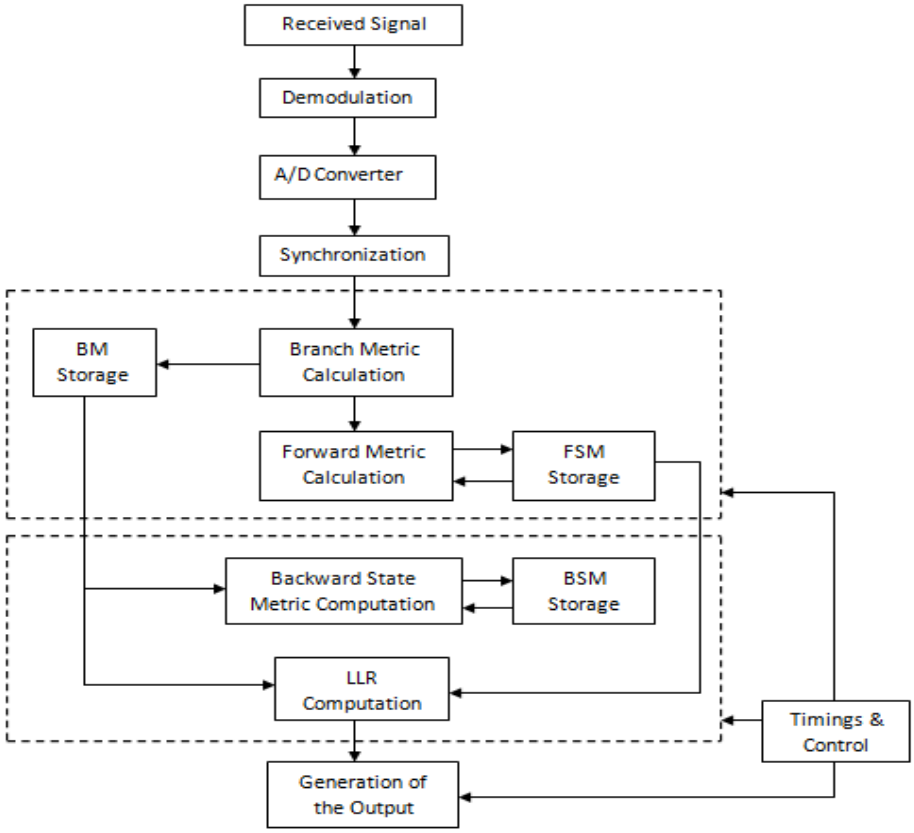


Fig. 2: Log-MAP Decoder Computation Flow.

The Log likelihood Ratio (LLR) of log-MAP decoders with information bit u_k can be written as

$$L(u_k) = \log \frac{P(u_k=1/y_k)}{P(u_k=0/y_k)} (1)$$

Where y_k= (y^s_k,y^p_k), assuming that the design uses the AWGN channel [2] for transmission of information and BPSK modulation is considered. The resultant expression for the operation becomes

$$L(u_k) = \log \frac{\sum_{(s',s)u_{k=1}} P(S_{k-1}=S',S_k=S,y_k)/P(y_k)}{\sum_{(S',S),u_{k=0}} P(S_{k-1}=S',S_k=S,y_k)/P(y_k)} (2)$$

From BCJR (Bahl-Cocke-Jelinek-Raviv) algorithm [1],

$$P(S', S, y_k) = \alpha_{k-1}(S') * \gamma_k(S', S) * \beta_k(S) (3)$$

Where $\alpha_k(s)$ is taken as forward recursive probable value, $\beta_k(s)$ refers to backward recursive probable value and $\gamma_k(s', s)$ branch transfer probable notation. The values of $\alpha_k(s)$ and $\beta_k(s)$ are recursively computed and normalization is done to avoid the occurrence of overflow in calculation.

$$\alpha' k(S) = \frac{\sum_{S'} \alpha'_{k-1}(S')\gamma_k(S',S)}{\sum_S \sum_{S'} \alpha'_{k-1}(S')\gamma_k(S',S)} (4)$$

$$\beta'_k(S) = \frac{\sum_{S'} \beta'_{k-1}(S')\gamma_k(S',S)}{\sum_S \sum_{S'} \beta'_{k-1}(S')\gamma_k(S',S)} (5)$$

From the above, it is derived that

$$\alpha(u_k) = \ln \frac{\sum_{S+} \alpha'_{k-1}(S') * \gamma_k(S', S) * \beta'_k(S)}{\sum_{S-} \alpha'_{k-1}(S') * \gamma_k(S'.S) * \beta'_k(S)}$$

$$= \ln \frac{\sum_{S+} \exp(\ln \alpha'_{k-1}(S') + \ln \gamma_k(S', S) + \ln \beta'_k(S)}{\sum_{S-} \exp(\ln \alpha'_{k-1}(S') + \ln \gamma_k(S', S) + \ln \beta'_k(S))}$$

$$= \max^*\{\sum_{S+} \exp(\ln \alpha'_{k-1}(S') + \ln \gamma_k(S', S) + \ln \beta'_k(S))\} - \max^*\{\sum_{S+} \exp(\ln \alpha'_{k-1}(S') + \ln \gamma_k(S', S) + \ln \beta'_k(S))\} (6)$$

Where max* operation [23] is expressed as

$$\max^*(x, y) = \ln(e^x + e^y) (7)$$

If there is a large difference between x and y, then Jacobean algorithm is used to simplify and approximated later.

$$\ln(e^x + e^y) = \max(x, y) + \ln(1 + e^{-|x-y|}) \approx \max(x, y) (8)$$

Applying the above simplification to the expression (6) and the obtained expression is referred Max-Log MAP algorithm. It is observed that from the above sequence of expressions, at the cost of performance deprivation algorithm can simplify the computation. So the modified version becomes

$$(\sum_{i=1}^n e^{x_i})[n + (n-1) + \cdots + 1] \leq n * [ne^{x_1} + (n-1)e^{x_2} + \cdots + e^{x_n}] (9)$$

Let $x_1 \geq x_2 \geq \ldots . \geq x_n$, the inequality is equivalent to

$$(\sum_{i=1}^n e^{x_i})[n(n+1)/2] \leq ne^{x_1} * [n + (n-1)e^{x_2-x_i} + \cdots + e^{x_n-x_1}] (10)$$

After applying the logarithm for the above inequality on both the sides, the expression becomes

$$\ln(\sum_{i=1}^n e^{x_i}) \leq \ln[2/(n+1)] + x_1 + \ln[n + (n-1)e^{x_2-x_1} + + e^{x_n-x_1}] (11)$$

At Right Hand Side of the expression only two terms in the logarithm are considered and this simplifies to
$\max^*(x_1, x_2, \cdots, x_n) \approx \max(x_1, x_2, \cdots, x_n) + \ln[2n/(n+1)] + \ln[1 + (n-1)/n(n-1)e^{x_2 - x_1}]$(12)

From the expression (12) a second term in right of it is constant and which will not influence the consequent computation. Finally the customized expression is written as

$\max^*(x_1, x_2, \cdots, x_n) \approx \max(x_1, x_2, \cdots, x_n) + \ln[1 + (n-1)/n(n-1)e^{x_2 - x_1}]$(13)

Once L (u_k) is calculated, the corresponding extrinsic information is

$$L_e(u_k) = L(u_k) - L_c y_k{}^s - L_a(u_k) \quad (14)$$

Through the multiplication with $L_c(u_k)$, the performance of the max-log-MAP algorithm is gradually increased with a scale factor λ.

$$L_e'(u_k) = \lambda(L(u_k) - L_c y_k{}^s - L_a(u_k)) \quad (15)$$

3. Proposed low-power turbo decoder

3.1. Clock gating

The control flag is designed for the operation of this component, when many delayed cycles are running, which are not required. The pipeline co-ordinates in favor of, once the device quits running and eventually the combinational circuit connecting registers are additionally wiped out and short energy be able to accomplished. But the Gating requires an extra circuit component to produce low power signals.

3.2. Number of iterations can be adjustable

Once the decoding in completed, the number of iterations are not fixed, so it will stop the process immediately. This results in saving the power and reduces the computation time taken for unnecessary decoding even after the processing is gets over.

3.3. Floating inputs can be blocked

The yields of RAMs are skimming and the exception of accompanied by read or compose function. Subsequently, it ought to be avoided to decrease state power scattering. The occurrence piece coasting inputs utilizing AND or OR entry ways by way of command sign at 0.

4. Implementation results

The proposed low-power turbo decoder design is coded in verilog and simulated to check the coverage through a test bench for verification. The complete design is implemented using Cadence® Integrated Tool platform with 45nm generic process design kit (gpdk) library set. The turbo decoder top module RTL schematic is shown in Fig.3.

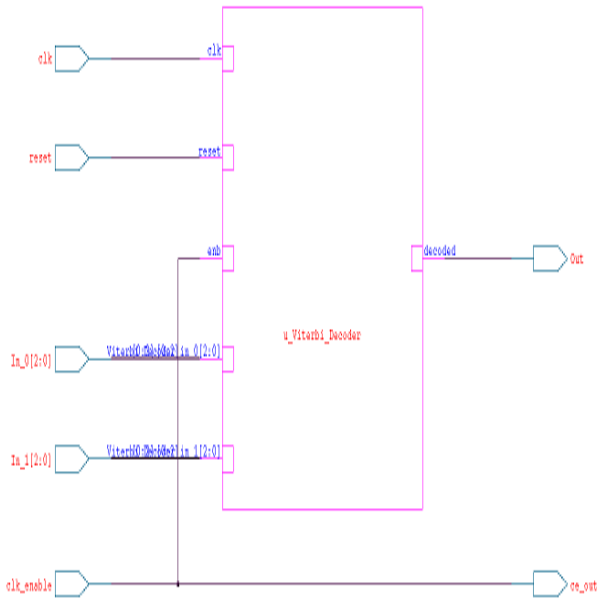


Fig. 3: Top Module RTL Schematic of Turbo Decoder.

The schematic of Branch Metric (BM), State Metric (SM) and Add-Compare-Select (ACS) are represented through the Cadence design compiler with the following RTL synthesis (gate level) diagram as shown in Fig.4.

4.1. Comparison

The proposed design achieved the power efficiency through the clock gating and the variable or adjustable iteration techniques. The obtained results are compared with the existing work. The clearly shows that there is a 34% of power consumption is reduced from the proposed design and it matches the data rate for the high speed wireless application. Table 1 shows the comparison of various parameters.

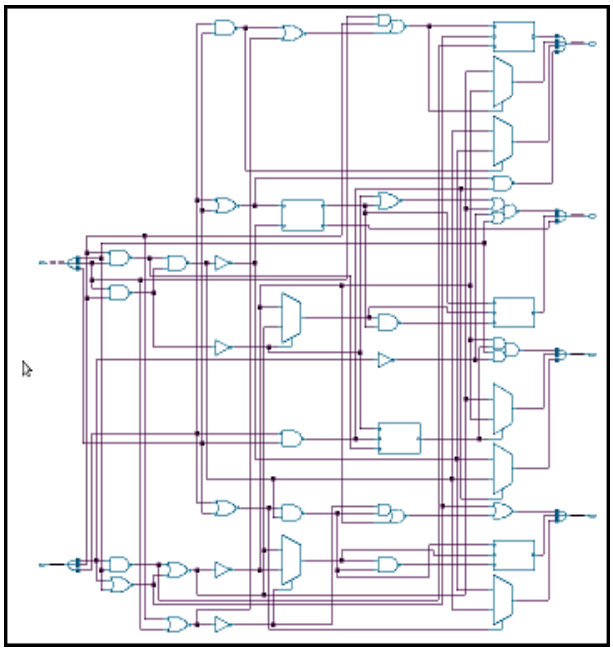


Fig. 4:RTL Schematic of Branch Metric Unit.

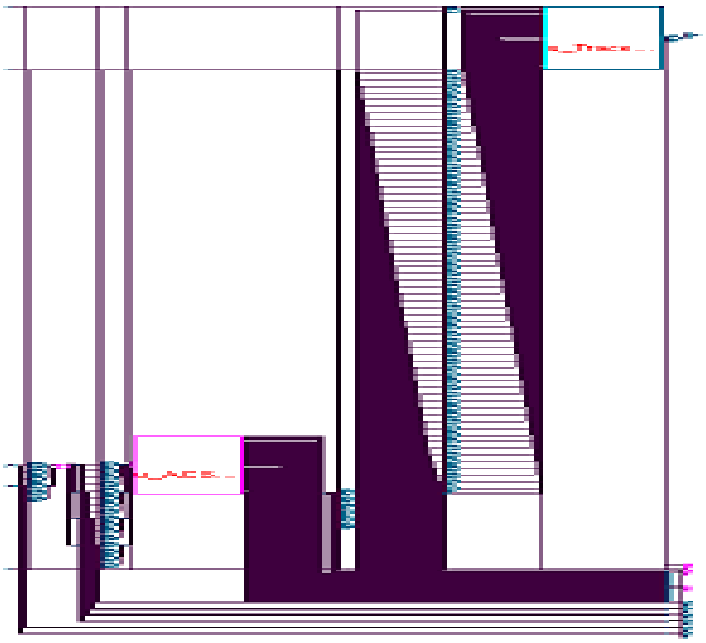


Fig. 5: RTL Schematic of Add-Compare-Select (ACS).

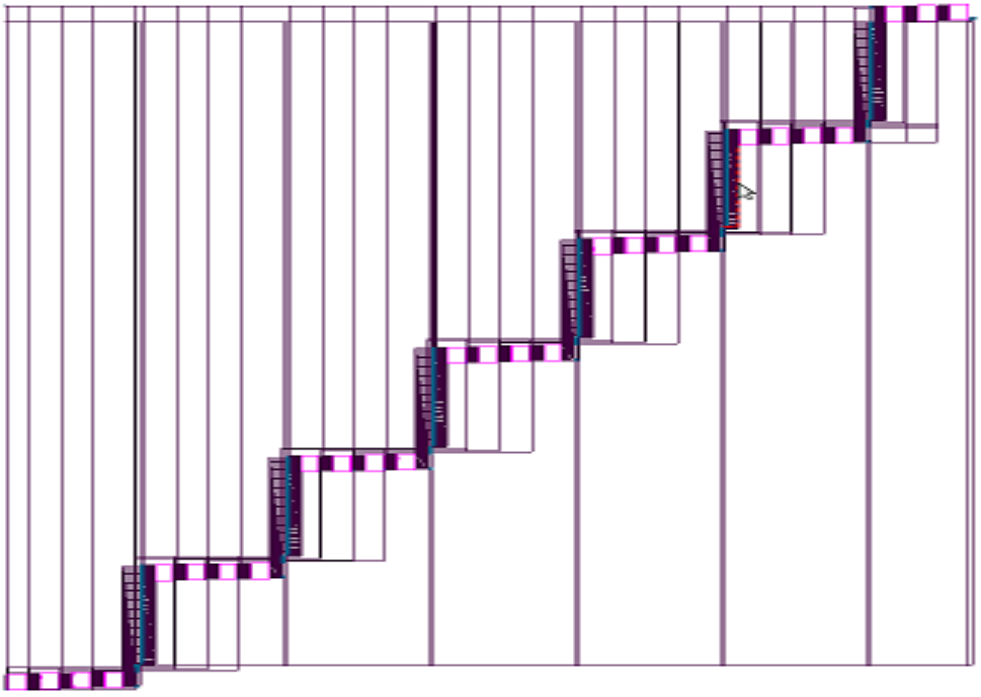


Fig. 6:RTL Schematic of State Metric Unit (SMU).

Table 1: Comparison of Various Parameters of Proposed and the Existing Technologies

Parameters/References	This work	[14]	[18]	[15]	[16]	[21]
Technology used (nm)	45	90	65	45	90	90
Power consumption (mW)	179	746	966	870	272.04	310
Throughput (Mbps)	340	1138	1013	1670	301.69	425
Max. iterations	8	5.5	5.5	5.5	8	6
Clk. Frequency (MHz)	550	486	410	600	625	370
BER	10^{-8}	-	-	-	-	-

5. Conclusion

A novel form of computation for Turbo decoder is proposed with a combination of clock gating and adjustable iteration in decoding to meet the LTE and LTE-advanced standards. The max-log-MAP algorithm is applied to the proposed architecture to achieve the power efficiency. The design is implemented in a 45nm technology using Cadence® platform. The proposed design has achieved 179.2mW with adjustable iteration (up to 8). The max-log-MAP based Turbo decoder has not only reduces the power consumption

but also meet the throughput of the core compared to the conventional method.

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