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Research paper

Harmonics reduction of a five-level inverter by unbalanced carriers and over-modulation techniques

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Abstract

The most concerns in the inverter's design are about, how to make the output voltage of the inverter sinusoidal at the desired fundamental frequency with low total harmonic distortion (THD). This paper presents a design and implementation of single-phase five-level inverter which is powered by single dc source and based on T-type multi-level inverters construction. The proposed inverter is built mainly by six IGBTs and two diodes. The used modulation technique is based on using two triangular carriers at 2000 Hz frequency and shifted by phase opposition disposition (POD) method. The carriers are made slightly unbalanced with their amplitudes. The over-modulation method is also introduced in the design to get the lowest possible THD effect without using filters. The inverter is simulated by MATLAB SIMULINK, implemented practically, and tested with the help of LabVIEW software.

Keywords: *Inverter; Multi-Level; Over-Modulation; POD; Unbalanced Carriers*

1. Introduction

The aim of utilizing the multi-level inverters is to get output voltage near in its shape to sinusoidal voltage form by making the inverter's output voltage has several levels of the input voltage which is typically obtained from separated dc sources or by single dc source with series connected capacitors. When the number of voltage levels is increased, the voltage stress on the used power electronics switches is reduced. Also, the effect of total harmonic distortion (THD) in the output side voltage is decreased even without using of filters or at least it reduces the filter's requirements and increasing the efficiency of the inverter. The early designs of multi-level inverters that include a single dc source such as diode clamped and flying capacitors or it may be based on several dc sources such as cascade multi-level inverters [1]. To reduce the THD in the multi-level inverter, several modulation techniques can be used. The Selective Harmonics Elimination (SHE) method is used to reduce of the THD of cascade or modified cascade multi-level inverters [2-3]. This method makes the switching pulses of the used IGBTs or MOSFETs at a fundamental frequency. Sometimes there is a need to power the inverter by single dc source. In this case, the input source is accompanied with couple or several dc link capacitors to get the required number of levels at the output voltage. In the work that was done by Suroso et.al [4], a new five-level inverter was made based on six MOSFETs, where the used modulation technique is based on two triangular carriers to make sinusoidal pulse width modulation (SPWM). The carriers are made by phase disposition (PD) method. Another topology is made by Biju K. and Rijil R. [5] of five-level inverter based on a full bridge inverter with a bi-directional switch but all the switches are pulsed by signals at the fundamental frequency and without showing the THD results. The same topology is used by them in [6] but with using of two carriers by PD method and also without showing the THD results. Another new design is made by Rabiya and Saju [7] which contained five MOSFETs switches, where each switch is fired at the fundamental frequency and the THD result is 31.3% which is considered as high result. There are different circuit topologies based on T-type multi-level inverters as in [8-10] where its modulation is based on PD or phase opposition disposition (POD) methods. Where for five-level inverter, only six IGBT switches are used. In all of the presented modulation techniques, all the carriers are balanced in their amplitudes. In this paper, a five-level inverter is designed based on T-Type circuit with using of six IGBT switches, but the modulation technique is made different, where some of the used switches are fired at the fundamental frequency and the other by SPWM method with carriers at relatively high frequency and unbalanced in their amplitudes and also by using POD method. The over-modulation technique [1] is also introduced in the design which is a good way to reduce the THD and increase the RMS of the output voltage of the inverter. This paper is organized as follows: An introduction, a description about the proposed inverter circuit with its modes of operations, the used modulation techniques with the resulted logic expressions, simulation and experimental results, and conclusion.

2. The proposed five-level inverter

The proposed multi-level inverter is five-level inverter. It contains of six switching devices as IGBTs (S1 - S6) with anti-parallel diodes. Four of them are making a portion of a bridge inverter, and the other two are bi-directional switches, as shown in the Fig 1. The circuit is also containing of two series capacitors which are connected in parallel to the dc source to make voltage divider for 50% of the supplied voltage for the inverter switches. The five levels of the output voltage will be as the switching status changing, with the help of voltages of capacitors and the main dc supply. The portion that forms a full bridge inverter i.e. (S1 – S4) gives the voltage at ±Vdc and zero levels. The remaining IGBT switches

S5 and S6 with their series connected diodes are responsible for making the output voltage at ± 0.5Vdc levels.

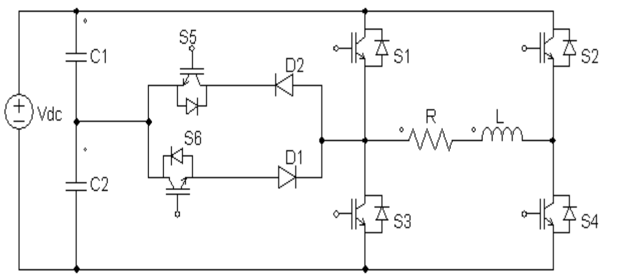

Fig. 1: The Proposed Five-Level Inverter Circuit.

3. Modes of operation of the proposed inverter

As shown in Fig 2, and according to the pointed arrows, there are six modes of operations of the proposed five-level inverter as follows: The 1st mode is when the output voltage is +Vdc, where only IGBT switches (S1 and S4) are ON, see Fig 2-a. Later the 2nd mode is when the switches (S6, D1, and S4) are ON, where the output voltage is at level of +0.5Vdc, see Fig 2-b. The 3rd mode is at Zero level which occurs when only (S3 and S4) are ON, see Fig 2-c. By the end of this mode, the positive half cycle part of the output voltage is completed. The 4th mode is when the switches (S2, D2, and S5) are ON as shown in Fig 2-d, where in this mode the output voltage is at level of -0.5Vdc. The 5th mode is when the output voltage is –Vdc where, only IGBT switches (S2 and S3) are ON, see Fig 2-e. In the last mode i.e. 6th mode, Zero level occurring when the two switches (S2 and S1) are ON as shown in Fig 2-f. By the end of this mode, the negative half cycle part of the output voltage is completed. Table 1 represents the states of each IGBT switch at different levels of the output voltage where "1" represents the Switch is ON and "0" represents the switch is OFF. By observing Table 1, it can be seen that of the working of each of the following switches (S4, S1, and S3) are the inverse of the switches (S2, S5, and S6) respectively. This means generating the pulses of any group of the mentioned switches is sufficient to get the pulses of the other group switches by taking the (Inverse) or NOT gate to them. This will be described in the next section.

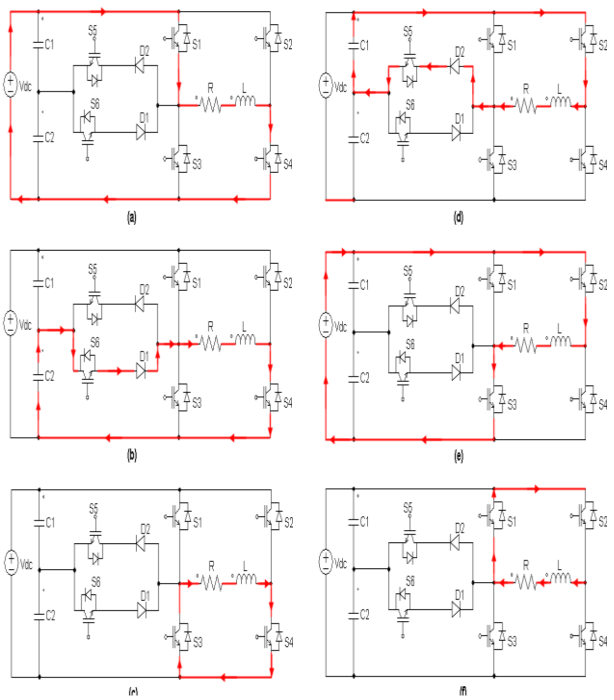

Fig. 2: Modes of Operation of the Proposed Inverter.

Table 1: The Proposed Inverter Switching States at Different Voltage Levels

Switches	Voltage Levels					
	+Vdc	+½Vdc	0Vdc	0^*Vdc	-½Vdc	-Vdc
S1	1	0	0	1	0	0
S2	0	0	0	1	1	1
S3	0	0	1	0	0	1
S4	1	1	1	0	0	0
S5	0	1	1	0	1	1
S6	1	1	0	1	1	0

4. Modulation technique and logic expressions

In this inverter, an absolute of sine wave at the fundamental frequency is generated to work as modulating (reference) signal noted by MS, with two triangular carriers at frequency of 2000 Hz are made. Most researches that use similar modulation techniques, assume that the carriers' amplitudes are balanced, i.e. have the same amplitudes [8-10]. In this research, the carriers are unbalanced in amplitude where, carrier 1 dimension according to the sequence [0.55 0 0.55] whereas carrier 2 dimension is according to the sequence [0.55 1 0.55]. The sequences are also making the two carriers are shifted to behave as Phase opposition disposition (POD). Another modification is also made, which is the using of over-modulation technique where the amplitude of the modulating signal MS is made higher than 1 by 10% to be 1.1, as shown in Fig 3. The over-modulation and the unbalanced carriers are the ways to decrease the total harmonic distortion THD as it will be shown in the following sections of this paper.

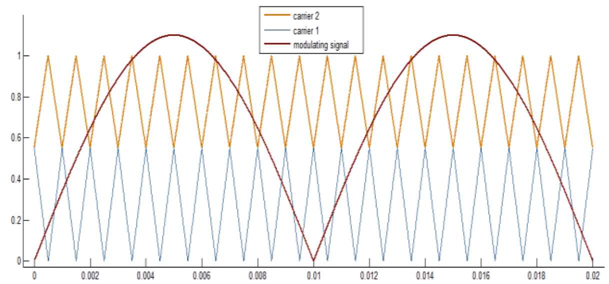

Fig. 3: The Modulating and Carriers Signals.

Each of the carriers is compared with the MS to make two signals which are responsible about the pulse width modulation PWM of the output voltage of the proposed inverter. These comparisons are Ca and Cb as shown in Fig4. Another Two square signals at the fundamental frequency and inverse to each other are also generated to make the output voltage flow at the positive and negative half cycles. These signals are S2 and S4 where, S4 is ON for the first half cycle of the fundamental frequency and S2 is ON at the second half of it. See Fig 1. Now, the signals of two IGBTs are known. The signals of the other IGBTs will be according to the signals S2 and S4 and the comparison signals Ca and Cb. The logic expressions of the all six IGBT switches as named from S1 to S6 are as follows:
MS is absolute of Sine function at fundamental frequency.

$$Ca = MS \leq \text{Carriar } 2 \quad (1)$$

$$Cb = MS \geq \text{Carriar } 1 \quad (2)$$

S4 = square wave at fundamental frequency with 50% duty cycle

$$S1 = (S4.(\overline{Ca})) + (S2.(\overline{Cb})) \quad (3)$$

$$S3 = (S2.(\overline{Ca})) + (S4.(\overline{Cb})) \quad (4)$$

$$S6 = \overline{S3} \quad (5)$$

$$S5 = \overline{S1} \quad (6)$$

$$S2 = \overline{S4} \quad (7)$$

Where the symbols ($\bar{S}$), (.), and (+), represents NOT, AND, and OR logic expressions respectively. The modulation index (Ma) can be determined by the following formula:

$$Ma = \frac{Am}{Ac_1 + Ac_2} \quad (8)$$

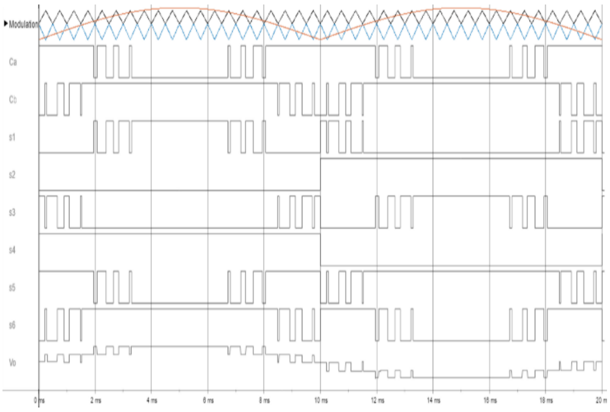

Fig. 4: Switching Pattern of the Proposed Inverter.

5. Simulation results

To test the working possibility of the inverter's circuit by using simulation tools, the proposed inverter is simulated by using MATLAB SIMULINK R2017a. All the carries, reference signals, and square wave signals are generated then; the logic circuit is made according to the comparisons that are made among all of these signals as explained in the previous section of this paper. This is to get the required pulses for the six IGBT switches. Fig 5 shows the simulated output voltage of the inverter.

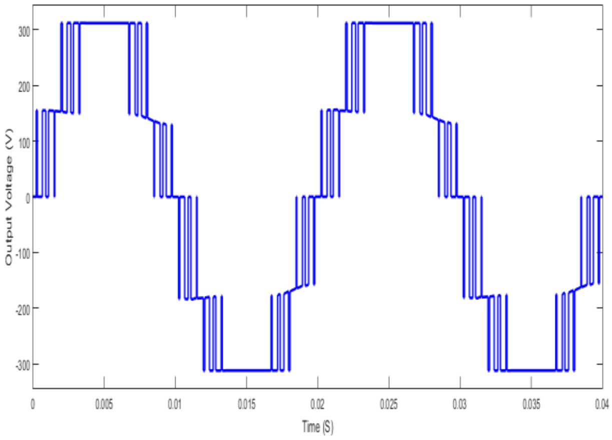

Fig. 5: The Simulated Output Voltage of the Inverter.

The THD of the output voltage of the inverter is also calculated which is 3.46% as shown in Fig 6, and the calculated THD is made without adding any filters at the output side of the inverter, where the aim in this design is to get the possible lower THD of the inverter's output voltage without filters then the filter can be added later but with a reduction in its size. For balanced carriers' amplitudes, the THD is 3.95% if the condition of over-modulation is used.

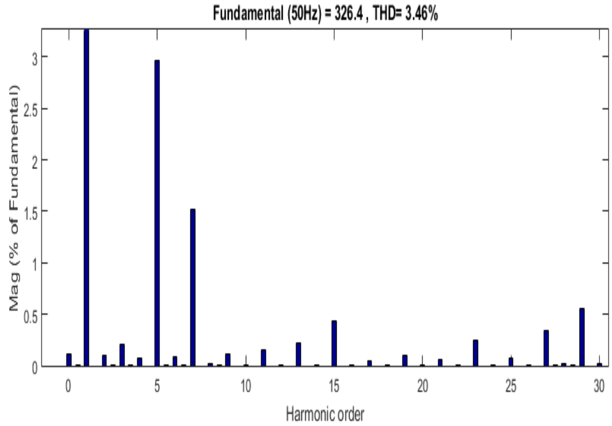

Fig. 6: Total Harmonics Distortion THD of the Proposed Inverter by MATLAB SIMULINK

6. Experimental results

The experimental results of this paper will be subdivided into two sections as follows:

6.1. Using lab view software

The LabVIEW of version 2017 is used to generate the required pulses for each IGBT switch of the inverter's circuit. The generated pulses can be gotten practically by using a data acquisition which is NI DAQ PCI-6259, to get the required pulses at their desired number and frequency with the synchronization among all of them. Fig 7 represents the six pulses that are generated by the LabVIEW before it goes to the DAQ. All of the work of the 3rd section of this paper is made by using LabVIEW, and each of the six signals pulses are made in form of a matrix. These matrices are taken as constants and then fed to the data acquisition "PCI DAQ" card. As shown in Fig 8, where the signals flow from the PC to the inverter's IGBTs is as shown in Fig 9.

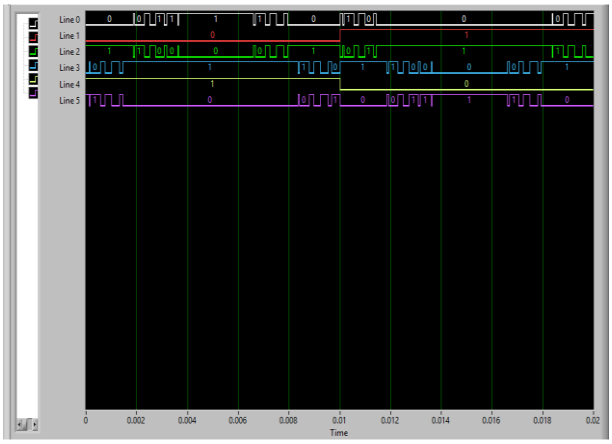

Fig. 7: The Generated Pulses by Labview (Six Pulses from 0 to 5).

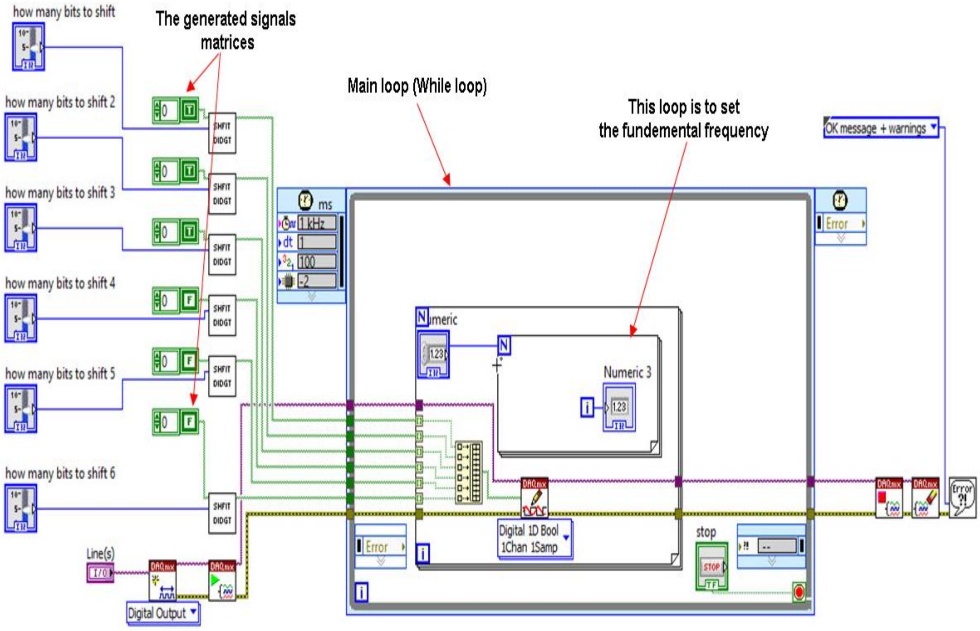

Fig. 8: The Generated Pulses to the PCI-DAQ 6259.

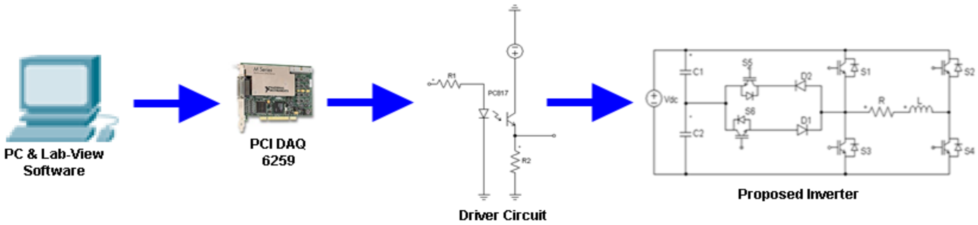

Fig. 9: Signals Flow from PC to the Inverter's Igbts.

6.2. Practical test

The proposed inverter circuit prototype is implemented practically as shown in Fig 10. The components of its circuit are as shown in Table 2.

Table 2: Proposed Inverter Components and Its Values.

Component	Value
IGBT (all)	SHG80N60UFD
Diodes (all)	RURP3060
DC link capacitors (C1,C2)	330 µF
Carriers frequency	2000 Hz
Fundamental Frequency	50 Hz

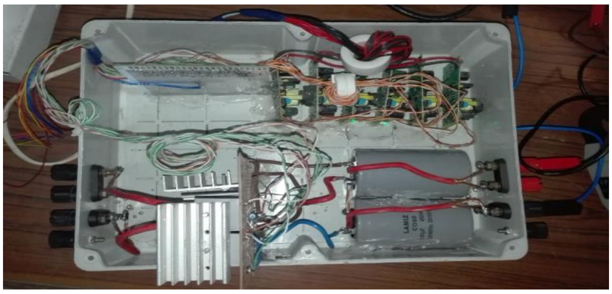

Fig. 10: The Proposed Inverter Prototype.

The inverter is tested at different input voltages where it was powered by variable dc supply. The inverter's driver circuit is built mainly by PC817 opto-couplers. All the used opto-couplers are used to isolate the PCI-DAQ and the inverter's IGBTs. To test the signals synchronization and their frequencies for all of the pulses that fed from the DAQ, All of them are tested practically by using 8-channels Saleae logic analyzer as shown in Fig11. The output voltage and THD of the inverter are measured by using DSO 2820 Virtins multi instrument PC oscilloscope, which is powered by USB as shown in Fig 12. The shape of output voltage in the experimental measurements is slightly different than the voltage of Fig4.

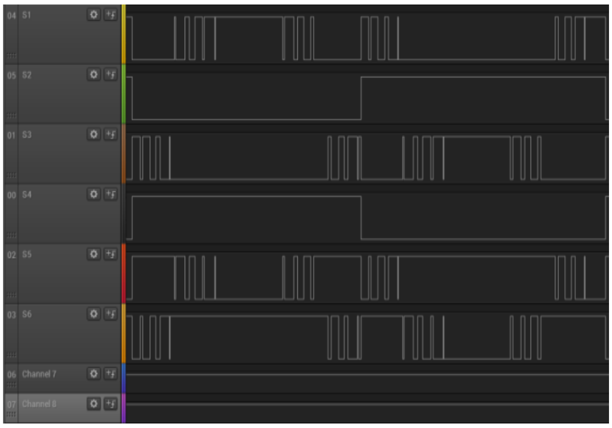

Fig. 11: Signals Synchronizing Test by Saleae Logic Analyzer Via Software (Saleae 1.1.3 Beta).

Fig. 12: The Experimental Test.

This is because of the capacitors charging and discharging, and switching losses, where each IGBT is fired at different frequencies of pulses. This results in different rise and fall times of each IGBT pulse. For the same reasons the measured THD is becoming higher than the THD of Fig6, which is approximately 6.51% and without using any filters at the inverter output stage. The measured output voltage and its FFT analysis are as shown in Figs 13 and 14 respectively.

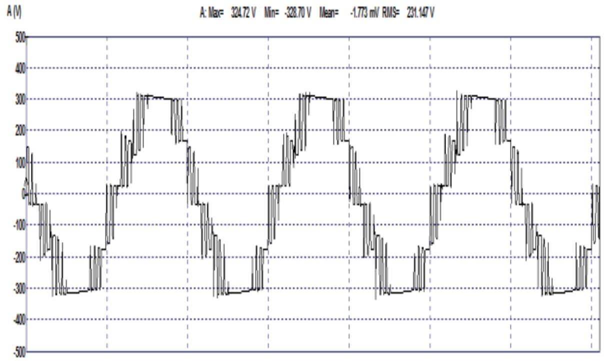

Fig. 13: Output Voltage of the Proposed Five-Level Inverter (Tested Practically).

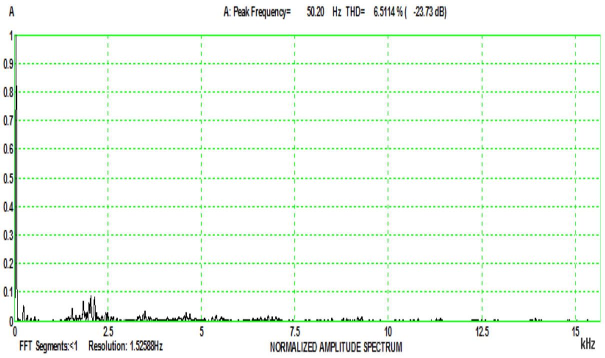

Fig. 14: FFT Analysis of the Proposed Inverter Output Voltage (Tested Practically).

Some other points that should be taken into account when designing the inverters that have the same circuit topology or similar. These points are about the pulses of some switches pairs that should not be fired simultaneously or a short circuit may be made. The pairs like (S1,S3), and (S2,S4), their pulses should have some dead time while changing the switching status between them or a short circuit may be made on the power supply. Also, for the pairs (S5, S1), and (S3, S6), there should be also dead time between their pulses to prevent short circuit occurrence at capacitors C1 or C2 respectively.

7. Conclusions

In this paper, the proposed five-level inverter is designed and implemented successfully. The used methods of making the carriers as unbalanced by POD and with over-modulation technique are good solutions to improve the performance of the inverter with low THD value and without using of filters. This inverter is recommended to be used for off grid applications with the renewable energy sources that connected to it directly such as solar cells and/or being powered by batteries, or via some of dc/dc step-up voltage converters at the dc link side.

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