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Research paper



Analysis of a Multiple Supply Voltage Floorplan Considering Voltage Drop and Electron Migration Risk

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Abstract

In Contemporary Integrated Circuits (IC), the Voltage drop in the power rails and Electron migration risk (EM) due to high current densities are the most important factors degrading the reliability of the chip. The effect of these factors leads to an imbalance in the flow of charge carriers and voids in interconnects. This paper resolves the above issues, through analyzing and predetermining it in a Multiple Supply Voltage (MSV) design during the floorplanning stage. Simulations were carried out in Cadence digital Encounter system with 180nm technology for the circuit net list of 8 point FFT (Fast Fourier Transform) and FIR filter. Results show that floorplanning scheme is powerful in reducing 100% of voltage drop and 50% of EM risk in the chip as compared to previous works.

Keywords: *Electron migration, Floorplanning, Low power Integrated Circuits (ICs), Multiple Supply Voltage (MSV), Voltage drop*.

1. Introduction

Modern Integrated Circuits (IC) developed for wearable technologies consists of many intellectual property modules inside the chip. Due to the frequent switching action of the transistors inside the chip, the module consumes dynamic power which in turn deliberately increases the overall power of the chip. To overcome these issues, an IC operates with multiple supply voltage (MSV). In this, the designers have a choice of assigning high supply voltage to the critical cells and low supply voltage to noncritical cells. Consequently, it reduces the power and delay in circuits [1].

As the chip has more number of modules, it is essential to have a power planning aware floorplan representation for the placement of modules below their respective power rails. A region consisting of arrangement of all modules under their operating power rails is named as Power domain. Every power rail consists of a voltage regulator circuit. For the ideal case, regulator circuit gives a maximum power transfer to the load underneath. However, in a practical case, due to the electrical properties of the voltage regulator circuit transfer is 90% of the power to the module. Hence it is expected to have a 10\% voltage drop in a module from their respective power rails. This creates the balance in flow of current in the Power domains. However, voltage drop above 10% leads to imbalance in the flow of current in the power domains which may lead to malfunctioning of modules [2].

Even though high current density is advantageous, it leads to widening, short and open in interconnects of the chip. This can be overcome through selection of optimal width of rail [3]. Electron migration occurring due to these current densities builds voids in the IC which diminishes the life expectancy of the chip.

Hence, concurrent floorplanning and power planning are required to increase the lifetime of IC. The Blacks' formula is used to evaluate the Mean time to failure (MTTF) of the IC. It is given by

$$\mathrm{MTTF} = \frac{\mathrm{A}}{\mathrm{J}} \exp^{\frac{\mathrm{Q}}{\mathrm{KT}}} \quad (1)$$

Where, A refers to the area of the chip in μm^2 , J is the current density $mA / \mu m^2$, Q is the amount of charge, K is the Boltzmann constant and T is the temperature in degree Celsius of the IC. The equation (1) shows that an increase in current density reduces the MTTF. In [4], Jens Lienig and Göran proposed methods based on verification of current density in interconnect during the physical design process of an IC. The power routing with reduced wire length accelerates the currents in interconnects incorporated in [5]. Placement of standard cell also plays a significant role in dealing with the electron migration problem due to Through Silicon Vias (TSVs) [6]. In the interest of floorplanning, an initial step to govern the wire length, there is an urge for Electron migration-aware floor plans [7].

Hence, this paper analyzes the Skewed Binary tree (SKB) floorplanning representation, which is based on the Binary tree [8]. From the motivation of its analytical framework, this paper examines the performance of floor planner on Voltage drop and Electron Migration risk

2. Multiple Supply Voltage Floor Planning

Representation of the floorplan helps the IC designers for the placement of modules in the core area of the chip. Eventhough B*tree [9] and sequence pair [10] representation performs better in MSV floorplanning, SKB tree take less time to floorplan with wire length and power as its constraints.

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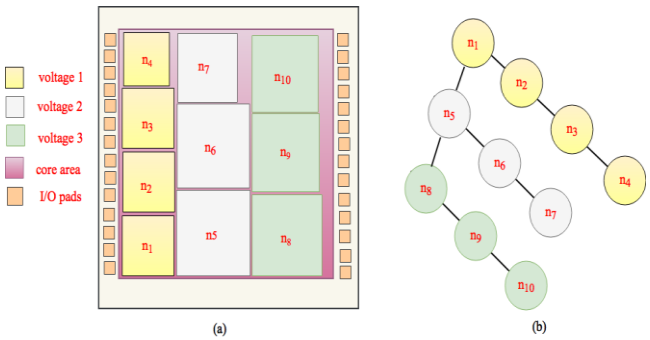


Fig 1: Example of typical floorplan. a) Floorplan after application of SKB tree b) SKB tree structure of Floorplan

Every parent node in the SKB tree is has ordered nodes, arranged one after another without left child. Modules are occupied in each node present in right child of parent node. Parent node in the tree structure which is also a module which is placed in the left-corner of the voltage island. Every parent node of the level is connected to root node due to its interconnect. Thus, every levels of the tree represents power domain. Thus, each level will have modules at different operating voltages.

Figure 1(b) illustrates a typical SKB tree representation and fig 1(a) shows floorplan of a circuit consisting of 10 modules. Modules $\{n_1, n_2, n_3, n_4\}$ operates in voltage level 1 and $\{n_5, n_6, n_7\}$ in voltage level 2. Similarly, $\{n_8, n_9, n_{10}\}$ modules works in voltage level 3. n1 is considered as parent node in the level 0 since it is need to be placed in the left corner of the floorplan. Similar way, modules n_5 and n_8 represents parent node for the levels 1 and 2, and placed in the left corner of their power domain.

In this way, SKB tree helps the designer for the placement of modules in the chip's core area. In the event of tree traversal, the time complexity is reduced for placement of modules in the core area of the chip.

2.1. Placement Process

For the given N number of modules, let n_i be the number of modules present in the n^{th} power domain. Let (w_i, h_i) be the width and height of the module n_i. Using Depth first search algorithm, the modules are chosen from the tree structure and placed into a power domain of width W_i. The width of the power domain is calculated as

$$W_i = \frac{a_i}{a_t} w_c (1+\gamma) \quad (2)$$

In the above equation (2), a_i refers to the total area of modules in the power domain, a_t refers to total area of the chip, W_c refers to the width of the chip and γ refers to the allowable gap.

The module $n_{(i+1)}$ is placed subsequently to n_i if it fits inside the width $(W_i - n_i)$. If $w_{(i+1)} > w_{ij}$ the module $n_{(i+1)}$ is put in a virtual stack. Since it fails to fit inside bounded width Wi the module n_i placed above $n_{((i+1))}$. Before the placement of the module $n_{(i+2)}$ priority is given to the modules in the virtual stack. This makes a compact floorplan.

The representation has cluster constraint which serves as an upper bound for a minimum quantity of modules a Power domain can group.

2.2. Perturbations

Exchange of modules between the voltages levels is performed to shrink the empty area in the chip. Thus it is efficient in reducing the silicon cost during fabrication. Figure (2) shows the arrangement of 48 modules using SKB tree. The floorplan in figure (2), also has a vacant region but it is for the placement of standard cells.

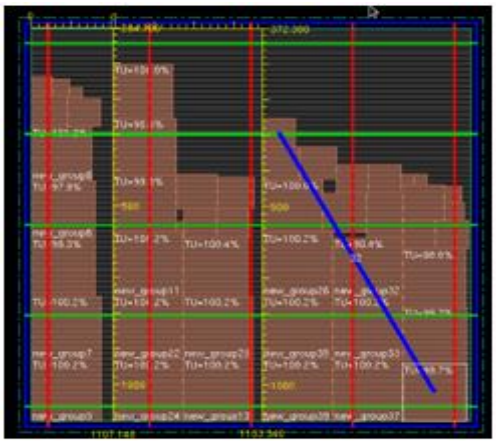


Fig 2: Floorplan of 48 modules using SKB tree

3. Results and Discussions

The analysis of representation is performed in Cadence digital Encounter System for the netlist in the Verilog Hardware Description Language (HDL) synthesized in 180 nm technologies.

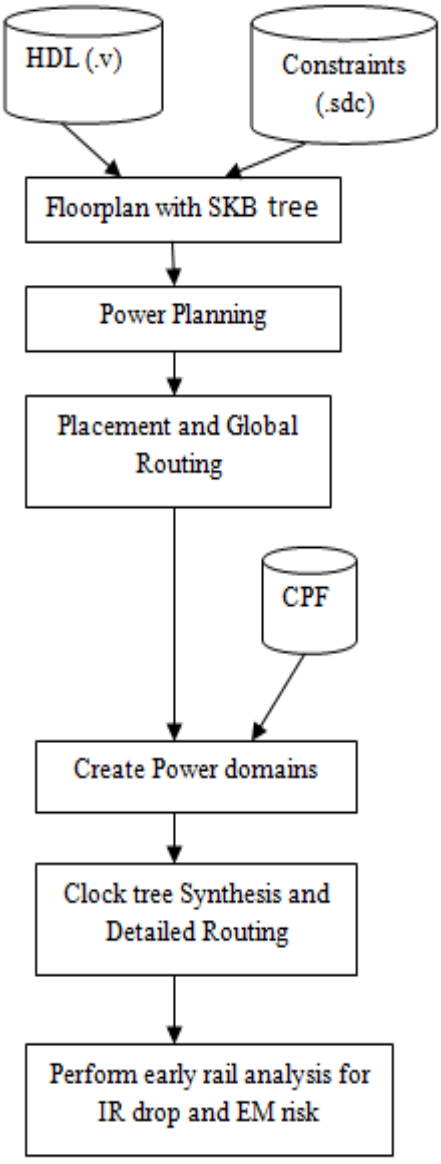


Fig 3: Design flow for analysis

Figure 3 shows the design flow for the analysis. For circuit 8 point FFT and FIR filter netlist in Verilog with its operating constraints in .sdc file format, SKB tree floorplanning is implemented. Table 1 illustrates the number of modules present in the circuit netlist. The physical design process incorporates the design environment as mentioned in Table 2. After identifying the suitable locations of the modules in the chip; Power planning realizes the power rails and strips horizontally and vertically in the chip area. Subsequently, insertion of standard cells takes places in the vacant regions of the chip through the placement process. Next, global routing connects all the pins of the modules in metal six layer. A Common power format (CPF) file consisting of affirmations on modules operating at different voltages is committed after global routing. This is due to the compact placement of modules. Then, clock buffers are inserted, and detailed routing is executed which connects all the layers and tracks between the modules. A congestion analysis is performed to determine the routing complexity. The results tabulated in Table 3 show that algorithm induces 4.34% congestion. Rail analysis arrives at the creation of power pad file for all the supply rails. As a result, voltage drop and electron migration of the modules are found.

Table 1: Number of modules in the net list

Name of the Circuit	Modules
8 point FFT	25
FIR	49

Table 2: Design Environment Specification

Name of the Circuit	Floorplan Specification	
FIR filter and 8 point FFT	Core ultization	0.9
	Power	Planning
	Number of strips	4
	Layers	6
	Voltages	1.62V, 1.98, 1.8V

Table 3: Congestion Analysis

Name of the Circuit	Congestion %
8 point FFT	7.015
FIR	5.12

3.1. Voltage Drop Reduction

Voltage drop in the modules is found using early rail analysis. It is assumed to have 10% of the allowable drop in the modules from its respective power rails. Table 4 illustrates the results after early rail analysis. Here, #blks refers to the number of hard modules present in the netlist; islds indicates the number of voltage islands in the design. #IR viol shows number modules violating the threshold limit of its voltage. The result indicates that SKB based floorplanning reduce the IR drop to 100%. There is an increase in the power distribution network (PDN) as the SKB tree fits 50% of modules in their respective islands. Thus it gives directions for the need of an algorithm which aims to fit 100% of modules in below their voltage rails. Also, figure 4 shows the distribution of current in the power domains. It is implicit that there is exist a uniform flow of current in the all the power domains which gives maximum transfer of the power from the rails to all the modules.
Since the number of modules are similar as in [5] for circuits with 49 modules and 25 modules results were compared with [5].From the table 5, the SKB tree algorithm consumes 7.5% increase in area and 25% increase in wire length(WL). Analogously, it is due to increase in the power PDN routing resource.

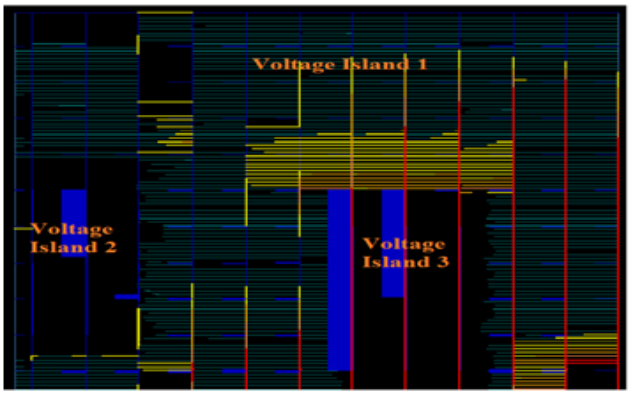


Fig 4: Current distribution in the voltage islands in the circuit FIR filter

3.2. Modulating the width of Power Rails

Effect of variation in the width of power rails is monitored in for the two circuits. The results from Table 4 shows for the circuit containing 25 modules increase in width shrinks the lifespan of the
chip due to increase in the probability of failure of modules per year. This is due to high wire length. However, for the circuit with 49 modules, failure probability reduces due to a reduction in wire length. Thus the floor planner controls the probability of failure by a shortening in wire length.

3.3. Control of Electron Migration Risk

Electron migration risk analysis is performed to evaluate the failure of modules per year for the floorplan mode and placement mode. Results show that floorplanning the hard modules in the chip have an impact towards an increase in the lifespan of the chip through decreasing the probability of failure of modules. Table 6 reveals that compared to placement mode [12], floorplanning mode increases the life span of the modules to 52%. Thus SKB tree representation is also centric to electron migration risk.No more than 3 levels of headings should be used. Other headings must be in 9pt font. Only the first word in a heading must be capitalized and other word should be in small case.

4. Conclusion

This analysis of the multiple supply voltage floorplan to explores its ability in the placement of modules in consideration with the voltage drop and electron migration risk. Furthermore, since the change in the width of power rail have more coverage modules in the chip; the analysis also includes the effect of a change in the dimensions of the supply sources. The results conclude that the floor planner is voltage drop aware as it exhibits 0% IR drop in the modules operating with respective voltage levels. Also, results show that since the floorplan reduces the overall wire length of the chip, it also centric with the reliability of the chip with minimal likelihood of failure of the modules. The results also show that due to the top-to-bottom hierarchy in the physical design process of Integrated Circuit(IC) flow where the placement follows the floorplanning it is implicit that lifespan of the chip can be extended through a good floorplan representations.
Finally, some suggested future enhancement includes optimization in representation for voltage island floorplanning with minimal utilization of the power distribution network (PDN) routing resource. The inclusion of this constraint is creating an impact with 100% placement of modules in their respective voltage levels owing to reduction in the congestion and wire length which in turn increases the lifespan of the chip

Table 4: Voltage Drop and Electron Migration Risk Analysis

#blks	#islds	Width	Threshold	Area ratio	#Wire Length (µm)	#IR viol	Probability of failure per year
49	3	4	10%	0.80	231857	0/49	0.818
		5		0.9	6564	0/49	0.2547
25	3	4	10%	0.91	286910	0/49	0.00185
		5		0.91	900312	0/49	0.6173

Table 5: Comparison with Existing Works

#blks	#islds	Threshold	[1]		SKB		Increase%	
			Area ratio	Wire length(µm)	Area ratio	Wire length(µm)	Area ratio	Wire length(µm)
49	3	10%	0.835	1337163	0.809	2318579	9	42.32
25	3	10%	0.845	85911	0.9	6564	6	8.7

Table 6: Electron Migration Risk Comparison with Placement and floorplanning

#blks	Probability of failure of modules/year	
	Placement[12]	**SKB Floor planning**
49	1.00	0.53
25	0.85	0.3

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