International Journal of Engineering & Technology, 7 (2.24) (2018) 304-306

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

A New Empirical Evaluation of Existing Methods for Estimating BDD Sizes

Madasamy Raja[1*], K. Vidhya Lakshmi[2], Mohamed Raseen

[1,3]Department of Computer Science and Engineering
[2]Department of Information Technology
[1,2,3]Vel Tech Multitech Dr. Rangarajan Dr. Sakunthala Engineering College, Chennai – India 600 062
**Corressponding Author E-mail: madasamyraja@veltechmultitech.org*

Abstract

Binary Decision Diagrams (BDDs) are very useful structures to represent Boolean function in VLSI synthesis. Time taken to build a BDD and obtaining its size plays a major role in the time of complexity of VLSI synthesis. This time complexity increases drastically as the number of input variables increases. Various models to estimate the size of the BDD, without actually building it already exists. These models claim to support both simplified and un-simplified Boolean functions. The models were developed under the justification that time to estimate will be far less compared to the time taken to actually build the BDD. There are two drawbacks with the existing model. First drawback is that, the current model just follows a random curve fit without any substantial mathematical support. Second drawback is the existing model is based on experimental results which used only less than ten variables. Since current practical functions may use hundreds of variables, there is no guarantee that the model is accurate enough. Given the two drawbacks, it becomes necessary to test the existing model for more complex circuits with hundreds of variables. In this paper the existing models were tested with standard benchmark circuits. Results were compared with actual BDD sizes of the benchmarks and the estimated sizes from the parameters of the benchmarks. Comparison of the results proved that existing models give poor results for the circuits with more than ten variables and existing models become inapplicable to most of the current practical functions that uses more than hundreds of variables.

Keywords: *Binary Decision Diagrams, Modeling, Invalidation.*

1. Introduction

Binary Decision Diagram (BDD) is acyclic graph (similar to binary tree) representation of a Boolean function. This was first proposed by Akers[1] and later developed by Bryant [2]. The technique was very successful and hence attracted many researchers in the area of synthesis and verification of Logic Circuits. The BDDs are also used in VLSI and CAD systems [3], [4]. As the number of inputs for Boolean functions increases, the time taken to build the BDD increases correspondingly. Thoughthere are powerful processers and faster RAM nowadays, the size of the Boolean functions and the time to build them also increases proportionately.

In order to reduce the time taken to build the BDD, various models were proposed to estimate their sizes. The models were initially developed for un-simplified Boolean functions [5], [6], [7] and then for simplified functions [8]. More detailed analysis about the validation of the model with un-simplified functions was done in and proved that the estimated model from [5], [6], [7] might be incorrect[9]. Thus it became a necessity to validate the existing models for more practical functions using benchmarks. In this paper standard benchmarks were taken and were used to prove that the existing models to estimate the BDD sizesare incorrect.

Section 2 explains the methodology used by the existing models to estimate the BDD sizes. Section 3 explains the disadvantages of the existing BDD estimation models. Section 4 explains, the methodology used in this research work and the experimental results used to invalidate the present models. The final section concludes the paper.

2. Existing Models to Estimate the BDD Sizes

Initial research to estimate the size of the BDD was done with un-simplified functions [5]. In [5], initially the number of variables was fixed, then random un-simplified functions were generated for the number of variables and then BDDs were built for them. Graph was then plotted between the number of product terms in SOPs in the Boolean function and the corresponding BDD size. Fig. 1 shows the relation between the number of product terms in the SOP and the number of nodes for 9 variables using symmetric sift reordering method. In [5] the graph for the number of variables (Fig.1) was modeled using the eq. 1, shown below.

$$NN = \alpha \times NPT^{\beta} \exp(-NPT \times \gamma) + 1 \quad (1)$$

In eq.1 the parameters α, β, γ is dependent on the number of variables. Hence the number of nodes is dependent on the number of variables. Fig. 2 indicates the graph for the experimental and the modeled values. In the literature [5] it is mentioned that the model in Eq. 1 is very suitable since both the graphs are matching. The work was extended for other reordering models and the eq. 1 was generalized to eq. 2 below (where μ depends on the variable ordering).

$$NN = \mu\alpha NPT^{\beta}e^{(-NPT\gamma)} + 1 \quad (2)$$

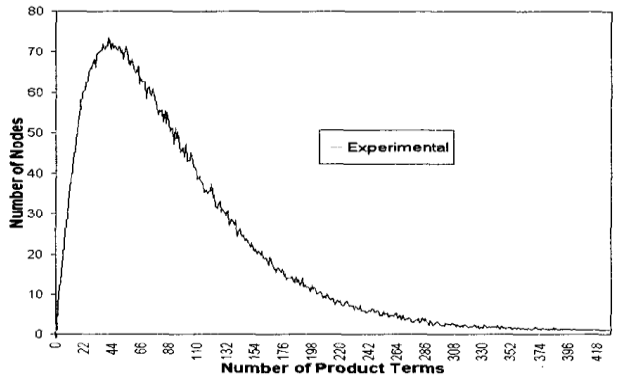

Fig. 1: Number of Nodes for 9 Variables

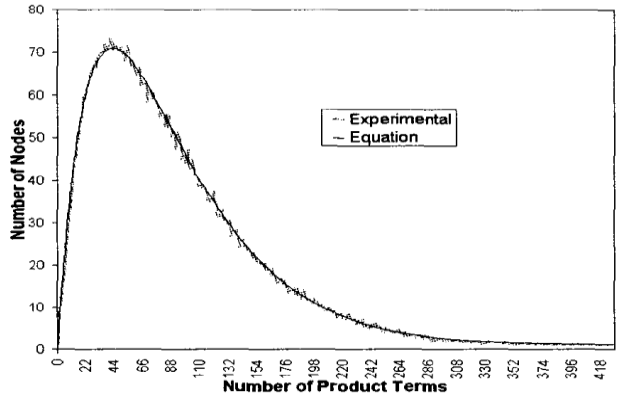

Fig. 2: Number of Nodes for 9 Variables, Equation and Experimental

The work was further extended in [6], [7] to find the maximum and minimum of the number of nodes, as in the following eq. 3.The eq. 3 was based on eq. 2 with the assumption that eq. 2 is valid.

$$NN_{\max} = (\mu\alpha)\left(\frac{\beta}{\gamma e}\right)^{\beta} + 1 \quad (3)$$

Similar work was done for simplified Boolean functions in [8]. The graph for simplified Boolean functions is shown in fig. 3.Fig. 3 shows the number of nodes for both for experimental and equation.

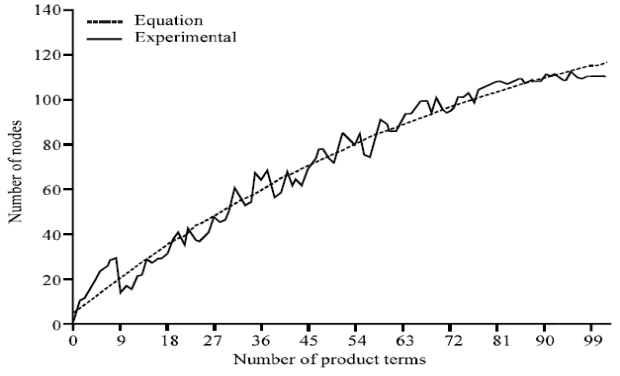

Fig. 3: Number of Nodes for simplified Boolean function

Similar to [6], model for fig.3 was developed and is shown in eq. 4. In eq. 4 COP is the limit of the maximum number of product terms (Simplified) that can exist for a given number of variables.

$$\begin{aligned} COP &= 0.6378*e^{(0.5591*NV)} \\ NN &= 0 \text{ for } NPT <= 0 \\ &= 0 \text{ for } NPT > COP \\ &= 323.5*e^{(-0.002399*NPT)} - 319*e^{(-0.008221*NPT)} \end{aligned} \quad (4)$$

3. Disadvantages of the Existing BDD Size Estimation Model

First drawback is in [5], [6], [7]existing model is derived without any mathematical or theoretical proof.

Second drawback is a same BDD size can be represented in more than one curve. So we cannot give the guarantee that a BDD and Curve has a one-to-one relationship. This point is proved in the Fig. 4. In Fig. 4, a poison distribution with λ=4, will yield the same curve. Thus the same experimental BDD size can be fitted by more than onecurve. But when the λ changes the size of the curve is also changes.

Third drawback is the existing model is based on experimental results which used only less than ten variables. Since current practical

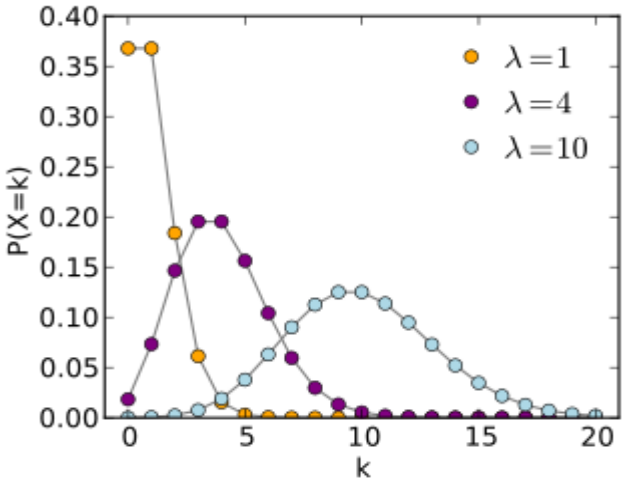

Fig. 4: Poisson Distribution

functions use hundreds of variables and there is no guarantee that the model is accurate enough.

Moreover in [9], the model estimation was approached in a more detailed manner and was realized that adding multiple parameters varies the graphs of the BDD sizes. Given the above drawbacks, it becomes necessary to test the existing model for more complex circuits with hundreds of variables.

4. Invalidation of the Existing Model

In this paper the existing model is tested by using benchmark circuits. BDDs were built for the benchmark circuits and their sizes were compared with the one estimated by existing model. Table 1, shows the results of the experiment.

The comparison indicates a huge difference in BDD sizes for most of the Benchmark circuits. For example in line 18 for benchmark cc, the actual size is 125 and the predicted size is 83.32 and 6.59 which is difference in hundreds. In line 17 for Benchmark C880, the actual size is 14837 where as the estimated size is 1.42e11 and 2.69e34, which is a difference in more than trillions. The rational for the difference is that the existing model assumes the BDD size is an exponential rise.

Table 1: BDD Sizes for Benchmark circuits (Actual and Estimated)

No	Bench-mark	BDD Size		
		Actual	Existing Methods' estimation	
			Un-Simplified	Simplified
1	5xp1	94	88.84	29.45
2	9sym	25	45.46	501.7
3	9symml	25	19	0
4	alu2	324	267.22	6034.49
5	alu4	1047	4.50 e 3	3.26 e 6
6	apex1	2589	3.89 e 8	7.59 e 29
7	apex4	1447	668.94	4515.31
8	apex5	1850	4.35 e 5	1.79 e 17
9	apex6	1197	4.30 e 4	1.76 e 15
10	apex7	614	1.07 e 5	1.76 e 15
11	b1	12	6.16	1.06
12	b9	256	1.09 e 3	3.13 e 6
13	b12	93	167.87	666.32
14	C8	137	4.63 e 2	4.05 e 5
15	C17	12	8.5	1.67
16	C432	5416	1.56 e 9	7.56 e 26
17	C880	14837	1.42 e 11	2.69 e 34
18	cc	125	83.32	6.59
19	cht	247	139.48	23.46
20	clip	147	300.14	2.50 e 3
21	cm42a	50	44.26	8.38
22	cm82a	19	15.9	0.13
23	cm85a	59	188.87	6.46 e 3
24	cm138a	56	77.6	-2.22
25	cm150a	33	4197.41	3.25 e 12
26	cm151a	34	172.88	1.54 e 5
27	cm152a	16	59.58	1.63 e 4
28	x1	775	6.6 e 4	1.45 e 16
29	x2	57	90.97	5960.82
30	x4	809	5122.25	1.72 e 7

Hence for even 50 variables, exponential curve lead to a value in trillions.As the number of variables increases further, the estimate size from the model will increase rapidly and further deviate from the actual size. Hence in this paper it is proved that existing model is not suitable for complex functions with more than 10 variables and the model will definitely fail for modern circuits with hundreds of inputs.And, if the estimating models areincorrect the equations 1, 2, 3 and 4 should become invalid too.

5. Conclusion

In this paper the necessity to prove the correctness of BDD size estimation is considered. Most of the practical functions are huge and may not be applicable for the BDD size estimating models, which were derived with less than 10 variables. In order to clarify the correctness of the model, BDD sizes were built for benchmark circuits and the sizes were compared for actual and estimated sizes. Results indicated that the current estimating models fails miserably for more than 10 variables and is unsuitable for most of the modern and latest circuits.

References

[1] S. B. Akers, "Binary Decision Diagram," IEEE Trans. Computers, Vol. 27,pp. 509-516, 1978.

[2] R. E. Bryant, "Graph–Based Algorithm for Boolean Function Manipulation," IEEE Trans. Computers, Vol. 35**,** pp.677-691, 1986.

[3] S. Minato, "Binary Decision diagrams and Applications for VLSICAD," Kluwer Academic Publishers, 1996.

[4] K. Priyank, "VLSI Logic Test, Validation and Verification, Properties & Applications of Binary Decision Diagrams," Lecture Notes, Department of Electrical and Computer Engineering University of Utah, Salt Lake City, UT84112.

[5] M. Raseen, P.W.C. Prasad, and A. Assi, "Mathematical Model to Predict the Number of Nodes in an ROBDD," The 47th IEEE International Midwest Symposium on Circuit and Systems (MWSCAS' 2004), Vol. 3, pp. 431-434, Hiroshima, Japan, July 2004.

[6] M. Raseen, Ali Assi, P.W.C. Prasad and A. Harb, "An Efficient Mathematical Estimation of the BDDs Complexity", The 16th IASTED International Conference on Modelling and Simulation, pp 381-386, Mexico, May 2005.

[7] M. Raseen, P.W.C. Prasad and A. Assi, "An Efficient Estimation of the ROBDD's Complexity", Integration - The VLSI journal, Vol. 39, Issue 3, pp.211-228, Elsevier Publications, 2006.

[8] M. Raseen and K. Thanushkodi, "ROBDD's Parameter Estimation for Simplified Boolean Functions", International Journal of Soft Computing, Vol. 3, Issue 6, pp.451-460, Medwell Journals, Nov-Dec 2008.

[9] M. Raseen and E. Venitha, "Exact Modeling of Binary Decision Diagram Complexity", International Conference on Internet of Things and Challenges, pp. 244-248, Chennai, India, December 2017.

[10] T.Padmapriya, S.V.Manikanthan, "An enhanced distributed evolved node-b architecture in 5G tele-communications network", International Journal of Engineering & Technology, DOI: 10.14419/ijet.v7i2.8.10419, ISSN NO:2227-524X, Vol-7, No.2.9(2018)

[11] S.V.Manikanthan and V.Rama "Optimal Performance Of Key Predistribution Protocol In Wireless Sensor Networks" International Innovative Research Journal of Engineering and Technology, ISSN NO: 2456-1983,Vol-2,Issue –Special –March 2017.

[12] T. Padmapriya, V.Saminadan, "Performance Improvement in long term Evolution-advanced network using multiple input multiple output technique", Journal of Advanced Research in Dynamical and Control Systems, Vol. 9, Sp-6, pp: 990-1010, 2017.