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Research Paper

Design of delay efficient Booth multiplier using pipelining

Abhishek Choubey, SPV Subbarao, Shruti B. Choubey

Department of Electronics and Communication Engineering, Sreenidhi Institute of Science and Technology, Hyderabad, Telangana, 501301
**Corresponding author E-mail: abhishek@sreenidhi.edu.in*

Abstract

Multiplication is one of the most an essential arithmetic operation used in numerous applications in digital signal processing and communications. These applications need transformations, convolutions and dot products that involve an enormous amount of multiplications of an operand with a constant. Typical examples include wavelet, digital filters, such as FIR or IIR. However, multiplier structures have relatively large area-delay product, long latency and significantly high power consumption compared to other the arithmetic structure. Therefore, low power multiplier design has been always a significant part of DSP structure for VLSI design. The Booth multiplier is promising as the most efficient amongst the others multiplier as it reduces the complexity of considerably than others. In this paper, we have proposed Booth-multiplier using seamless pipelining. Theoretical comparison results show that the proposed Booth multiplier requires less critical path delay compared to traditional Booth multiplier. ASIC simulation results show proposed radix-16 Booth multiplier 13% less critical path delay for word width *n*=16 and 17% less critical path delay compared for bit width *n*=32 to best existing radix-16 Booth multiplier.

Keywords: *Booth multiplier, Pipelining, Very-large-scale integration (VLSI).*

1. Introduction

Multiplication is important operation in various applications; for example in image processing, digital signal processing and wavelet. In certain DSP applications, like digital filter and wavelets uses large number of multipliers, it is necessary that multipliers optimized as much as possible for increasing the performance of all those applications. Multiplication of an operand with a constant can be implemented with numerous methods such as multiple constant multiplications [1, 5], graph-based multiplication [3] and shift-and-add algorithm. However, this method results in large area and delay. Since the constant is known beforehand, the appropriate approach can be optimized in order to significantly improve design parameters, such as area, delay and area-delay product, resulting in more efficient multiplication.

Booth multiplication is used to increase the speed of the multiplier by encoding the numbers that are multiplied. Booth Encoding multiplication is able to reduce the number of partial products row by *N/r*, where r number of bits encoding. The radix-r Booth multiplier offers the best area and power performance among then multiplier [2,7,8]. In this paper we have proposed Booth multiplier as constant multiplier with less critical delay. The advantage of proposed multiplier is that lowest delay as compared to existing multiplier design.

The remainder of this paper is organized as follows. The proposed constant radix-8 Booth multiplier is given in Section 2. Hardware-time complexities and performance comparison is presented in Section 3. Conclusion is presented in Section 4.

2. The Proposed Booth Multiplier

The general design of a multiplier is shown in Fig. 1. The input data Y is multiplied with a specific coefficient X and the output *Z* is the result.

Consider two *n*-bit signed numbers *X* and *Y* are multiplied, where *X* is multiplicand number and Y is multiplier number. Both *X* and *Y* are represented in 2's complement number system as

$$X = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i \tag{1}$$

$$Y = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i \tag{2}$$

where x_{n-1} and y_{n-1} are the sign bits.

With shift-add method multiplication of two signed binary numbers involves partial product terms, and these partial product terms are added in adder unit. On the other hand radix Booth multiplication algorithm offers multi-bit encoding and it generates fewer partial products than the shift-add method. Therefore, the adder unit of radix-r Booth multipliers involves less number of adders than those of shift-add method.

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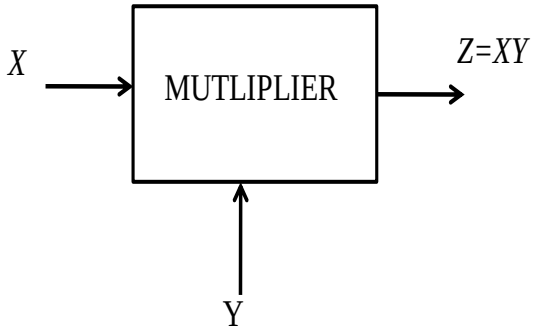

Figure 1: General block multiplier

A general block diagram of Booth multiplier is shown in Fig.2. It has four parts (i) Partial product generator (PPG) (ii) Booth selector (BS), (iii) Booth encoder (BE) and (iv) Adder unit (AU).The PPG unit generates the partial product row, BS unit select the partial row. BE unit is generates the control signal to select the partial product row and The AU compress the partial product rows to calculate the product word. We have proposed Booth multiplier with less critical path delay. In proposed Booth multiplier adder unit is comprise of pipelining to reduce the critical delay for higher bit width. The proposed Booth multiplier is best performance as compared to other exiting Booth multiplier without pipelining. shown in Fig.2 AU unit use pipelining to reduce to critical path delay.

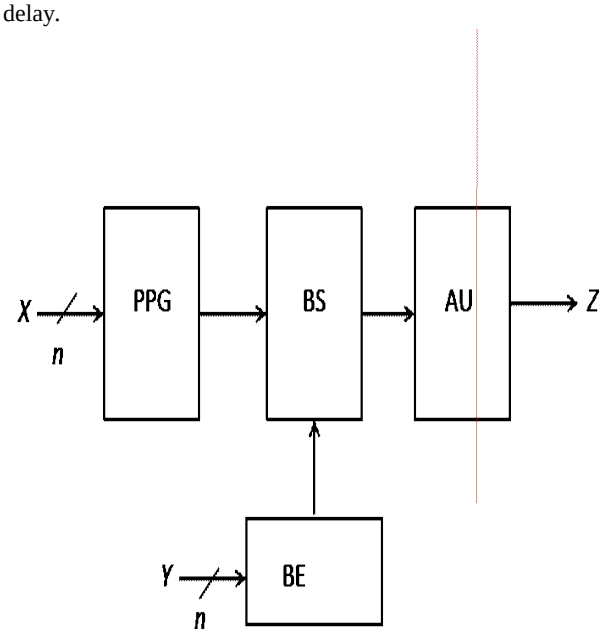

Figure 2: Block diagram of Booth multiplier using pipelining

3. Hardware-time complexities and performance comparison

The multiplier is consist of BS, BE and AU unit. Hardware complexity of BS and AU of different word length is shown and different radix sizes are given in table 1. As shown in table-1, complexity AU higher for small radix sizes but it involves large critical path delay for large bit width (*n*).

In general, complexity of BS of radix Booth multiplier structure increases for higher radix sizes while the AU complexity decreases. Therefore, higher radix sizes Booth multipliers have lower adder complexity than the smaller radix size Booth-multipliers. Keeping in this we have analyses complexity of Booth multiplier for different word length and different radix Booth multiplier.

We have also coded radix-4, radix-8 and radix-16 Booth multiplier for 16 bit and 32 bit size in Verilog and synthesized them using 45nm library. Synthesis results are given in table 1 in terms of area, delay and area-delay (ADP). Based on the synthesized result we found that radix-4 has 11% less delay for n=16 and 18 % less dealy compared to existing radix-4 Booth multiplier [9] respectively. The proposed radx-8 Booth multiplier 14% less CPD for n=16 and 17% less CPD for n=32 as compared to existing radix-8 Booth multiplier [6] respectively. The proposed radix-16 Booth multiplier 13% less CPD for *n*=16 and 17% less CPD for *n*=32 bit width compared to existing radix-16 Booth multiplier [8].

Table 1: Synthesis result of radix-4, radix-8 and radix-16 booth multiplier using cadence tool

Radix size(r)	Bit-width (n)	DAT (ns)	AREA (um^2)	ADP (u.sqm.s)
Radix-4[9]	16	1.90	7832	14880
	32	2.35	10234	24099
Proposed multiplier	16	1.68	8321	13979
	32	1.92	10978	21077
Radix-8[6]	16	2.12	8321	17640
	32	2.35	10731	25217

4. Conclusion

In this manuscript, we have proposed pipelining radix-r Booth multiplier for different word length. The proposed radix-r Booth multiplier involves less critical path delay compared to best existing Booth multiplier. Due to less critical path delay significant reduction in the area-delay product (ADP). Experimental results show significant improvements of the proposed radix-r Booth multiplier. ASIC synthesis results show that 13% and 17% less critical path delay for *n*=16 and *n*=32 respectively for radix-16 Booth multiplier. These features could be traded for low area delay product real time digital signal processing applications. The proposed Booth multiplier is suitable for the efficient VLSI architecture of digital filter and wavelet.

Acknowledgement

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