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Research Paper

10 Ghzcharge pump PLL for low jitter applications

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Abstract

This paper presents design and simulation of charge pump architectures for 10GHz Charge Pump Phase locked Loop. Differential delay cell VCO with symmetric load and Programmable frequency divider are efficiently implemented in loop. Able to achieve Peak jitter of the Divider 10ns, Peak jitter of VCO 205ps at 1GHz.Charge pump is analysed in loop by reduced current mismatch using improved high swing cascode structure including start up circuitand it has low turn ON voltage and high ouput impedance to provide stable voltage.Charge pump results current mismatch less than 0.05%.10GHz DPLL is simulated with 65nm techonology, 1.2V and tsmc foundary model files

Keywords: *Charge Pump PLL; Jitter; Differential VCO; Cascade; PFD; Current Mismatch.*

1. Introduction

Charge Pump Phase Locked Loop (CP PLL) has large area of application for its simplicity and performance. Here input and output frequencies are digital in nature, but processing isanalog and digital. In functionality Phase Frequency Detector (PFD) and divider are digital, Charge pump (CP) and Voltage controlled oscillator (VCO) are analog. The stability of loop is accomplished with passive filter components in loop. Each block has major challenges to design and execute in loop to achieve loop parameters. Charge pump current and its non-idealities dominates in loop performances. Charge pump generates proportional voltage to phase difference caused by input frequency and feedback frequency. Glitch free charge pump output voltage determines capability of any CP PLL to measure its jitter. Depends on loop requirement, there are different types of charge pump: single ended and differential ended can be implemented and available. This work focuses on single ended CPs.
Similar way many other CP PLLs are experimented in literature [1] - [6].Low power PLL is designed and simulated with current splitting technique-based CP in literature [1]. Current starved differential delay cell VCO and linear PFD is implemented in loop to successfully achieve reduced spur. Switch at source is power full of way reducing charge sharing effect in CP. It is adopted with reverse leakage compensation technique in literature [2] to reduce spur in wideband PLL. In literature [2] Charge pump and reconfigurable ring VCO.is proposed. CP is functioning is free from effects of current mirror. The design efficiently works for 0.8GHz to 28.2GHz with 0.82ps RMS jitter. Integer N third order 2.4 GHz PLL is implemented in literature [3]. Literature [6] structures a Digital PLL to work in digital mode and analog mode for coarse and final tuning. Here Storage cells are utilized to tune digitally, and achieving 0.8ps jitter.
Literature [7] exploits high swing cascode current source and switch at source to achieve current mismatch 0.01% with 3.3v, 90nm technology. Literature [8] incorporates rail to rail opamp and cascode structure to design precise charge pump with 1.8V, 90nm technology. Present work is continuation of literature [7], [8]. In this work proposed charge pump as in [7] and [8] is incorporated in CP PLL loop to determine its performances as current mismatch and proper control voltage to reduce jitter generated through processing by loop iterations. The work implements the loop blocks like PFD with reset delay path, VCO delay cell, passive filter and programmable divider. This work successful to execute for CP PLL as synthesizer for frequency range 0.5GHz to 10GHz with 65nm tsmc, 1.2V across Process Voltage Temperature corners.

2. CP PLL loop architecture

Incorporating Phase detection and frequency detection in CP PLL is the reason to increased acquisition range. 3rd order type II CP PLL [7], [8] is shown in Fig. 1. The CP PLL is designed for 0.5GHz to 10GHz frequency range with 100 MHz has reference frequency REF_CLK. Any other input frequency is scaled to 100 MHz using pre-scaler. UPand DNare the inputs for CP switches to produce control voltage $V_{ctrl}$with passive loop filter components RP, CP and C2. VCO Output frequencyis divided through divider by N to input as feedback frequency FB_CLK to PFD. The iteration is succeeding to lock for reference frequency with reduced jitter and settling time.

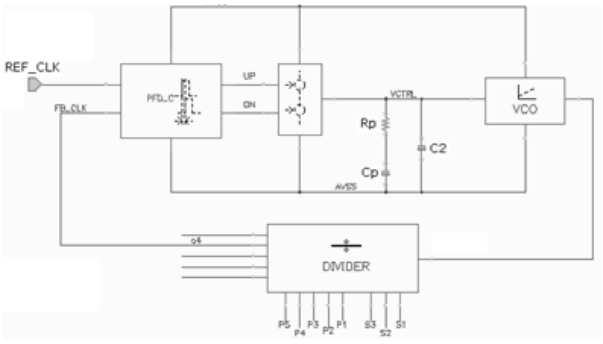


Fig. 1: 3rd Order Type II CP PLL Frequency Synthesizer.

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2.1. Phase frequency detector

A digital PFD is chosen because of the ease of implementation and built in frequency detector feature for low frequencies. The circuit implementation of the functional block shown in Fig.2. It is insensitive to duty cycle. Inverter delay units are added in reset path to eliminate the dead zone issue. The critical path is limited by just three gate delays: two from the cross-coupled, two-input NANDs, and on from the four the four-input reset NAND. The output of the PFD produces UP, DOWN and their complements.

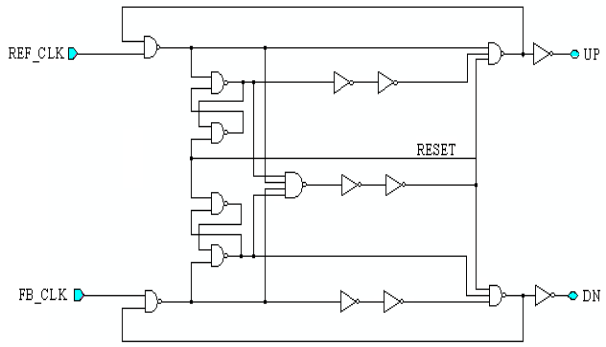


Fig. 2: PFD with Reset Delay.

2.2. Design of new charge pump

Charge pump proposed in literature [8] is redesigned to scale for technology 65nm 1.2V. To achieve current matching between UP and DN charge pump is designed as shown in Fig.3. Rail to rail error amplifier is adopted to follow voltage. Source switch charge pump directly avoids charge sharing because switch is away from output capacitor. Fig. 4 shows current matching of CP variation across CPOUT is less than 0.05%. CP is designed for 100uA current for supply 1.2V.

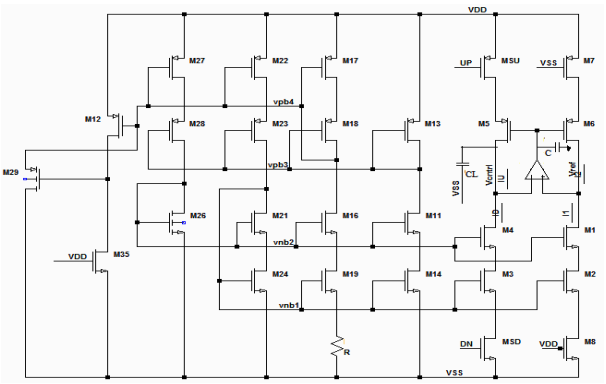


Fig. 3: charge Pumpcircuit.

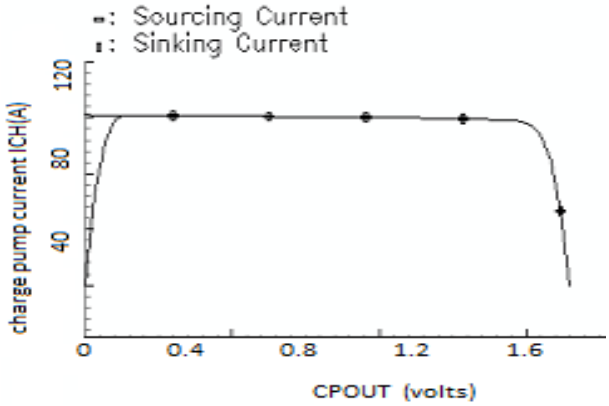


Fig. 4: Charge Pump Current Matching Characteristics

2.3. Loop filter

By integrating CP in PLL loop, the use active filters are eliminated. Active filter generates noise and limited by offset voltage.Passive filters have no inherent offset voltage [10]. System requirements demands active or passive filter(PF). In this work passive low pass filter adds value to obtain stability in loop. It is easy way to change the dynamics of the PLL and to remove high frequency noise.The filter components can be experimented and obtained through modelling. The closed loop transfer function of the Charge pump PLL is given by transfer function H(S) [7],

$$H(s)=\frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s+1)}{s^2+\frac{I_P}{2\pi}\frac{K_{VCO}R_P s}{N}+\frac{I_P K_{VCO}}{2\pi C_P N}} \quad (1)$$

Where K_{VCO} is VCO gain and I_P is charge pump current
The loop filter values are

$$C_P=\sqrt{\frac{I_P K_{VCO}}{2\pi\omega_n N}} \quad (2)$$

$$R=\frac{2\varsigma}{\omega_n C_P} \quad (3)$$

2.3.1. Acceptable range for the ς and ω_n for loop design

The Phase margin as a function of ς [9] as

$$\phi=a\tan\left(2\varsigma\sqrt{2\varsigma^2+\sqrt{4\varsigma^4+1}}\right) \quad (4)$$

Hence if ς is between 0.5 and 2, the PM is between 51.8º and 85.8º respectively. Thus, to have stabilitythe value of damping co efficient is chosen minimum value 0.5 and maximum value 2.0.

The relation between damping coefficient ς and natural frequency ωn as [11, 9].

$$\left(\frac{\omega_{ref}}{\omega_n}\right)>\frac{\pi}{2}\left(\varsigma+\sqrt{\varsigma^2+1}\right) \quad (5)$$

$\left(\frac{\omega_{ref}}{\omega_n}\right)\geq 10$ is taken as a minimum practical value that guarantees stability. Where ω_{ref} is reference frequency.

2.4. Voltage controlled oscillator

The design of VCO incorporates differential delay cell and a level shifter. Differential operation finds advantages in environmental noise by its increased immunity and linearity. Voltage swings is maximized with output differential nature. By using current source in differential delay as in Fig.5 cell provides high speed operation. Transistor M4, M6 are biased to output of PF V_{ctrl}. M5 and M6 are diode connected helps to reduce ratio of saturation voltage. M2 and M3 are input transistor which are operated complementary input signals. M1 is tail current source for differential delay cell to set source voltage. Level shift as shown in Fig.4 is used at the output of VCO to improve swing as rail to rail for divider. Level shift uses similar symmetric load structure to reduce leakage current and providegood swing.

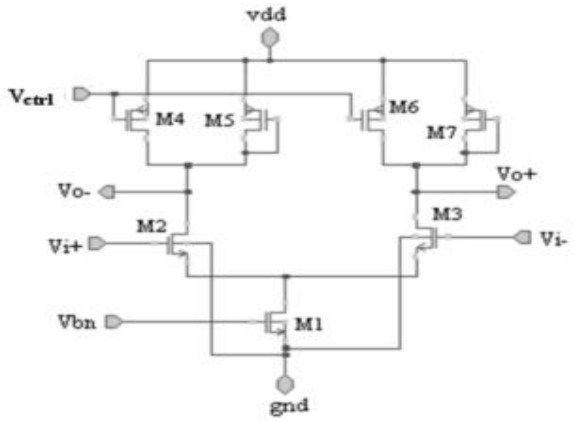


Fig. 5: Differential Delay Cell.

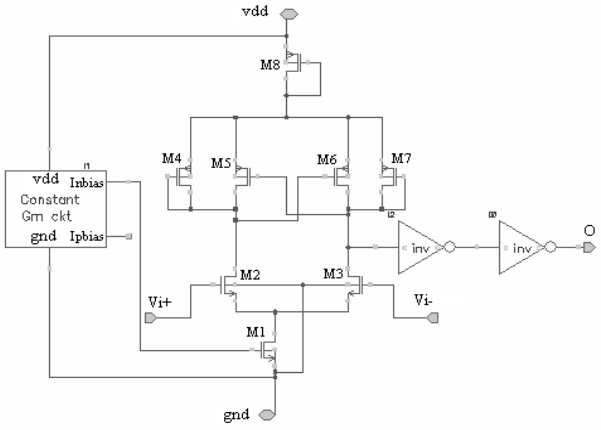


Fig. 6: Level-Shifter with Constant Gm Circuit.

The layout of the delay cells, PMOS differential amplifier, Comparator, Level-shifter are done using common centroid technique - used for differential pairs and Interdigitated method - used for current sources. Common-centroid layout, as the name implies, constructs two devices symmetrically about a common center in the layout. This allows the devices to cancel process gradients in both the x and y directions and exposes both devices to heat sources in an identical manner. Common-centriod technique creates lot of paracitics but provides better matching between differential pairs. For current sources, we use interdigitated method, which creates less paracitics. The measured VCO parameters are tabulated in Table 1.

Table 1: Measured VCO Performance

Parameter	Value
Tuning range	0.5GHz -10GHz
Peak Jitter	205ps at 1GHz
Gain	140 MHz/V
Control voltage range	0.7V- 1.1V

2.5. Divider

A programmable counter is efficient divider provided good digital design. Divider comprises fixed divider cascaded with a programmable divider.Resolution of divider is multiplication of Resolution (programmable divider) and Division ratio (fixed divider).

In digital systems, parallel load capability is used in count operation. Fig.7. shows the logic diagram down counter with parallel load capability.If the load input is 1 count sequence ceases and data transfersthe inputs I_1 I_2 I_3 into corresponding flip-flops. If the load input is 0 and the count input control is 1, the circuit operates as a down counter. The clock pulses then cause the state of the flip-flops to change accordingly to the binary count sequence. If both control inputs are 0, clock pulses do not change the state of the register.

Table 2: Function Table for the Above Counter

clear	clk	load	count	function
0	X	X	X	Clear to 0
1	X	0	0	No change
1	↓	1	X	Load inputs
1	↓	0	1	Count down net binary state

The operation of the counter is summarized in Table 2. The four control inputs: clear, CLK, load, and count determine the next output state. The clear input is asynchronous and, when equal to 0,causes the counter to be cleared to all 0's, regardless of the presence of clock pulses or other inputs. This is indicated in the table by the X entries, which symbolize don't-care conditions for the other inputs, so their value can be either 0 or 1. The clear input must go to the 1 state for the clocked operations listed in the next three entries in the table. With the load and count inputs both at 0, the outputs do not change, whether a pulse is applied in the CLK terminal or not. A load input of 1 causes a transfer from $I_1 - I_3$ into the register during the positive edge of an input pulse. Irrespective of the value of count, input digital information is loaded because count is inhibited when the load input is 1.The count operation take over when load input is set to 0. Every positive-edge transition of clock pulse enables the next binary count, but no change of state occurs if the count input is 0. The divider simulated output waveform is shown in Fig. 8 and its peak to peak jitter is shown in Fig. 9.

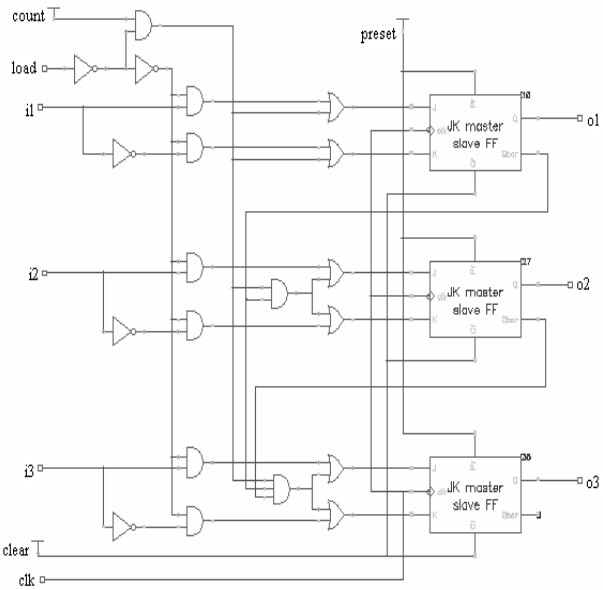


Fig. 7: 3-Bit Loadable Down Counter.

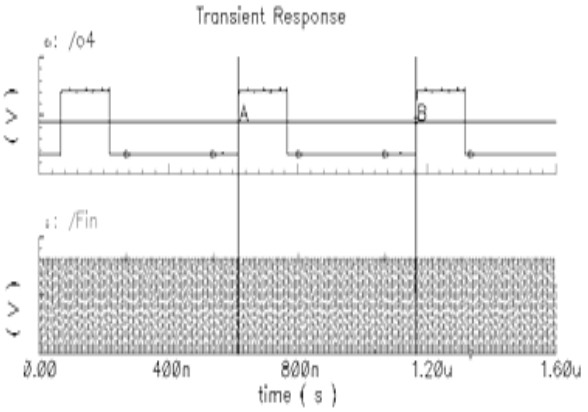


Fig. 8: The Divider Output Waveform.

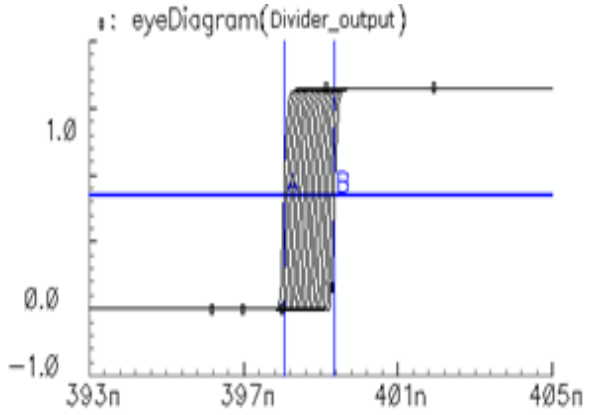


Fig. 9: Divider Jitter Calculation Using "Eye Diagram" Function In Cadence Tool Peak Jitter of the Divider = 10ns at 1 GHz.

3. Simulation results

The PFD, charge pump and loop filter are designed so that loop is stable. The By using an error amplifier and reference current sources, we can achieve a charge pump with good current matching characteristics. It shows nearly perfect current matching characteristics on the whole VCO input range. Finally, integration results of the Integer-N 0.5GHZ - 2GHz PLL Frequency synthesizer is shown in Fig. 10.

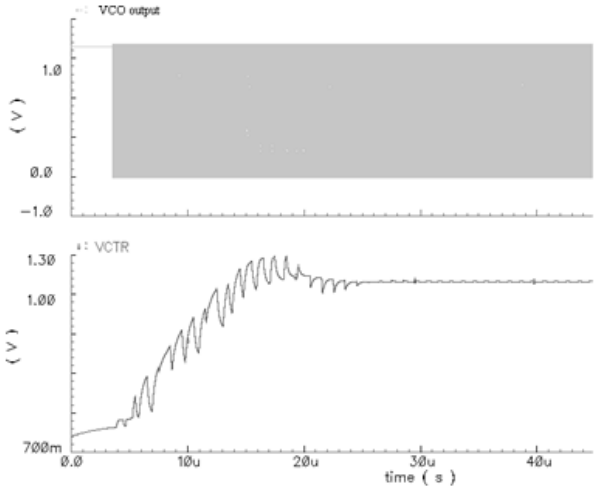


Fig. 10: VCO Output and Control Voltage Plot for CP PLL Simulation.

Table 3: Comparisons of Present Work Simulation Results with Others

	This work	[1]	[2]	[3]	[4]	[5]
Jitter dBc/Hz	-102.5	-113.5	-	-110	-126.2	130
Spur dB	-	-	28	50	-	-
Frequency range (GHZ)	0.5 – 10	4.27	0.7-1.6	2.4	0.8 – 28.2	0.8 – 3.2
Reference frequency (MHz)	100	20	10	1	10 - 400	10-40
Technology(nm)	65 CMOS	180 CMOS	65 CMOS	65 CMOS	40 CMOS	40/65 CMOS
Supply (v)	1.2	-	1.2V	0.68	1.2	-
Charge pump current (uA)	100	150	50	-	-	-
Power (mW)	2.9	4.9		0.68	1.25	-

4. Conclusions

In most electronic applications the PLL based frequency synthesizer covers the frequency spectrum from low to ultra-high frequency. The CP-PLL are advantageous than Conventional PLL. The charge pump based PLL can deliver type-II operation without the existence of op amp in the Loop Filter. This is particular benefit of CP. The PFD, CP, LF, VCO and divider are the functional blocks of the CP-PLL. In this project design and simulation of PFD, CP and LF is achieved.

The non-ideality effect of the PFD/CP/LF is dead zone, current and timing mismatch and switch errors. The architectures of PFD/CP/LF are implemented nearly to avoid dead zone and current mismatch. These architectures are designed to work at the reference frequency. VCO and the Programmable Frequency Divider are designed and simulated. VCO provides a good tuning range of 0.5GHz-10GHz with the control voltage range of 0.7V to 1.1V, which is good to use it in PLL. The symmetric load differential delay cell array offers less jitter 205ps at 1GHz compared to linear load differential delay cell array and provides high supply noise rejection. The replica bias is a self-biasing technique, provides a good bias for a range of control voltage. Finally, PFD/CP/LF is integrated with VCO and divider. The CP-PLL is simulated for output frequency range of 0.5GHz to 10 GHz.

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