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Research Paper

Implementation of ISLIP scheduler for NOC router on FPGA

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Abstract

Network on chip (NoC) effectively replaces a traditional bus based architecture in System on chip (SoC). The NoC provides a solution to the communication bottleneck of the bus based interconnection in SoC, where large numbers of Intellectual modules are integrated on a single chip for better performance. In NoC architecture, the router is a dominant component, which should provide contention free architecture with low latency. The router consists of input block, scheduler and crossbar switch. The design of scheduler leads the performance of the NoC router in terms of latency. Hence the starvation free scheduler is paramount importantin the NoC router design. iSLIP (Iterative serial line internet protocol) scheduler has programmable priority encoder which makes it fast and efficient scheduler over round robin arbiter. In this paper 2x4 NoC router using iSLIPscheduler is proposed. The proposed design is implemented using the Verilog programming on Xilinx Spartan 3 device.

Keywords: *System on Chip (SOC); Network on Chip (NOC); Router; Scheduler; Islip Scheduler; Round Robin Scheduler*

1. Introduction

Due to rapid technological evolution, it is possible tointegrate anincreasing number of circuits on a silicon wafer. This has led to the emergence of System on chip (SoC) where multiple processors, memory units and various IP modules are placed on a single chip. As the number of IP modules and processors in theSoC increases, bus based interconnection architecturescausecommunication bottlenecks. A solution for such communication bottleneck is the use of an embedded switching network, called Network on chip (NoC). The NoC provides a solution for the interconnection of IP modules and processors in the SoC.The NoC has emerged as scalable and suitable design approach to solve the interconnection problem for the SoC architecture [1].

The NoC architecture consists of three main parts, namely router, link and network interface through which cores are interconnected to NoC. The router is the heart of NoC as it coordinates data packet propagation from source to destination port based on information received from the scheduler. A Router consists of the input port, scheduler, orarbiter, crossbar and output port. In the router, scheduling algorithm decides the data packet transfer from the input devices to output devices. The scheduler allows access of cross bar switch depending on the priority scheduling algorithm, which ensures fair service to all the input devices. Scheduler plays very important role for communication of data packets in the NoC. The core function of any scheduleris to resolve the contention free requests for the same destination[2]. Since,the speed of data packets transfer of the router depends on the scheduler, the efficient design of the scheduler is of paramount importance.

In this paper, we present a design and an implementation of the scheduler on hardware such as FPGA. iSLIP (Iterative serial line internet protocol) scheduler is used to configure 2x4 crossbar switch of NoC. This scheduler is modified version of round robin arbiter in which programmable priority encoder is used to achieve a maximum throughput and to eliminate starvation [3]. This scheduler is simple to implement in hardware.

This paper is organized as follows. In section 1.2, we describedvarious schedulers and their limitations. The proposed NoC router with iSLIP scheduler implementation is given in section 1.3.In section 1.4, simulation result of iSLIP scheduler for 2x4 cross bar switch is discussed.The conclusion is given in section 1.5.

2. Various scheduler working

The scheduler plays very important role in on the chip interconnection network. The latency of data packets in a router depends mainly on the scheduling algorithm. The main function of any scheduler is to resolve conflicting requests for the same destination.A lot of research work is done on fast scheduling algorithms for crossbar switches [4]-[9]. For efficient performance of a scheduler, following properties are required [10]-[11],

- High throughput:All requested input ports should get a grant for output ports. Ideally an algorithm will sustain an offered load up to 100% on each input and output.
- Starvation Free: The algorithm should not allow any input request to be left unserved indefinitely.
- Fast: Scheduling algorithm should not become a performance bottleneck for crossbar switch interconnection. The algorithm should therefore select a crossbar configuration as quickly as possible.
- Simple to implement: Scheduling algorithm should be fast and easy to implement in hardware.

Various schedulers and their working are described below:

2.1. Simple priority arbiter

For this scheduler each requester is assigned a fixed priority. In this algorithm, the scheduler will check the priority of the requester and then assign the grant signal to cross bar switch foractive highest priority requester. This arbiter will work efficiently when NoC has few requesters.

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2.2. Round-robin arbiter (RRA)

The key limitation of a simple priority arbiter is that in very busy systems, it may possible that the low priority request may need to wait for a long time to receive a grant signal. A round-robin arbiter overcomes the limitation of simple priority arbiter. A round robin arbiter allows every requester to assign the highest priority in turn. The priority of each requester rotates in cyclic order. It operates on the principle that a request which was just served should have the lowest priority on the next round of arbitration. It gives a reliable prediction of theworst-case wait time for requesting ports. The maximum waittime for any requester is proportional to the numberof requesters minus one.

2.3. Islip arbiter

In the round robin arbiter, assigned priority to any request is rotated in cyclic order. The drawback of round robin scheduler is that, few cycles may be wasted if the lower priority requester demands for a grant signal. This is because in the round robin arbitration, each requester has some priority and a request which was served just, should be assignedthe lowest priority on the next arbitration. The priority of each node will be changed in every clock cycle in a round robin scheduler.Suppose, for 8 requester node if requester 4 has asked for grant, but for round robin arbiter, request 0 has the highest priority and no request is assigned to it, still the scheduler checks for the all high priority requests, before granting the request to node 4. Few cycles will be wasted during this task. Though the design of scheduler provides fair chance to all nodes, but it may degrade router performance, as the requester node has to wait for a long time if it is not having the highest priority.

iSLIPscheduling algorithm overcomes the problem of the round robin arbiter.iSLIP scheduler is designed in such a way that it can skip the non-requesting node and find the grant signal for the requested node specifically by keeping priority in order.iSLIP uses the principle of round robin arbiter with programmable priority encoder.The main characteristic of iSLIP is its simplicity, it is easily implemented in hardware and can operate at high speed.

In the proposed design iSLIP scheduler is implemented with programmable priority encoder.An extra port is used to decide priority for granting the request for input ports.In iSLIP scheduler, for each cycle one of the requested nodehas the highest priority for accessing a shared resource. If the highest priority requester node does not require the resource in the current cycle, thenscheduler gives access to the next highest priority requester and so on till grant signal is accepted by anyone requester.The pointer of the requester will change in round robin fashion.

3. Proposed NoC router implementation

The proposed NoC router is designed with small side buffer and iSlip scheduler with programmable priority encoder. It is implemented using following blocks,

- Input block using single side buffer memory
- iSLIP scheduler
- Cross bar Switch

In the proposed design of NoC router, input block is designed with single memory buffer instead of using a virtual channel buffer. Only deflected data packets are stored in the side buffer memory[12]. The second block is iSLIP scheduler which has programmable priority encoder and it decides the direction of data transfer. The advantage of iSLIP scheduler is that data packets are transferred to the specific direction instead of going in round robin fashion which gives fast scheduling. Following figure 1 shows the block diagram of single node NoC router.

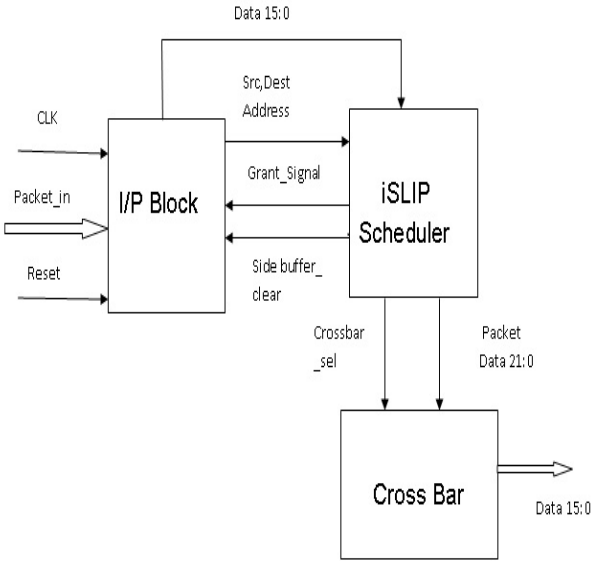


Fig .1: Single Node Noc Router.

Theproposed NoC router has implemented as 2x4 mesh topology in which 8 devices are connected.Each node is implemented using above single node architecture.Each router node is consisting of 5 ports. In 5 port router data packets are coming from 4 directions, such as North, East, West, South and the remaining one port is connected with the processing elementwhich is the core of the node.Here the port can be shared in 2 directions. Data is transmitted in 2D (2-Dimensional) directions, such as the X axis and Y axis directions. XY routing is more preferred for mesh topology.

Data packets are considered as 22 bits in which first 16 bits are data, next three bits are used for source address and the last 3 bits are used for the destination address. Source node sends the request to the scheduler for the destination port. The scheduler grants a request based on a scheduling algorithm that ensures fair service to all input ports. Once a grant is issued, the crossbar switch is configured to map the granted input ports to their destination output ports. The crossbar switch is responsible for physically connecting an input port to its destined output port, based on grant permitted by the scheduler. Here we have assumed for each router data packets are coming from 5 directions. Hence, cross bar is having grant signal in five directions, such as Xgrant _N, Xgrant_S,Xgrant_E, Xgrant_W, Xgrant_C. The router will transfer data packets from source to the destination through cross bar.

When two input ports want to access the same output port, the arbiter will resolve conflicting request for the same output port. In the proposed design, iSLIP scheduler is implemented using round robin arbiter with programmable priority encoder. Here we have assumed for each router node data packets are coming from 4 directions. The round robin arbiter is implemented using FSM with some specific priority. For example, priorities from highest to lowest are given as east,west,north and south directionsrespectively. If a data packet has to send to north direction from the input port, it has towait for a minimum two clock cycles as arbiter will give preference for higher priority ports first. This problem is solved using programmable priority encoder, in which priorities can be changed.

4. Simulation result of NOC router using ISLIP scheduler

This paper presents the design of iSLIP scheduler which is a starvation free scheduling algorithm. iSLIP uses programmable priority encoder based round robin arbiter. The design is implementedusing Verilog HDL on SPARTAN 3 family with XC3S4000 device, FG 456 package. Simulation is done by usingISIM simulator and synthesis is performed using XST tool of Xilinx ISE 14.2. The following table gives logic utilization for implemented iSLIP scheduler.

Table 1: Logic Utilization for Islip Scheduler

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	95	7168	1%
Number of 4 input LUTs	436	7168	6%
Number of bonded IOBs	202	264	76%
Number of GCLKs	1	8	12%

Simulation result of various test cases is given below in figure 2.
Test Case:
Send packet from source node 0 to destination node 2
packet_data_e = 16'h0ff02;
packet_src = 3'b000;
packet_dest = 3'b010;
grant_e= east direction
packet_out=0fffh after delay of 180 ns.
It gives latency of 6clk cycle for each node data transfer. Design works for maximum operating frequency of 72 MHz.

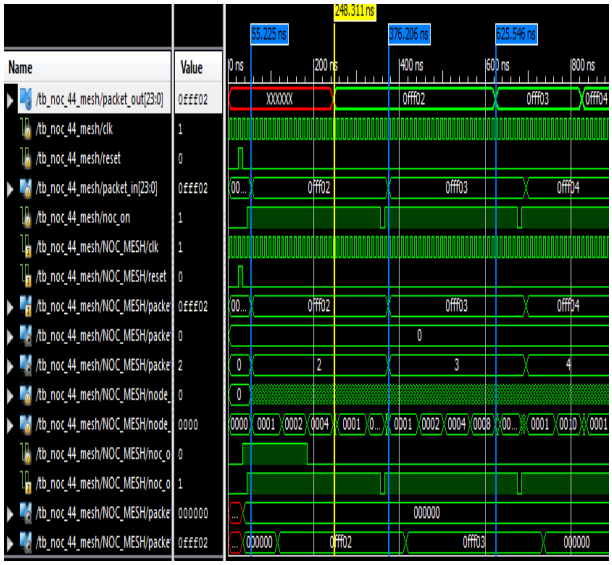


Fig. 2: Simulation Result of Islip Scheduler.

5. Conclusion

In this paper, advantage of iSLIP scheduler over round robin arbiter is discussed. To improve the speed of the router, iSLIP scheduler with programmable priority scheduling algorithm is used. iSLIP scheduler overcomes the problem of rotating priority of round robin arbiter in cyclic order. It has the property of programmable priority,hence as per the condition of an active source and destination, priority of grant signal is changed. It works as a fast scheduler for NoC router. iSLIP algorithm meets the criterion of a best scheduling algorithm which gives good performance,fast switching andsimple to implement. The synthesis and simulation of the proposed router are verified using XILINX ISE 14.2 software. In the future, we intend to work on various designs for programmable priority encoder of the scheduler for better performance.

References

[1] Atienza D., Angiolini F., Murali S., Pullini A., Benini L. and De Micheli G.: Network-on-chip design and synthesis outlook. Integration, the VLSI journal, vol.41, pp 340-359, (2008).
[2] Rantala V., Lehtonen T. and Plosila J.:Network on chip routing algorithms. Journal of Systems Architecture, TUCS Technical Report No 779, pp. 5-7, (2006).
[3] Aziz A. and Pape J.:Implementation of an on-chip interconnect using the i-SLIP scheduling algorithm. Intermediate Report – Specification and Timeline, (2006).
[4] McKeown N.:The iSLIP scheduling algorithm for input queued switches. IEEE/ACM transaction on Networking, vol. 7, pp 188-201, (1999).
[5] Belhajali D., Mbarek I.B., Hasnaoui S. and Jelassi K.: A SoC interconnection scheduling: Design and implementation of a scheduler based on credited iSLIP algorithm. International Journal of Advances in Optoelectronic Materials (AOM) vol 1, (2013).
[6] Gospodinov M. and Gospodinova E.: Analysis of iSLIP scheduling algorithm for input-queuing switches. International Conference on Computer Systems and Technologies – CompSys Tech (2004).
[7] Ruma D. and Rajrajan: Speed efficient implementation of round robin arbiter design using VERILOG International Journal of Enhanced Research in Science Technology & Engineering, vol. 2, pp1-9, (2013).
[8] Saravanakumar U. and Rajsekar K: Implementation of scheduling algorithms for on chip communications. International Journal of Computer Applications, Vol 62, (2013).
[9] Gupta P.and McKeown, N.:Designing and implementing a fast crossbar scheduler.Micro,IEEE, vol.19,pp.20-28,(1999).
[10] McKeown N. W.: Scheduling algorithms for input-queued cell switches. Doctoral Thesis, University of California at Berkeley (1995).
[11] Mahobiya D.: Designing of Efficient iSLIP Arbiter using iSLIP Scheduling Algorithm for NoC. International Journal of Scientific and Research Publication, vol.3, (2013).
[12] Fallin C., Nazario G., Yu X., Chang K., Ausavarungnirun R.and Mutlu O.:MinBD: Minimally-buffered deflection routing for energy-efficient interconnect. Networks on Chip (NoCS), IEEE/ACM International Symposium, pp. 1-10, (2012).