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Research Paper

Implementation of 16 Bit SAR ADC in CMOS and sub threshold cml techniques

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Abstract

The trends of the VLSI technology is advancing, due to this majority of the industry players are showing interest in development of the devices with ultra low power applications. Analog-to-Digital converters are getting extensively used in Medical implant machines and in lots of Sensor machines, because it is serving an imperative role in interfacing between analog signal and digital signal. This paper presents a modernistic technique called as Sub threshold Current Mode Logic (CML) for ultra low power digital components. Here 16 bit SAR ADC is designed and compared with the techniques like CMOS and STCML for power consumption and delay. Schematics are materialized with Cadence Virtuoso tool using 45nm process. The transistors in these CML and CMOS operate at threshold voltages and Sub-threshold voltages where the executable design is done using 1V to 0.5V power supply (VDD). The comparator dissipates aggrandized power, so most of the intension is converged on forming this chunk. The CML logic procedure operates primarily with the current domain, due to this the performance can be constitutionally high. This approach decreases static power dissipation.

Keywords: *Sub Threshold CML; Successive Approximation Register; Leakage Currents; Static Power Dissipation.*

1. Introduction

SAR ADC is becoming important for research because of its high performance, intermediate resolution, lesser power and lesser area. Most aspects of digital circuits and system require Ultra low-power. Achieving the low power dissipation [1] reduces the minimization of the overall leakage current. In CMOS logic, static dissipation is the primary concern with respect to the leakage currents (it is due to sub-threshold off-state leakage and gate tunneling). [2]

With the technology scaling, Power consumption of an overall system exhibits larger impacts. Reduction of supply voltage in CMOS logic slows down the performance of a circuit, so it is necessary to have a standardized high supply voltage to increase the performance of a circuit.

Voltage level escalating is not a perfect solution, hence new techniques, logics are needed to achieve better and augment systems with low energy consumption rate.

Energy consumption, [3] is the total power produced by a system over a period of time where it is the power rate at which energy is consumed to reduce energy consumption. To produce the average power it is needed to dwindle energy consumption, this can be done by curtailing the average current flow through the circuit or a system. Performance of a system can also be measured by using a PDP (power delay product).

Sub threshold Current Mode Logic is the good substitute of the conventional CMOS technologies. This STCML technique dwindles the static dissipation and is also dwindling the average current flow. For high applications compared with the CMOS logic, CML logic has reduced output voltage swing. Its consists of current bias transistor that should remain in saturation region to maintain the constant current, due to this fast switching takes place at the input differential pair transistors. If the transistor is in sub- threshold region, Vgs voltages will be below the threshold voltage.

2. Current mode logic

Current Mode Logic consists of mainly NMOS bias transistor, NMOS Differential pair transistors and PMOS load transistor. Current bias transistor can be coordinated by modifying the biasing transistor, by sizing the W/L ratios or using the threshold voltage.[4] Sub-threshold CML logic families are extensively suitable for mixed signal design. With the Current driven structure it is applicable for high frequency applications. Agility of the operation and quick switching takes place because of its lesser voltage swing. Essential pre-requisite for this logic is rear end current drive transistor should always be in the saturation region to maintain the consistent current. Always the output voltage-swing should be increased abundantly for switching the input differential pairs to the succeeding stage. [5]

CML circuits are designed using the algorithm BDD (Binary Decision diagram) [6]. This is introduced by Akers for implementing and analyzing logic for large digital functions. Each input acts as each node, each interconnection are represented as edge and output nodes represents as "0" and "1", called as leafy nodes.

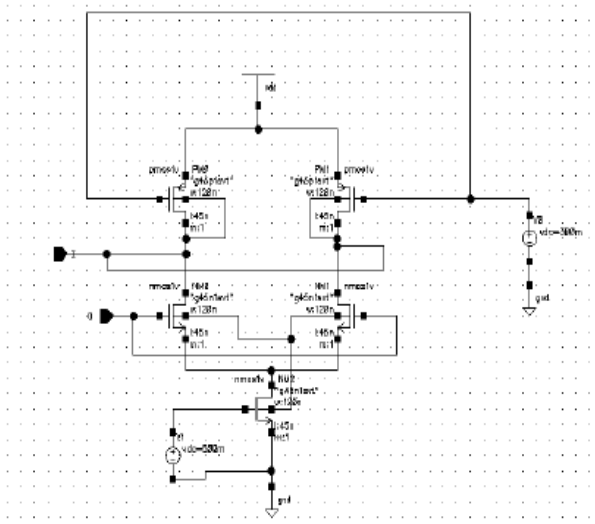

Fig. 1: Conventional CML Inverter/Buffer Circuit.

3. SAR ADC architecture

ADC (analog-to-digital converter) is very critical component in all digital communication systems. There are many ADC's with its own Excellencies and de-excellencies. To augment the converting agility and for better power consumption, excellent and simple architecture SAR ADC has been constructed and designed.[7]
Fig 2 shows the architecture of SAR ADC. Sample and Hold (S/H), Comparator are the analog components and DAC (Digital- to- analog converter) is the digital component.

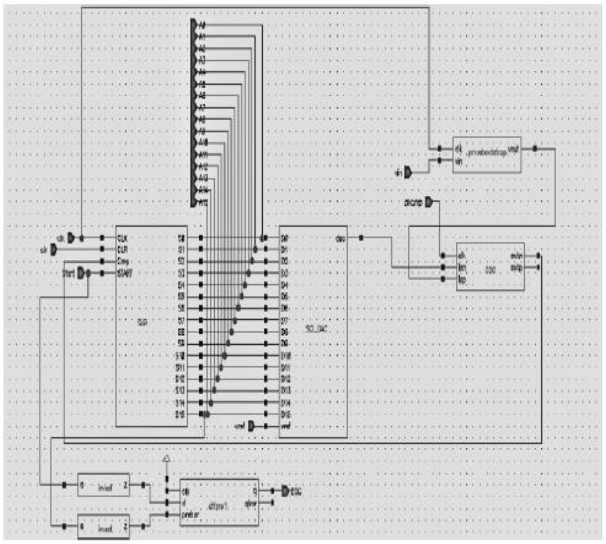

Fig. 2: SAR ADC Block Diagram.

Conversion cycle starts by resetting the SAR (Successive-Approximation register) at logic high, As soon as it reaches to LSB (least significant bit) conversion cycle ends. The positive edge of the clock cycle takes as MSB (most significant bit) it sets as "1" and other remaining bits are set as "0". Sample and Hold generates a sample signal which is given as one of the input to the comparator. The DAC (digital to analog converter) generates analog signal identical of this digital word which is given to the comparator as another input.
The comparator compares 2 inputs, it sets as logic high when the DAC output is greater than sample signal and sets as logic zero when the DAC output is lower than sample signal, it then continues till all the SAR bits are resolved.

2.1. Sample and hold

Sample and hold circuit can be occupied with digitizers to spunk a single value from the analog source, preserving that value balanced for at least the time recommended for the digitalization, and then can be set to sample a value for later time. The main operation of the sample and hold is, sampling the value of an input analog signal and holding the sampled value. Initially Sample and Hold was designed with the basic transmission gates, due to its high voltage drop later it is designed with clock booster technique. [8]

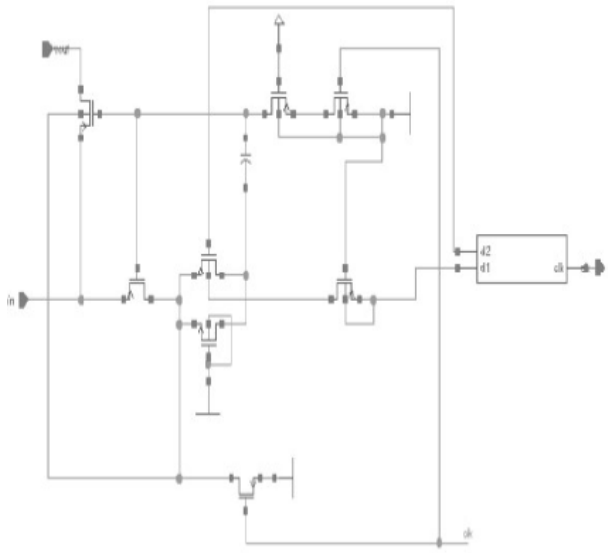

Fig. 3: Sample and Hold Using Clock Booster Technique.

Clock booster circuit contains control signal generator and a clock booster. Control signal generator generates the signal according to the range of the analog input and the clock booster strengthens the clock signal based on the equal or above the supply voltage. This Sample and Hold circuits is of PMOS. Designing with the transmission gate, clock booster and Control signal generator are not used. For CMOS logic, Transmission gate design is suitable as using high supply voltage where as for Sub threshold CML logic transmission gate design is not fruit full.

2.2. Comparator

Op-amp is not reliable as it is a power consuming technique. Conventional latch comparator is designed as it has high speed and low power dissipation. For CMOS the power consumed is 180uW with a supply voltage of 1V and for sub threshold CML the power consumed is 110nW with the supply voltage of 0.5V. For the proposed double tail comparator power consumption is reduced when compared with the conventional dynamic comparator.
This comparator operates in 2 phases: reset phase and the comparison phase. [9] In reset phase, clock will be lesser and in the comparison phase, clock will be higher. The main advantage of double tail comparator over conventional dynamic comparator is it reduces the static power consumption and also the delay.

2.3. DAC (Digital-to-analog converter)

Digital to analog converter is a digital block in SAR ADC. It performs the reverse function of ADC (analog to digital). Binary weighted capacitor array is used in designing SAR ADC. The duration of the overall Successive Approximation Register ADC is dependent on the duration of the DAC. The operation of the DAC is different for both the logics (CMOS and sub threshold CML).
Many types of architectures are there for materializing the DAC (Digital to analog converter) such as weighted binary capacitors and

resistors, split capacitor etc. In this SAR ADC design ,Binary weighted capacitors is used.

2.4. SAR register

Successive approximation registers logic can be designed in 2 architectures. First architecture consist of Ring counter and a shift register, second one is flip flops with some combinational logic. In this design SAR logic is designed with first architecture. Shift register is designed with D-flip flops with preset and clear. The outputs of the shift register are given as inputs to the ring counter.[10]
SAR ADC functions with the binary search through all the possible bits. Every bit has [3] capabilities, it maintains its value and resets to "0", or sets to "1".

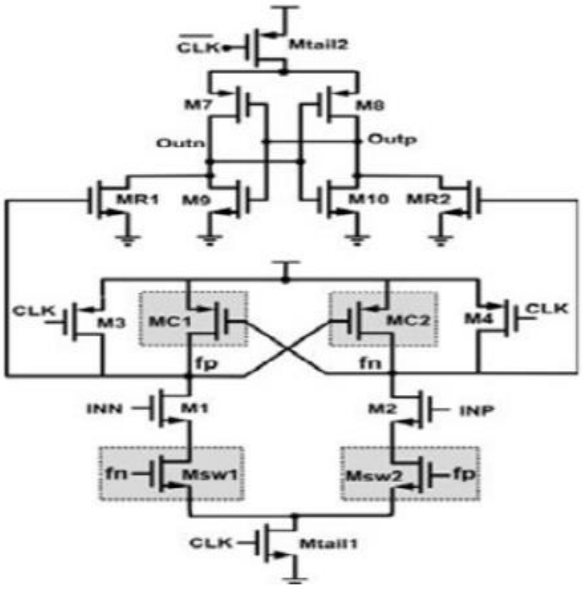

Fig. 4: Double Tail Comparator.

4. Simulation results

All the results are materialized using Cadence Virtuoso tool in 45nm technology and distinct analysis were executed for all the blocks. For calculating the power consumption and delay calculator was used in the tool.

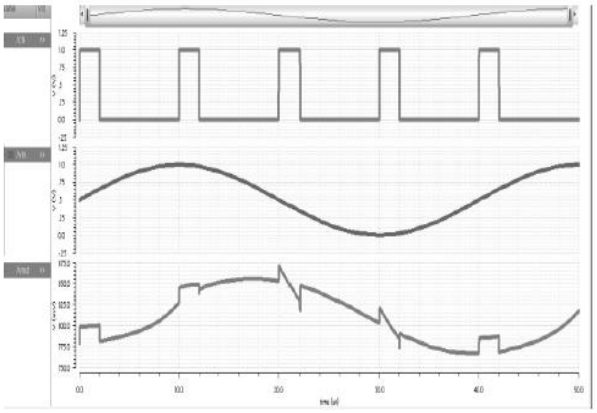

Fig. 5: Simulation Result of Sample and Hold.

Vin is the analog input signal and CLK is the clock pulse. Based on the clock or control signal the switch will be ON or OFF and it takes the samples of Vin accordingly in above fig 5

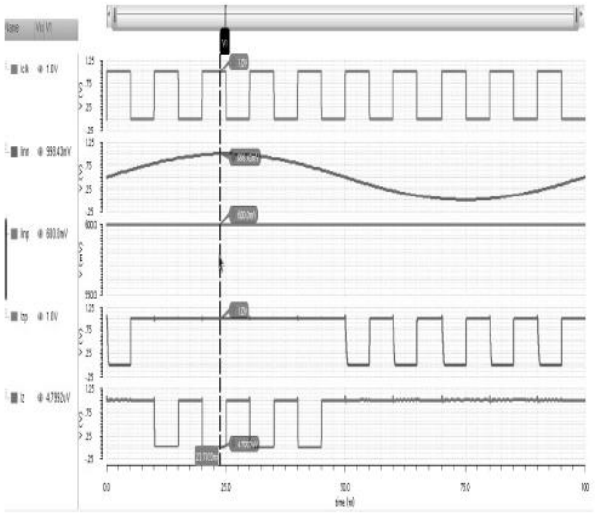

Fig. 6: Output of the Comparator.

Comparator compares the 2 inputs. First input is DAC output and the other is sampled signal. The output is amplified output. The output of the comparator is defined as follows, if the inverting terminal is less than non inverting terminal, the output n become high. If the inverting terminal is greater than non inverting terminal the output p goes high.

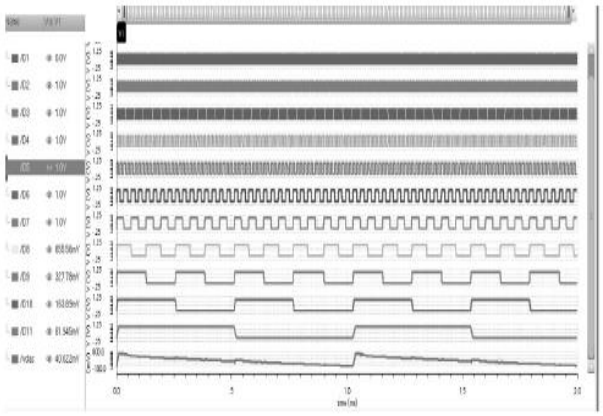

Fig. 7: Output of the DAC.

In below figure, 16 bit data (D0-D15) is applied to the DAC circuit. Analog value Identical to the data is obtained at the output of the DAC. This 16-bit data is actually the output of the SAR logic.

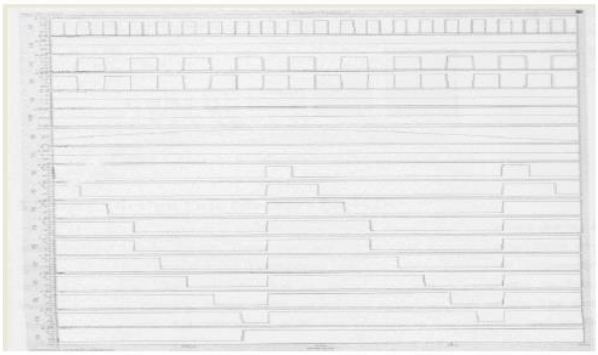

Fig. 8: Output of the SAR ADC.

A Comparisons of CMOS and ST CML technologies
Power consumption and delay in two technologies (CMOS and Sub threshold CML) for all the blocks are calculated using the tool. The power consumption for Sub threshold CML inverter is high over CMOS inverter power consumption, this is because transistors are more in CML logic over CMOS logic. But when comparing for SAR ADC, the overall power consumption for Sub threshold CML over CMOS, CML having reduced power consumption.

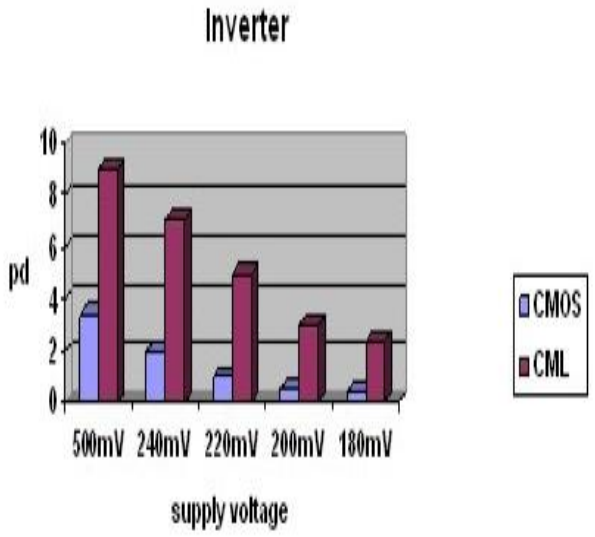

Fig.9: Comparison of Power Consumption and Supply Voltage of Inverter with the Two Technologies.

Below figure contains the delay values for both the technologies. When comparing with the Sub threshold CML over CMOS, CMOS delay is less for both the power supplies as it is very less voltage. But when comparing with the 0.5V Sub threshold CML delay decreases.

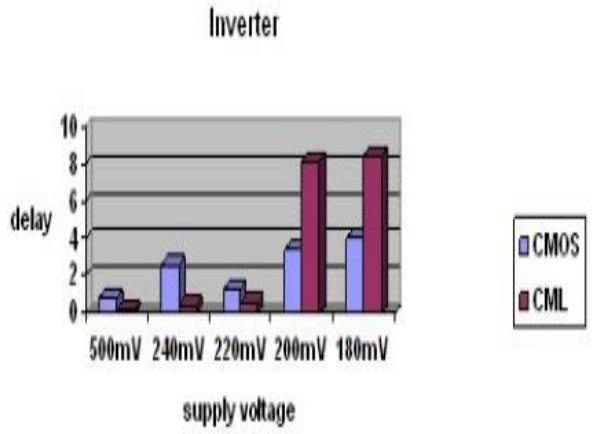

Fig. 10: Comparison of Delay and Supply Voltages of Inverter with the Two Technologies.

Table 1: Power and Delay Comparison for All the Blocks in two Technologies

	CMOS		STCML	
Blocks	Power	Delay	Power	Delay
Inverter	51.93nW	77.9ns	7.6nW	15.1ns
NAND Gate	86.69nW	1.11ns	4.81nW	20.36ns
N0R Gate	87.69nW	1.742ns	4.8nW	35.1ns
Transmission Gate	38.63nW	25us	5.8nW	30.1ns
Sample and Hold	716uW	12us	3.48uW	24.35ns
Comparator	22.17uW	10.06ns	89.9nW	40.9ns
D-FF with Clear	966uW	10us	151.5nW	56.06ns
D-FF with Preset	40.61uW	25us	159nW	141.2ns
D-FF with preset and Set	947.7nW	5us	179nW	76.33ns
DAC	3.86uW	30ns	114.7nW	58.32ns
SAR ADC	60uW	4.35us	25uW	5.35us

For digital wave forms, delay calculations are calculated Using the cadence tool and for analog waveforms delay is calculated using the rise time and fall time.

5. Conclusion

The Designs have been done using 45nm technology. This technology is implemented using GPDK (Generic process design kit) provided by cadence design system. Schematics are designed using Virtuoso Schematic Composer. Symbol creation for the schematic is done using Symbol editor. Simulations are done using ADE (Analog Design Environment) with Spectre Simulator. A 16 bit SAR ADC is designed and compared in 2 technologies CMOS and Sub threshold CML at transistor level. For Better performance of Sample and Hold, Bootstrapping technique is used. For CMOS technique power supply of 1V and for Sub threshold CML technique power supply of 0.5V are used.. For the proposed SAR ADC implementation, the power consumption in CMOS technique is 60uW and in Sub threshold CML technique it is 25uW. Delay value for the CMOS technique is 4.35uS and for the Sub threshold CML technique it is 5.35uS.

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