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Research Paper

Design of high performance, low power sub thresholds ram using source coupled logic for implantable applications.

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Abstract

Low power circuits functioning in sub threshold were proposed in earlier seventies. Recently, growing with the need of low power consumption, the low power circuits have became more attractive. However, the act of sub threshold design logics has become sensitive to the supply voltage & process variations like temperature and so on. In sub threshold region of operations the supply voltage (Vgs) is less than the threshold (Vth).This leads to less power dissipation in over all circuit, but drastically increment in propagation delay. The major intention of the paper is to offer new low power & less delay digital circuits. SRAM is the major power drawing element and dissipation is about 40% in total power. The primary objective is to design of sub threshold SRAM design, Functionality and performance is estimated from the power and delay.The second objective is to offer novel Source coupled logic based SRAM (ST-SC SRA) M & Operating these design under sub threshold operating region. Performance is analyzed through power and delay. Finally comparing the traditional sub threshold SRAM with source coupled based SRAM in power and delay on par with the performance. Discussing some of the applications, where there is a requirement of less power and delay.

Keywords: *St-SC Sram; Sub-Threshold Sram; EEG; ECG; Pace -Makers*

1. Introduction and motivation of low-power designs

The motivation for sub threshold has been derived from the following needs. I.e. power hungry, less delay, portability, lifetime of battery, and functionality & performance.

1.1. Objectives of the paper

The major intention of the research paper is to offer new low power and less delay digital designs focused on low power circuit level models. A Source coupled logic based SRAM is one of the prominent design is the future trend based on the survey. Operating this design under sub threshold region will leads to achieve the goal. [One, [2], [3].
Selecting & designing of Source coupled logic based SRAM is the most versatile memory that occupies at least 40% of space in the chip and that will be applicable to real time.ie SRAM. Comparing the sub threshold source coupled SRAM with traditional sub threshold SRAM, in functionality using read & write operations & performance in terms of power and delay. [7], [8], [10]

1.2. Sub threshold SRAM using traditional 8T design

Write & Read Operation Write operation
The stability of the SRAM is enhanced by providing the isolation between reading port from the write bit line. Aanother set of stack transistors are used to Control the reading and write operation are done by write word line (WWL) & read word line (RWL) [4], [5].

During a read operation, the read bit line (RBL) is pre-charged & WWL is maintaining as high depending on the value stored in cross-coupled inverters during charges & discharging operations.

1.3. Read Operation

Read bit line discharges during read operation, it is treated as storage bit is either '1' or 0. Data storage nodes are completely isolated from write bit lines. But during a write operation, the WBL & WBLB lines are precharged to predetermine value. During the write operation. Additionally, there are two-word lines are used to perform write and read operation. Therefore the stability is increased and also the metal density, dynamic and leakage powers are greatly reduced [6].

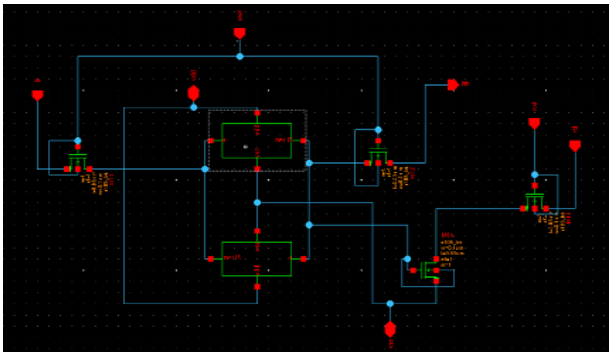


Fig. 1: Schematic Diagram of Sub Threshold SRAM.

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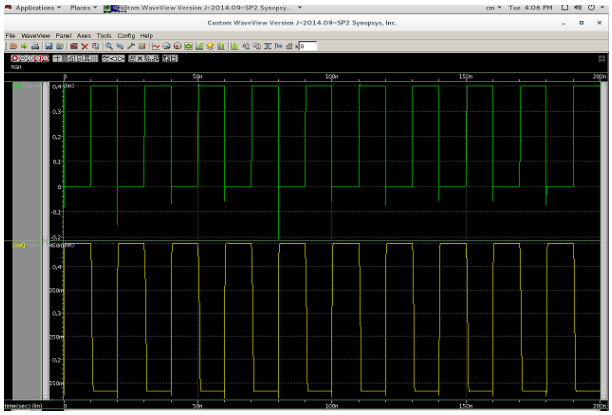


Fig. 2:.Read Operation.

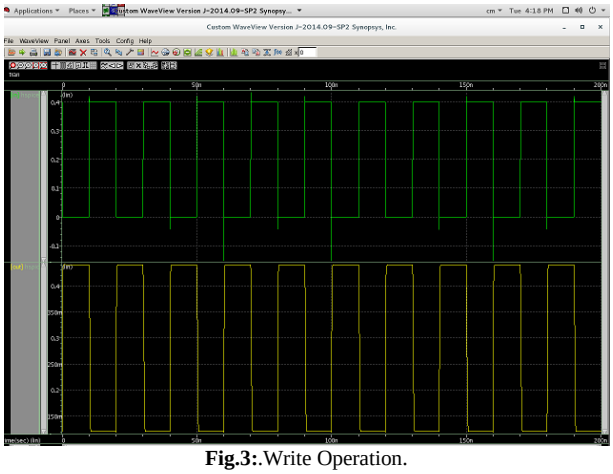


Fig.3:.Write Operation.

1.4. Power Analysis

Static Power Dissipation

As the technology is increasing, the leakage power is dominating the dynamic power under sub threshold design. Power is one of the most important parameters is to be considered in digital circuit design. As the circuit complexity is keep on increasing nowadays and operating in the sub threshold region. SRAM is a versatile component is used in most of the cache memory design. Generally, the power consumptions are idle [7], but in standby mode, the static power is dominating. Therefore we need analyze the circuit to estimate the power at a different mode of operations as showed in Fig: [1], [4].

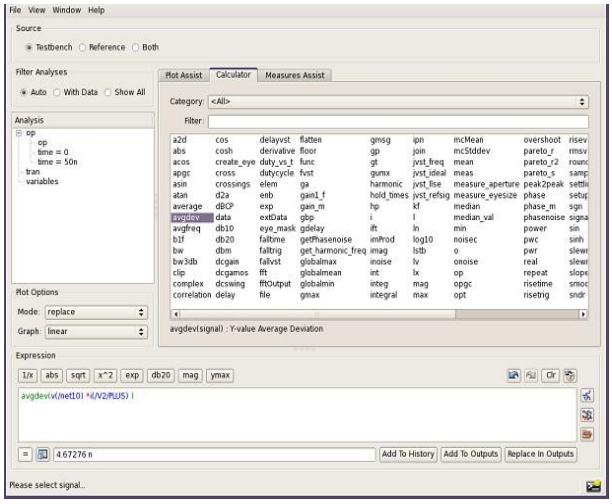


Fig. 4: Static Power Is 4.6727 NW.

Total Power Dissipation From Fig 1.5 Total power is estimated by static and dynamic power at a different mode of operation. ie in active and saturation regions. Normally the dynamic power is maximum when the supply voltage of above threshold (Vgs>Vth). But in the case of sub-threshold operation, the leakage power is dominating when Vgs<Vth, voltage and leakage power are dominating. Therefore there will maximum power dissipation across the circuit [8].

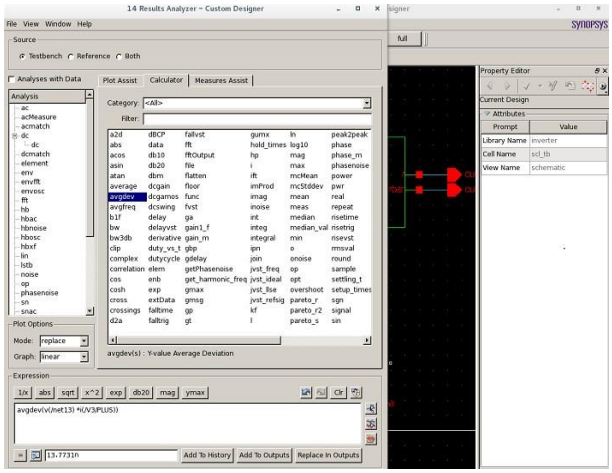


Fig. 5: Total Power Is 13.773nw.

1.5. Delay analysis

Rise Time Analysis

From the Fig: 1.6 The rise time of the SRAM is estimated by 10% to 90 % of the output response. Where the 10% is the minimum value VoL, and 90 % of the maximum value VoH of the output [9], [10].

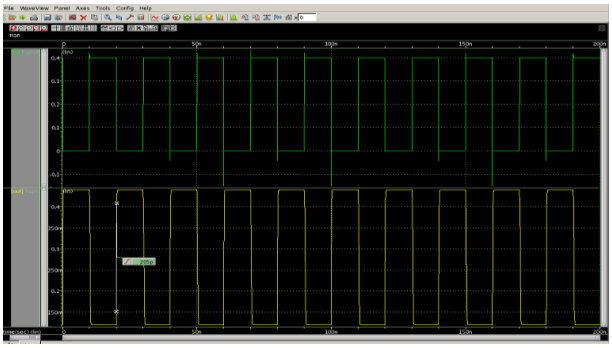
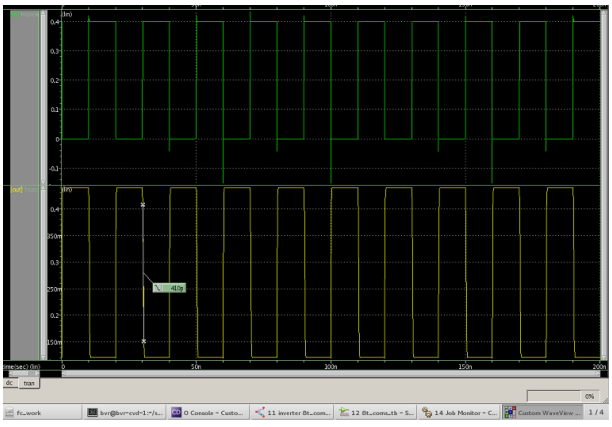


Fig. 6: Output Response of The Rise Time Is 205 Ps.

2. Fall time analysis

The fall time of SRAM is estimated by considering the 90% to 10



% of the output response. The difference of VoH to VoL is the fall time, where the VoH & VoL are the maximum & minimum voltage in output voltage and the response is showed below Fig 1.7.

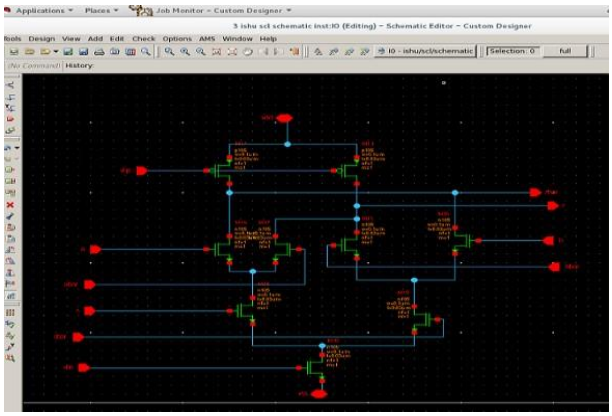


Fig. 7: Output Response of the Rise Time Is 410 Ps.

2.1. Novel design of sub threshold source coupled logic based sram design using 32nm technology

2.1.1. Introduction

A Novel approach of sub threshold source coupled logic SRAM (SCL), is one of the advanced techniques, to reduce the power and delay in digital circuits. Swing voltage is crucial in CMOS circuit while designing SRAM at high frequency of operation. These circuits are extensively used in the mixed mode of digital signal processing operations under sub-threshold region, where the noise due to supply and sub-threshold voltage is crucial [13]. Using this design, less power and maximum speed can obtained by tail biased current. The maximum output swing voltage can be obtained by avoiding relation between the power & delay.
Therefore Power delay product is made a successful method of SCL. [14] The speed of operation is depending on leakage current and independent of the supply and threshold voltage. It has better reduction in delay compared to the CMOS circuits even at low activity switching. The tail biased current Iss of SCL provides an opportunity to reduce the power at low switching activity too. This made a successful method as SCL operates with minimum supply voltages and a small logic gate depth [15].

2.2. Source-coupled logic based sram design & operation

A source coupled logic is converted into CMOS SCL by considering the PMOS & NMOS transistors are connected as shown in the below Fig 2.1.
Fig.2.1 SCL topology of Source-Coupled Logic of SRAM The main advantage of SCL is the speed over the CMOS circuit
and operates with higher frequency on a static or dynamic logic. SCL has high integration into low noise due to their differential in nature and a lack of switching noise due to the current steering mode of SCL circuits but they suffer from high power dissipation [16]. These SCL circuits are used in clock data recovery circuits to perform the power and delay performance.

3. Operation

Write Operation
When inputs ‘A’ is treated as 0v & complement of ‘A’ are treated as '0.4' v with a supply voltage of 0.4v, The first CMOS structure is acting differential pair & producing the logic value as 0.4v & vice versa
Read Operation
When inputs ‘B’ is treated as 0v & complement of ‘B’ is treated as '0.4' v with a supply voltage of 0.4v. The first CMOS structure is acting as a differential pair & producing the logic value as 0.4 v. The other differential pair is producing with 0v. This makes the sense with high current across the NMOS transistor by treating the select signals are ‘0’ & ‘1. The outputs of SCL SRAM indicate from the read & write operation as high & low values correspondingly.
Power analysis
Static Power Dissipation
The static power is estimated by the DC voltage, as the input 0.4V is applied across the design, and the current node at that input. This gives the output of power in a static mode of operation. The static power of the source coupled logic is estimated from the below
Fig 2.2Total power Dissipation
The total power is analyzed with the voltage and current across the input path of the circuit design. The product of the voltage and the current across the input, by applying a pulse with voltage values under the sub threshold operation. Therefore the dynamic power can be obtained from these inputs. The total power is estimated by static and dynamic modes of operation. The total Power of SCL is 2.16829nw, as showed from the following Fig: 2.3.

Total power =TStatic +TDynamic power

Therefore Dynamic power = total power - T static power

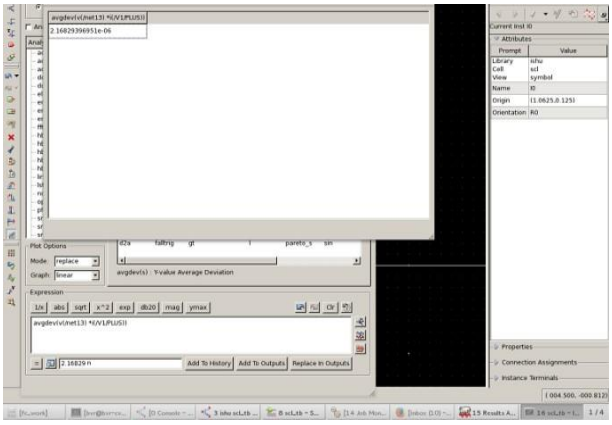


Fig. 8: Total Power of SCL SRAM 2.16829nw.

4. Delay analysis

Rise time (t_r)
In the digital circuit modeling, on and off time duration deals with the rise and fall time estimation. The characteristics from Fig 2.4 shows the 10% to 90% of rising time will give the duration of rise time. The rise time analysis is 223ps.

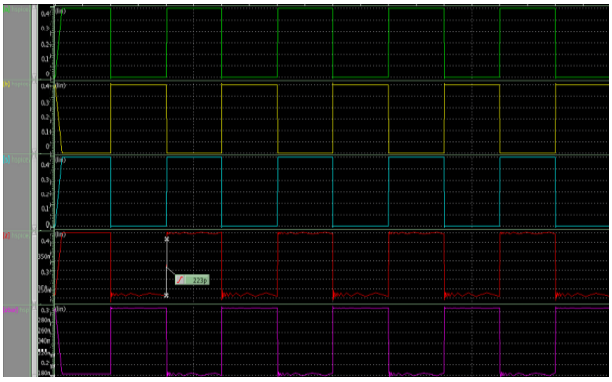


Fig. 9: Rise Time Delay Is 223 Ps.

5. Fall time (ft.)

The fall time is analyzed by with the signal at the condition, changing the state in the characteristics from 90% to 10% of response as showed in Fig 2.5 is 0.02ps.

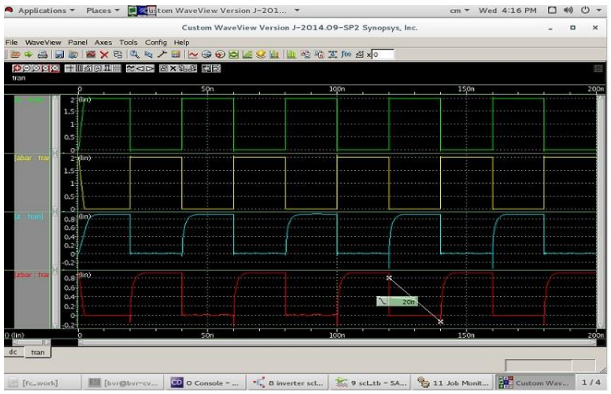


Fig. 10: Fall time Delay is 0.02ns.

Fig.2.2. Static Power of SCL inverter is 13.55µw
Novel SCL based sram is designed and compared with the existing SRAM. The functionality is analyzed based on the read and write operations, performance is estimated from power & delay. Static & dynamic, rise & fall time is quantitatively reduced in SCL based SRAM design, comparatively with sub threshold traditional SRAM design. Power is reduced by a factor of 88%, 39 % in delay and 7.5% in power delay product compared to traditional SRAM reduction.

Table 1: Comparison of Sub Threshold 8T SRAM with Sub Threshold Source Coupled SRAM

	ıreshold 8T SRAM	Sub threshold source coupled SRAM
Static power(nw)	4.497	2.16829
Dynamic power (nw)	9.276	0.01355
Total power(nw)	13.773	2.545
Rise time(ns)	0.205	0.02
Fall time(ns)	0.41	0.223
Total Delay analysis(ns)	0.615	0.243
Power Delay Product	8.47	0.636

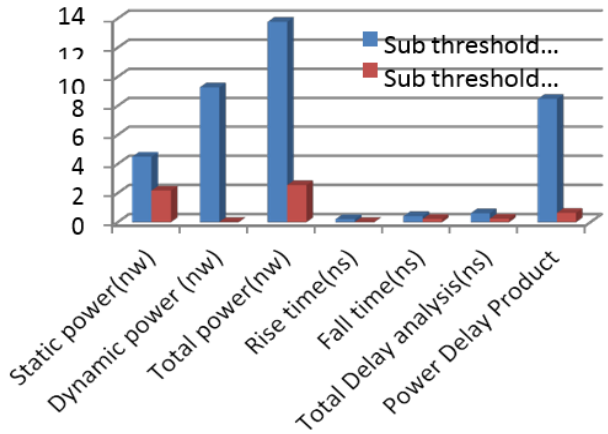
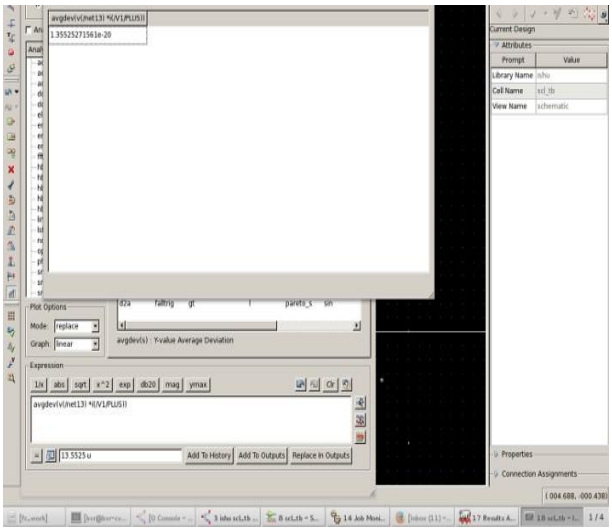


Fig. 11: Comparative Analysis of 8T SRAM with Sub Threshold Source Coupled SRAM.



6. Summary & future scope

The main application of source coupled logic is to reduce the high swing in a digital mode of operation. Therefore it can be mainly used in high frequency , low powered applications like processors & other computational operations. It also operates under sub threshold Low voltage, excellent energy saving with desired output performance. Therefore this model can be preferred for the high frequency applications, where speed is the main criteria. High activity switching rate and also better power delay product.
Low power designs like biomedical ECG, EEG, Pacemakers, where they need to operate longer duration with fewer power of fixed frequency of operation. In such bio medical equipment's can use SCL based logic memories in their designs. The amount of power consumption is depends on the circuit that run longer hours. Cache memory (L2) cache memory used in the processors in order to increase the speed, where the power is the major criteria with power, So the amount of power consumption of the circuits would be much higher than the cache memories. Therefore source coupled logic circuits can be preferred with min to a maximum speed of operations and to reduce the power

References

[1] H. N. Patel, F. B. Yahya and B. H. Calhoun, "Sub threshold SRAM: Challenges, design decisions, and solutions, pp. 321-324, (2017).
[2] N. Zheng and P. Mazumder, "Modeling and Mitigation of Static Noise Margin Variation in Sub threshold SRAM Cells, pp. 2726-2736, 2017.
[3] Yasuhisa Omura, Abhijit Mallik, and Naoto Matsuo: Performance Prospects of Sub threshold Logic Circuits by MOS Devices for Low-Voltage and Low-Energy Applications, First Edition (2017).
[4] C. B. Kushwah and S. K. Vishvakarma, "A Single-Ended With Dynamic Feedback Control 8T Sub threshold SRAM Cell," vol. 24, no. 1, pp. 373-377, Jan. (2016)
[5] P. Sharma, R. Anusha, K. Bharath, J. K. Gulati, P. K. Walia and S. J. Darak, "Quantification of figures of merit of 7T and 8T SRAM cells in sub threshold region and their comparison with the conventional 6T SRAM cell, pp. 1-2. (2016)
[6] P. Sreelakshmi, K. S. Pande and N. S. Murty, "SRAM cell with improved stability and reduced leakage current for sub threshold region of operation, pp. 1-5. (2015)
[7] S. Basuta and M. Shams, "Single-ended 6T sub-threshold SRAM with horizontal local bit-lines, pp. 1-4. 2015
[8] F. Moradi and J. K. Madsen, "Improved read and write margins using a novel 8T-SRAM cell. pp. 1-5(2014)
[9] B. Ebrahimi, H. Afzali-Kusha and A. Afzali-Kush: Low power and robust 8T/10T sub threshold SRAM cell pp.141- 144(2012).
[10] Kanika Kaur and arti noor : strategies & methodologies for low power VLSI designs: a review in International Journal of Advances in Engineering & Technology..159-165. (2011).

[11] S. Fisher, A. Teman, D. Vaysman, A. Gertsman, O. Yadid- Pecht and A. Fish : Digital sub threshold logic design - motivation and challenges pp.702-706.(2008)
[12] Ramesh Vaddi, S Dasgupta, RP Agarwal: Device and circuit co-design robustness studies in the sub threshold logic for ultra-low-power applications for 32 nm CMOS, (2010).
[13] Babayan-Mashhadi and S. Mortazavi, "A novel ultra-low- power time-domain comparator based on sub threshold source-coupled logic. pp. 471-475. (2017)
[14] Sumit Vyas and Sanjeev Rai: A Survey on Power-Delay Reduction Techniques for Ultra-Low-Power Sub threshold SCL Circuits (2012).
[15] A. Tajalli and Y. Leblebici, "Sub threshold SCL for ultra- low-power SRAM and low-activity-rate digital systems, pp. 164-167. (2009).