International Journal of Engineering & Technology, 7 (2.12) (2018) 182-183

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research Paper

An improved design of reversible adder/subtractor

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Abstract

Reversible logic has gained an importance in the fields such as Quantum computing, DNA computing, Bio informatics, Nanotechnology and Optical computing etc. This paper presents a new design of reversible adder/subtractor circuit. The proposed design has better performance than the existing counterpart in terms of reversible gates, garbage outputs and quantum cost.

Keywords: *Nanotechnology; Quantum Computing; Reversible Adder/Subtractor; Reversible Logic Gates.*

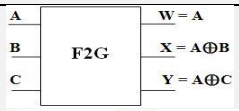
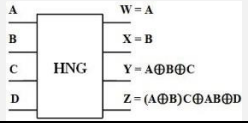
1. Introduction

Landauer principle states that for conventional logic operations, when each bit of information loss results in dissipation of KTln2 joules of energy where K= Boltzmann's constant, T= Temperature at which operation is carried out (Landauer, 1961). C.H. Bennett proved that dissipation of KTln2 amount of heat energy can be avoided if the logic operation is performed in reversible manner (Bennett, 1973).
A single digital combinational circuit that is capable of performing dual operations such as addition and subtraction depending on a control (Ctrl) bit is known as Adder/Subtractor circuit. When logic '0' is applied to the Ctrl then the circuit works as an adder and When logic '1' is applied to the Ctrl then the circuit behaves as subtractor. Adder/Subtractor circuit is used to design complex computational units like ALU, multipliers and dividers etc (Saha & Manna, 2007; Anil k. Maini, 2007)

2. Basics of reversible logic gates

A Gate is said to be reversible gate when it consists of identical inputs and outputs and also has one to one mapping between input and output vectors (Haghparast et al., 2011; Syed Mostahed Ali Chowdhury, 2003). In a system, reversible computation is carried out if the system comprises reversible gates (Vasudevan et al., 2004).
To design an optimized reversible logic circuit the parameter which plays a major role are (Haghparast et al., 2011).
Gate Count: Number of reversible gates employed in the implementation of the reversible circuit.
Constant Inputs: Inputs of reversible gate which are retain at fixed value either 0 or 1 to obtained desired output. These inputs are called constant inputs.
Garbage Outputs: Outputs of a reversible gate which are not necessary for further operations in the reversible circuit.
Quantum Cost: Number of primitive reversible gates (1x1 and 2x2) needed for reversible circuit design.
In literature, there are several types of reversible gates are existed among them two reversible gates, which are utilized in the proposed design, are illustrated in Table 1.

Table 1: Reversible Logic Gates

Reversible Gate	Logic Symbol	Quantum Cost
F2G (Parhami, 2006).		2
HNG (Haghparast et al., 2008).		6

3. proposed design

The basic building blocks of the adder/subtractor circuit are Full adder and EXOR gate. HNG is used as a full adder and Feynman double gate is used to perform EXOR operations which are needed in the adder/subtractor design. the implementation of proposed reversible 8-bit adder/subtractor circuit, eight HNG and four F2G reversible gates are utilized as shown in Figure 1. A inputs are directly applied to the HNG gates as a one of the input, where as B inputs and control (Ctrl) are applied to the Feynman double gates. Ctrl terminal is connected to the Cin and also to the one of the input of Feynman double gate. If logic '0' is applied to Ctrl, the Feynman double gates are behave as buffers whose outputs are an uncomplemented form of inputs and at this instant the circuit perform addition operation. If logic '1' is applied to the Ctrl, the Feynman double gates acts as an inverters and its input data bits are complemented, now adder performs the addition operation of A data with the complemented form of B data along with a single bit logic'1' as $C_{in.}$ This operation is identical to a subtraction operation using 2's complement (Saha & Manna N, 2007).

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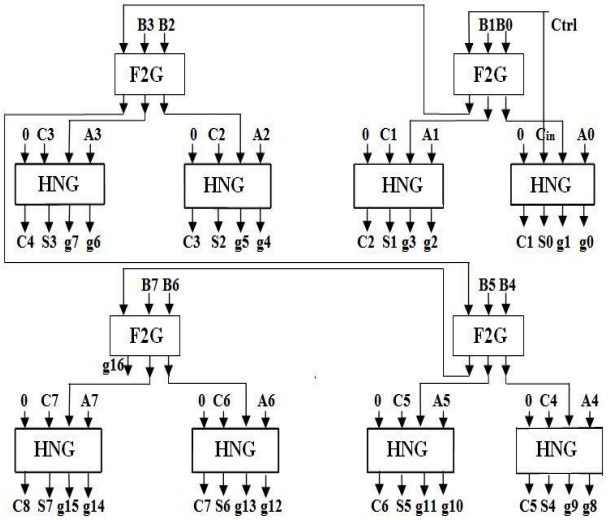


Fig. 1: Block Diagram of Proposed 8-Bit Reversible Adder/Subtractor.

The proposed 8-bit adder/subtractor design requires totally 12 reversible gates and it has a quantum constant of 56. This design utilizes eight constant inputs and generates 17 garbage outputs. The number of reversible gates (gate count), garbage outputs, constant inputs and quantum cost for N bit reversible adder/subtractor are as follows.

$$\text{Reversible gates} = N + (N/2)$$

$$\text{Garbage outputs} = 2N + 1$$

$$\text{Constant inputs} = N$$

$$\text{Quantum cost} = 7N$$

4. Simulation results and comparison

The proposed reversible adder/subtractor circuit is coded using Verilog HDL. The operation of a proposed reversible adder/subtractor design was tested by simulation process which is done in Xilinx 14.3 by creating a test bench written in a Verilog HDL. The simulation waveforms of the proposed reversible adder/subtractor as an adder and a subtractor is shown in Figure 2 and Figure 3 respectively.



Fig. 2: Proposed Design Simulation Waveforms as an Adder.

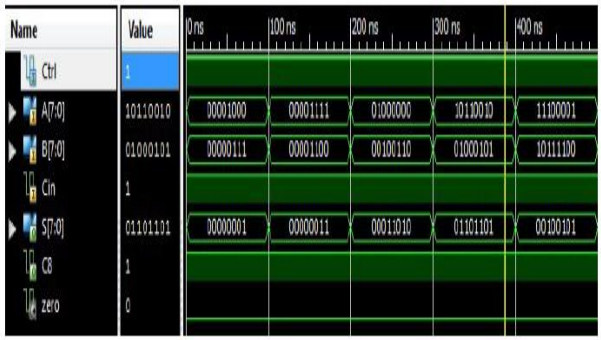


Fig. 3: Proposed design simulation waveforms as a Subtractor.

Table 2 shows the comparison between proposed and existing designs for 8- bit reversible adder/subtractor. The comparison is done on the design constraints such as reversible gates, garbage outputs, constant inputs and quantum cost.

Table 2: Comparison of 8-Bit Reversible Adder/Subtractor.

Designs	Reversible Gates	Garbage outputs	Constant inputs	Quantum Cost
Existing (Rangaraju et al., 2011).	31	23	08	76
Proposed	12	17	08	56
N bit	$N+(N/2)$	$2N+1$	N	$7N$

5. Conclusion

This article presented a new design for reversible adder/subtractor circuit. Table 2 illustrates that reversible gates required, garbage outputs generated and quantum cost of the presented design are optimized than the existing ones. The proposed design can be further extended to N bits and it may be used in large computational systems like quantum computers.

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