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***Research Paper***

# Design of High-Speed Multiplier Architecture Based on Vedic Mathematics

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**Abstract**

High speed and efficient multipliers are essential components in today's computational circuits like digital signal processing, algorithms for cryptography and high performance processors. Invariably, almost all processing units will contain hardware multipliers based on some algorithm that fits the application requirement. Tremendous advances in VLSI technology over the past several years resulted in an increased need for high speed multipliers and compelled the designers to go for trade-offs among speed, power consumption and area. Amongst various methods of multiplication, Vedic multipliers are gaining ground due to their expected improvement in performance. A novel multiplier design for high speed VLSI applications using Urdhva-Tiryagbhyamsutra of Vedic Multiplication has been presented in this paper. The multiplier architecture is implemented using Verilog coding and synthesise during Cadence RTL Compiler. Physical design is implemented using Cadence Encounter RTL-to-GDSII System using standard 180nm technology. The proposed multiplier architecture is compared with the conventional multiplier and the results show significant improvement in speed and power dissipation.

***Keywords***: *Binary Multiplication, Multiplier Architecture, Vedic Multiplier.*

## 1. Introduction

One of the most important classes of integrated circuits is processors. Over the years, the density of integration has grown tremendously and hence, today, it is possible to have large number of functionalities packed in an IC. As the number of functions increases, the need for computation also grows. Also, with the advent of new process technologies, shrinking of feature size coupled with the availability of modern CAD tools we could develop complex integrated circuits for various applications such as digital signal processing, mobile computations and communications, multimedia applications and processing required for scientific computing and applications. One of the main functional blocks in such circuits is arithmetic unit - the most important part of the processors- whose speed and efficiency are very crucial for meeting the requirements of the applications they have to support [1].

Multipliers have become an integral part of modern processors and computation systems. Especially, in digital signal processors speed of the computation is extremely important in addition to low power dissipation. Therefore, there is growing demand for low power and high performance multipliers [2]. As multiplication is a crucial arithmetic operation in processors and digital computer systems, multipliers are the core building block for many algorithms in a wide variety of computing applications [3, 4]. Although multipliers are main arithmetic components used for processing scientific data, the excessive power consumption and delay attracts attention from the research community. The current trends in architectures have been shifting towards multiple arithmetic cores working in parallel so that they can process large amounts of data with relatively low power and delay. Unfortunately, traditional arithmetic units dissipate large amounts of power [5].Thus there is a need to look at special multiplier architectures to be designed and implemented in appropriate circuit design styles[6-10] to achieve computation at low power, besides providing high performance. As the complexity of arithmetic core increases, the need for low power multipliers with adequate performance also grows.

In order to address the low power computation along with high performance, a new approach to multiplier design based on ancient Vedic Mathematics has been explored. The mathematical operations using Vedic mathematics are very fast and require less hardware. This aspect of Vedic mathematics can be utilised to increase the computational speed of multipliers. This paper describes the design and implementation of an 8 bit Vedic multiplier based on Urdhva-Tiryagbhyam Sutra. The number of steps required to perform a multiplication operation by using UrdhvaTiryagbhyam Sutra are considerably less compared to the conventional multiplication techniques [11]. In this paper, we have further explored a novel method to enhance the speed of a Vedic multiplier by replacing the existing full adders and half adders with multiplexers. The implementation of pre-computation logic using multiplexer based adder and XOR logic resulted in reduction of

delay. Moreover, in this paper, we also propose modifications to the conventional architecture of multiplier so as to reduce the power-delay product. The structure of the paper is divided as follows: The methodology and the architecture of the proposed Vedic multiplier is given in section 2 and section 3 respectively. Results are presented in section 4. Finally, conclusion and future research is given in section 5.

## 2. Methodology of Proposed Vedic Multiplier

The stepwise flow of the proposed Vedic Multiplier has been shown in Figure 1. The 8 bit binary inputs A[7:0] and B[7:0] are sent to the Vedic_4_bit_mul (4×4 bit Vedic multiplier) in pairs of 4 bits. The 8 bit outputs from each 4 bit Vedic multiplier are arranged as shown in the first block of the flow diagram. The carries obtained from each column are calculated and also the partial products of each column are XORed column wise side by side. As shown I the second block in the flow diagram the pre-calculated carries and the XORed partial products are XORed column wise to obtain the 8×8 product P[15:0]

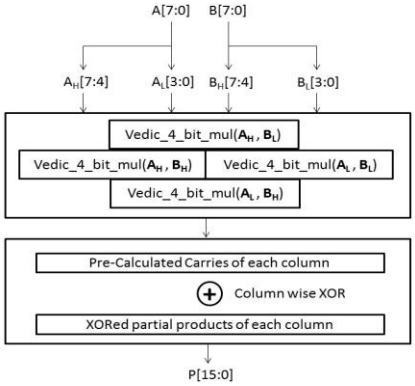


**Figure 1:** Bitwise flow diagram of 8×8 Vedic Multiplier

## 3. Architecture of Proposed Vedic Multiplier

In our proposed Vedic multiplier an 8 bit Binary Vedic multiplication is realized using 4-bit Vedic multiplication, Figure 2 shows 4 bit Vedic multiplication where A3,A2,A1,A0 & B3,B2,B1,B0 are 4 bit binary inputs and P7,P6,P5,P4,P3,P2,P1,P0 are the binary output bits.

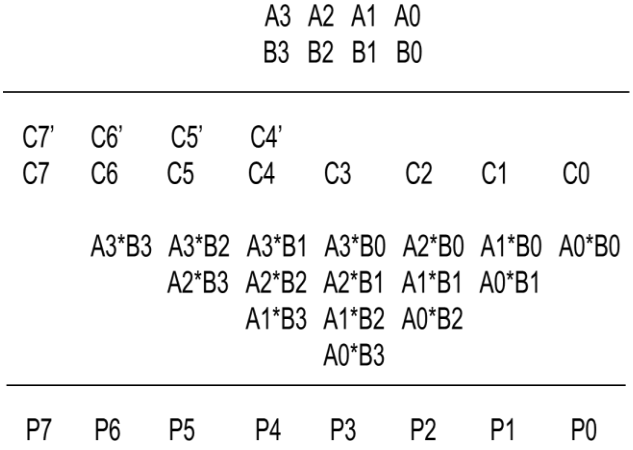


**Figure 2:** 4 bit Vedic Multiplication

Figure 3 shows a block where two 4 bits binary inputs are given to Vedic_4_bit_mul which produces 8 bit binary product. Pre-computation is used in this method, while calculating the product the column wise carries are obtained first by using MUX addition also the product values are obtained during this process. Finally, the column wise P [15:0] values are obtained by XORing the values in each column.

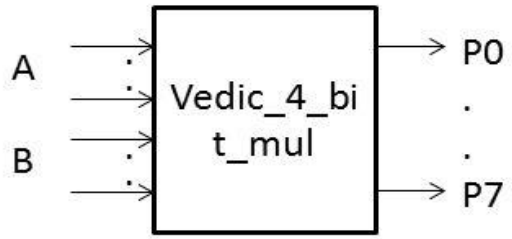


**Figure 3:** Block Diagram of a 4 bit Vedic Multiplication

This unit of 4 bit multiplier was used to perform the 8 bit multiplication as shown in the Figure6 where AH is A7 A6 A5 A4, AL is A3 A2 A1 A0, BH is B7 B6 B5 B4 & BL is B3 B2 B1 B0. The outputs from Vedic_4_bit_mul are positioned as shown in the Figure 4 [13] for addition and the carries are generated using MUX based addition. After the pre-computation, the calculated carries from each column and the outputs of 4 bit Vedic modules are placed as shown in Figure 5 and XORed to obtain the final product P [15:0].The output gives the final 16 bit product which is obtained in a parallel mechanism instead of sequential mechanism.

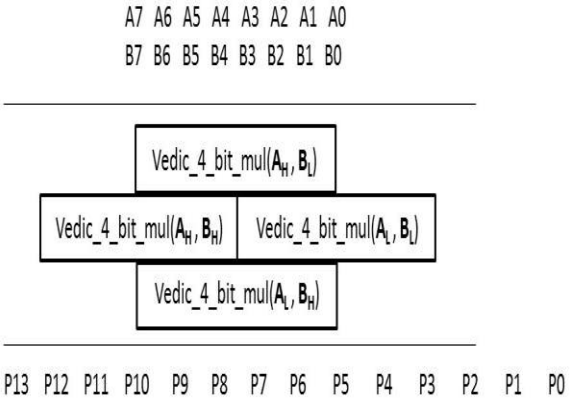


**Figure 4:** 8 bit Vedic Multiplication

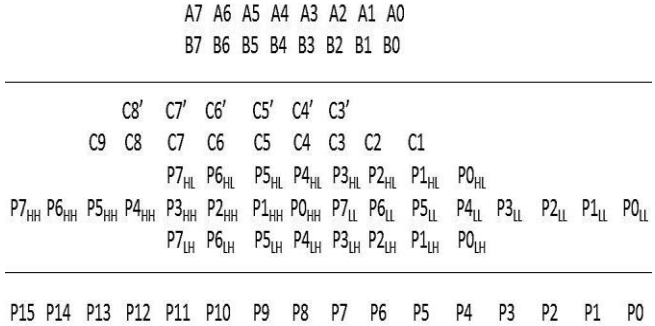


**Figure 5:** 8 bit Vedic Multiplier with expanded 4 bit module

## 4. Results

The synthesis of conventional & Vedic multiplier digital circuits was implemented using Verilog coding with the help of Cadence Encounter RTL Compiler in 180nm technology. The physical Design for the multipliers was obtained using Cadence Encounter RTL-to-GDSII System. The input to the tool was the netlist file generated from the Cadence Encounter RTL Compiler. The remaining parameters and specifications used were standard values already specified within the tool. While inputting the Import Design Browser in the Physical Design, the MMMC File is set with both the best and worst case libraries. Delay, Power & Area was estimated from the Physical Designs.

The results obtained from the proposed multiplier are given in the table 1 and 2. Cadence Design Compiler was made use of while synthesis and Cadence Encounter RTL-to-GDSII System for obtaining the Physical Layout using standard 180nm technology. The Physical layout of the proposed multiplier has been shown in Figure 6.

The Power-Delay Product obtained from the Vedic Multiplier is 29.62 % less than the conventional Multiplier. But, the area is 11.54 % more than the conventional design. The delay was 20.94 % less than the Conventional Multiplier delay which is within the target specification i.e., 10 to 30%. The high speed multiplication is achieved with the overhead in area and power.

## 5. Conclusion

In this paper, a high speed and low power architecture for multiplier was proposed using algorithm based on Vedic mathematics. An 8 bit Vedic Multiplier using Urdhva-Tiryagbhyam Sutra has been designed and implemented. The conventional architecture has been integrated with pre-computation logic in which adders were replaced by multiplexers.

The results show that the architecture is 20.94% faster, dissipates 10.99% less power and 29.62 % improvement in terms of power delay product when simulated in 180nm technology. This clearly demonstrates that the primary objective of design of an efficient multiplier and reduction of power-delay product in comparison with conventional multiplier and divider has been achieved. This will surely help increasethe computation speed of MAC and other Arithmetic units in processors, leading to faster execution of instructions.

**Table 1:** Summary of Post Synthesis Layout Results for Multiplier using Cadence

| FACTORS | VEDIC MULTIPLIER | CONVENTIONAL MULTIPLIER | PERCENTAGE CHANGE |
|---|---|---|---|
| DELAY(ns) | 4.029 | 5.967 | 32.48% |
| LEAKAGE POWER(μW) | 6.79 | 7.43 | 8.66% |
| DYNAMIC POWER(μW) | 95.20 | 86.59 | - 9.94% |
| TOTAL POWER(μW) | 101.99 | 94.02 | - 8.47% |
| TOTAL AREA | 1667 | 1516 | - 9.96% |
| POWER DELAY PRODUCT | 410.92 | 561.04 | 26.75 % |

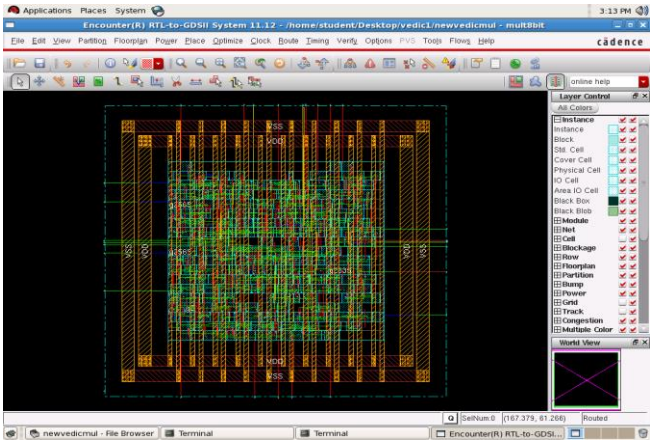

**Figure 6:** Physical Design Layout of Vedic Multiplier

**Table 2:** Summary of Post Physical Design Results for Multiplier using Cadence

| FACTORS | VEDIC MULTIPLIER | CONVENTIONAL MULTIPLIER | PERCENTAGE CHANGE |
|---|---|---|---|
| DELAY(ns) | 7.578 | 9.585 | 20.94 % |
| LEAKAGE POWER(μW) | 0.2678 | 0.4075 | 34.28 % |
| SWITCHING POWER( μW) | 233.8 | 188.4 | - 24.10 % |
| INTERNAL POWER( μW) | 292.7 | 402.9 | 27.35 % |
| TOTAL POWER(μW) | 526.7 | 591.7 | 10.99 % |
| TOTAL AREA($\mu m^2$) | 25,642.5 | 22,989.69 | - 11.54 % |
| POWER DELAY PRODUCT | 3,991.33 | 5,671.44 | 29.62 % |

The power dissipation can be further reduced by employing existing low power techniques like Dynamic Voltage Scaling, operand isolation, use of Multiple Vth devices etc., in the design of multiplier. Reduction of delay can be further improved by designing the pre-computation logic using Quine McCluskey solver in such a way that the number of carries generated in each column will be reduced.

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