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Research Paper

Comparative analysis of SRAM cell with leakage power reduction approaches

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Abstract

In deep sub-micron technologies, high number of transistors is mounted onto a small chip area where, SRAM plays a vital role and is considered as a major part in many VLSI ICs because of its large density of storage and very less access time. Due to the demand of low power applications the design of low power and low voltage memory is a demanding task. In these memories majority of power dissipation depends on leakage power. This paper analyzes the basic 6T SRAM cell operation. Here two different leakage power reduction approaches are introduced to apply for basic 6T SRAM. The performance analysis of basic SRAM cell, SRAM cell using drowsy-cache approach and SRAM cell using clamping diode are designed at 130nm using Mentor Graphics IC Studio tool. The proposed SRAM cell using clamping diode proves to be a better power reduction technique in terms of power as compared with others SRAM structures. At 3.3V, power saving by the proposed SRAM cell is 20% less than associated to basic 6T SRAM Cell.

Keywords: *6T SRAM; leakage power; power dissipation; SRAM.*

1. Introduction

Every VLSI (Very Large Scale Integrated circuit) chip consists of many blocks out of which memory block is very important during any operation of chip the major usage of memory is to store the data either temporarily or permanently based on the usage of the system. Temporary storage uses the stack memory so that the data is pushed into or popped out of the stack whenever it is necessary. The permanent memory consists of both internal memory and external memory for storing the data into the chip. The internal memory is needed for execution of programs or instructions which is written on to the chip and uses chip area. It can store and retrieve data as a part of instruction that are required while executing a program. The execution becomes faster when the memory is present in the chip itself. External memory is a storage which is used to store data externally and can be connected to the chip. It can store the files which are not needed by the processors. It may include USB drives, pen drives, hard disks etc. There are many other memories used for storage purpose like Cache memories in processors, which are faster memories but expensive and store less data [1].

The VLSI chips mainly use Random access memory as On-chip memory which is volatile and non-volatile. A volatile memory store the data till the power is applied to the device later on the data in the memory is erased. While the non-volatile memory stores the data even when the power is not applied so the data is stored for long time [5]. The volatile RAM (Random Access Memory) is divided into Static RAM and Dynamic RAM. Static cells are used to have a feedback which stores the data in it, while the dynamic cells use a floating capacitor to retain its state. The SRAMs are faster than DRAM but consumes more space than DRAM so a trade-off should be there for both Area and Speed. The SRAM is best suitable for VLSI chips, it stores in the form of Bits '0' or '1'.

The SRAM is made of a semiconductor which consists of hundreds of small chips like SRAM cells. The leakage power of each small chip must be considered to implement a large memory cell because if cells are combined it will dissipate more leakage power. The packaging cost of the chip depends on the power dissipation so it is taken very seriously while implementing a VLSI chip. Along with leakage power there are many other sources of power dissipation like switching, dynamic and short circuit power dissipation etc. Generally, the leakage power has more impact on VLSI chips hence this paper deals with different methodologies to reduce the leakage power [2].

This paper gives a clear explanation of the SRAM cell and its operations in the section II. In section III, it provides various leakage power reduction approaches suitable for SRAM. In section IV proposed 6T SRAM using leakage power reduction approaches are discussed. Section V explains results and discussion. Finally, in Section VI conclusion and future scope are discussed.

2. Operation of Basic 6T SRAM cell

[4]. The 6T SRAM (6 Transistor SRAM) cell is a memory cell which stores one-bit data. As the name indicates, it contains 6 transistors in which 2 are indicated as access based upon the work they do or pass transistors and remaining 4 transistors are connected as 2 inverters in such a fashion that the output of one inverter is fed back to the input of another inverter and vice-versa. This kind of connection is called as cross coupled inverters as shown in the Figure 1. The SRAM cell has active and standby modes. The operation performed by the SRAM cell is categorized

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as reading of data, writing or manipulating the data or storing the data. In a broad way it could be categorized into active and stand by modes [4]. Active mode is to access the data or to alter it, whereas the standby mode is to store the data inside the two inverters. Based upon the modes used the output is made available by one of the inverter output represented by Q, and the other which is the complemented value of Q as Q_b.

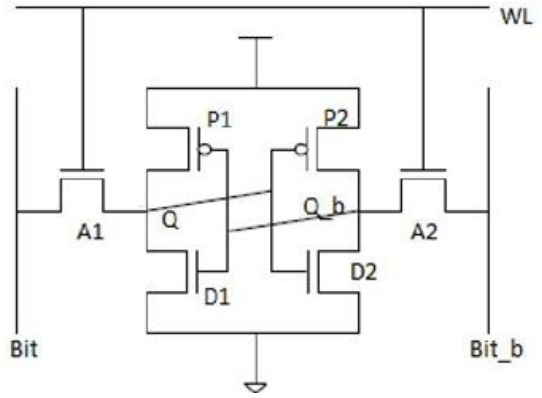


Fig. 1: Basic 6T SRAM cell

The power dissipation in the circuit is mainly due to leakage power which is being reduced to an extent by the positive feedback present in the cell. As by the name the access transistors are used to know the data present in the cell. Bit lines Bit and Bit_b drives the SRAM cell to store the desired bit and its complement respectively. The word line, WL is high during the active mode such that it could short the two access transistors. Similarly, the word line, WL is low during stand-by mode to remove the connection between the inverters and the bit-lines, therefore the data is captured in between the two inverters [6]. The data present is read by providing a high voltage to bit lines. Then by giving an active high voltage to word line, the SRAM is in active mode and the data value is retrieved by the bit line. The memory cell operation to read the data present and to alter the data in SRAM is elaborated in further sections.

2.1. Read Operation

SRAM consists of two different types of lines they are Bit line (Bit) and Word line (WL) for accessing the data present in the cell. The reading of data present in an SRAM is implemented by charging the bit lines to logic '1'. For an example, let us assume the value of Q is initially '0' then the value of Q_b will be '1' as both are complement of each other. Q_b and Bit_b must remain to logic '1'. When WL is set to logic '1', the line Bit will be set to logic '0'. As the line Bit is getting down, the value of Q will be raised simultaneously as shown in Figure 2. The drivers D1 and D2 must be strong, access transistors must be moderately strong and the pull up transistors must be weak. The transistors are in a ratio such that the node Q switching threshold must be less than the second inverter pair (P2/D2). This is called readability or read stability of SRAM Cell and the value at node Q follows the line Bit.

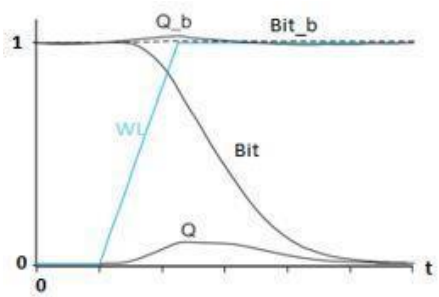


Fig. 2: Read Operation for SRAM cell

2.2. Write Operation

The SRAM cell needs to be updated as per the use of the system. To make it understandable let us consider an example to manipulate the memory cell to logic '1'and set the Bit to logic '1' and Bit_b to logic '0'. Assume the Q value is initially '0'. Due to read stability the line Bit will not allow us to read the value from A1, as shown in the Figure 3. So, the write operation must be done through Q_b. P2 must be less strong than the access transistor A2. This is called Writability or Write Stability. As the line Bit is high so the line Bit_b will be 0 and as the value of Q is '0' then the value of Q_b will be '1'. Then due to voltage drop across node Q_b its value will become '0' and the value of Q will become 1 respectively.

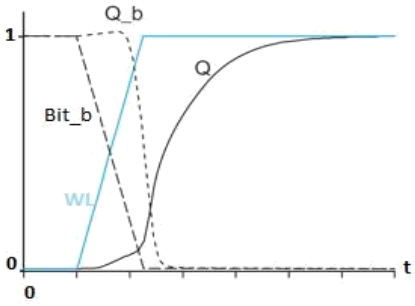


Fig. 3: Write Operation for SRAM cell

3. Leakage Power Reduction Approaches for SRAM cell

One of the major concerns in VLSI technology is to have low power dissipation and memory storage capacity must be high. When a device is in off mode then it shouldn't have any current flowing through the circuit, but due to high barrier potential the electrons are dragged towards the positive potential of the battery, which is called as reverse leakage current. The leakage power increases with increase in temperature, aspect ratio and supply voltage. Many methodologies are being developed which could reduce the leakage power in an SRAM cell. This paper explains two major leakage power reduction techniques.

3.1. Drowsy Cache Technique

Drowsy cache is the technique which is implemented by the idea that the power requirement to the cell in hold mode is less, therefore by providing less source voltage, one could reduce the power dissipation in the circuit. The drowsy cache technique includes two transistors which are the gateways to supply power. The input to these transistors is dependent upon the functionality of the cell.

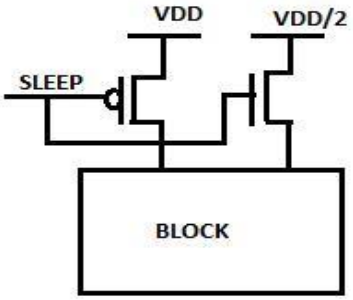


Fig. 4: Drowsy Cache Technique

The gate input to the two transistors are shorted and supplied with a sleep signal as shown in the Figure 4. This signal is low in active region such that the PMOS is ON and the VDD supply is provided to the circuit, such that the operation is done as the conventional SRAM cell. The sleep signal is high at standby mode as the requirement of power supply in this mode is less comparatively that of active mode. Hence, the voltage is divided to its half and given

to the drain of NMOS. In standby mode the NMOS transistor is ON and such the VDD/2, voltage supply is given to the SRAM cell.

3.2. Clamping Diode Technique

This technique is the most widely used technique to de-crease the power dissipation of any block of elements. The phenomenon behind clamping diode is to reduce the leakage current. In standby mode, the power supplied is not used to its full extent. Hence, this method is implemented to reduce the power by removing the un-wanted leakages. This technique is achieved by adding an NMOS with gate input to be as low power down (LPD) as shown in the Figure 5, which is high when the SRAM is in active mode and acts just like a ground with very less resistance. In standby mode, LPD is low hence the NMOS transistor is off which increases the drain voltage of NMOS.
The drawback behind this circuit is that the VSL at standby mode would be charged to a certain value which may be less immune to noise, hence getting distortions in the output wave-form which may lead to storing of erroneous elements.

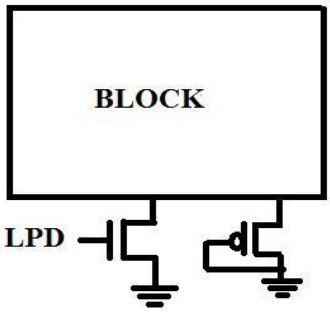


Fig. 5: Clamping Diode Technique

Therefore, to remove this drawback a PMOS is connected in parallel with the NMOS, this is called as clamping diode, as this PMOS would clamp the VSL to a fixed value, which relies upon the threshold voltage and size of PMOS transistor. When compared to NMOS the PMOS of the same size has high leakage blocking ability and it's on resistance is also high.

4. Proposed SRAM cells with Leakage Power Reduction Approaches

In the above sections, the standard 6T SRAM cell operation and different leakage power reduction approaches are elaborated. This paper implements the 6T SRAM cell with power reduction techniques which may furthermore decreases the power. The technology requires high storage which includes high number of SRAM cell. Overall, the power dissipation of the system must be low; hence for an individual SRAM cell the power dissipation must be low.

4.1. SRAM cell using Drowsy Cache Technique

The drowsy cache technique for the 6T SRAM cell is implemented by using 2 additional transistors which are connected to the VDD of the SRAM. A sleep signal(s) is given as input to both the transistors which are used to supply power. This technique reduces the power based upon the mode in which SRAM is. The additional transistors work individually in the active or standby mode based upon the SLEEP signal(s). The drowsy cache technique is implemented by additional two transistors connected to the supply, which is diagrammatically represented in Figure 6.

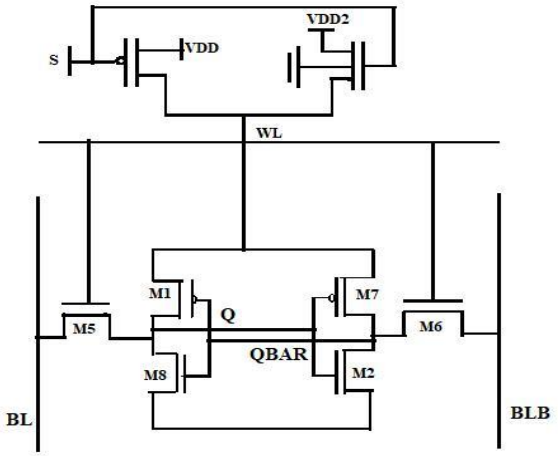


Fig. 6: 6T SRAM cell using Drowsy Cache Technique

The basic 6T SRAM cell works in 2 modes which are active mode and ideal mode. In active mode power requirement is more because it performs read and write operations for the data. The sleep signal gets logic '0' because the WL will be logic '1' during active mode. The PMOS is ON and the VDD is supplied directly to the circuit Figure 7. When the circuit is in active mode it requires a full voltage supply, so to reduce power dissipation 2 extra transistors were added.

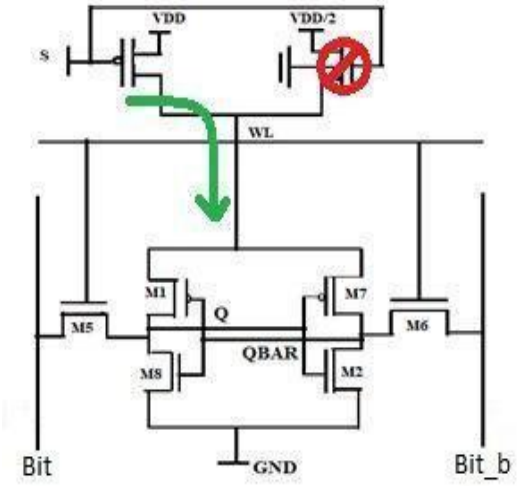


Fig. 7: Read and Write operations of 6T SRAM cell using Drowsy Cache Technique

During the ideal mode of SRAM cell, it will not perform any operations on data. It will just HOLD the data, so the supply power is leaked. To reduce the leakage power during ideal mode VDD/2 is supplied as the input to the SRAM cell through NMOS transistor. The NMOS transistor is ON only when the input of the sleep signal is a High logic which is illustrated in Figure 8. Operation is shown in the following circuit.

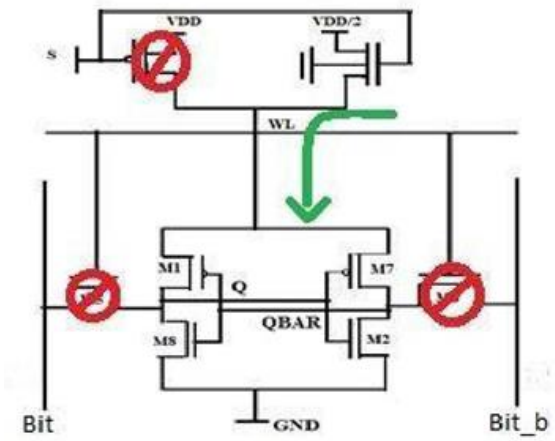


Fig. 8: Hold operation using Drowsy Cache Technique

4.2. SRAM cell using Clamping Diode Technique

Clamping diode technique has two extra transistors summed up to the SRAM cell to decrease the power dissipation. The low power down (LPD) is given to the NMOS transistor as shown in the Figure 9. This LPD signal works in a manner that it gets high in read or write operation and is low in hold operation.

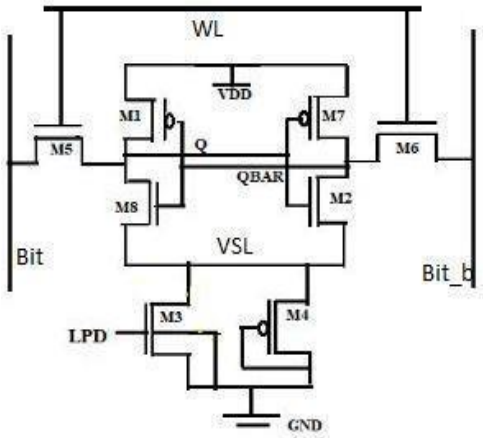


Fig. 9: Clampinf Diode Technique implemented on SRAM cell

In active mode, the low power down (LPD) signal is high such that the NMOS transistor is ON. Then the VSL is same as ground because the NMOS transistor has very less resistance therefore, the circuit operation remains same as the conventional SRAM cell which is illustrated in Figure 10.

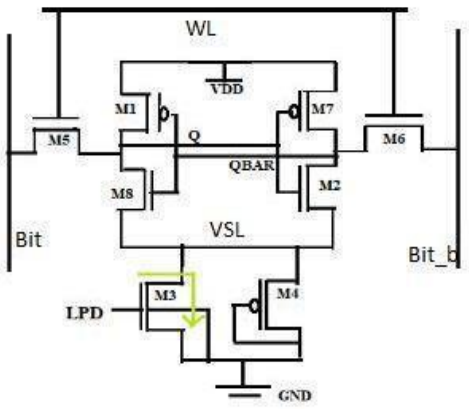


Fig. 10: Active mode of SRAM cell using clamping diode technique

In standby mode, the LPD signal is low hence the NMOS transistor is OFF, as shown in the Figure 11. The parallel connection of PMOS would maintain the VSL to a value which depends upon the PMOS transistor size and threshold voltage and the value must be less than that at other inverter side so that the data is hold. However, the ON resistance and leakage suppressing are high for PMOS when compared to an NMOS with same size.

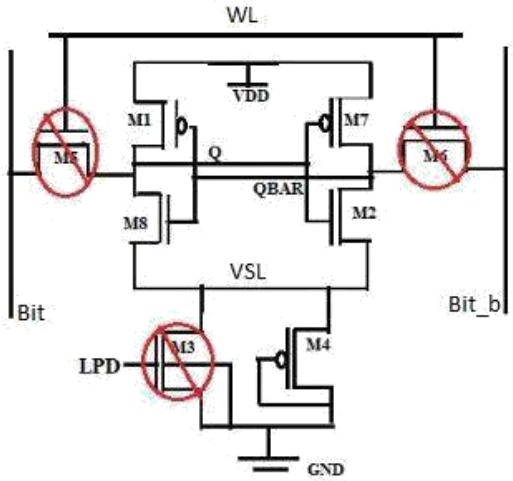


Fig. 11: Stand by mode of an SRAM cell in clmaping diode technique

5. Conclusion

The technology has been advanced such that the power consumption of an SRAM cell must be less which is a major challenge. The world today wants to store a large amount of data, as the database is increasing in a drastic manner. To meet those expectations, many SRAM cells need to be connected in a fashion that it doesn't require a high amount of power. This need could be achieved by applying some power reduction techniques. This pa-per majorly explains about drowsy cache and clamping diode power reduction techniques. The SRAM cell implemented with clamping diode technique has minimized power dissipation when compared to basic SRAM cell. This technique can be implemented in high speed registers, caches and small memory cells to reduce the overall power dissipation and to increase the overall efficiency of electronic device.

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