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Research Paper

Testing ripple carry adder using bist architecture

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Abstract

Very Large-Scale Integration has a greater impact on the developing circuit technology. The Cost and Size has been gradually reducing since years but increased the circuit complexity, there are problems which may affect the growth of VLSI technology. Among them one of major problem is circuit testing. To resolve this issue, we implement Built in Self-Test (BIST). BIST architecture is used to test the circuit itself. Engineers Design BIST to achieve high reliability and low repair cycle times. We implement Linear Feedback Shift Registers (LFSR) to generate the pseudo random test pattern and implement a ripple carry adder as circuit under test and Multiple Input Signature Register(MISR) as output response analyzer and test patterns are given to circuit under test and outputs are obtained these are compared with the actual outputs to test whether the circuit is faulty or not. To check whether the circuit is faulty or fault free we check the obtained outputs with actual outputs using Signature Analysis.

Keywords: *BIST, LFSR, MISR, Cost and Size, Signature analysis*

1. Introduction

BIST is a Hardware technique used for testing and diagnosis of circuit and the hardware which is used to implement BIST structure is not so expensive, we go for Hardware BIST because in Software testing involves low fault coverage and it is not so fast while detecting faults. In Hardware BIST we can achieve high fault coverage and improved system performance at component level [1].

As referred in [2] BIST has many testing techniques Stored-pattern technique, Exhaustive testing technique, Pseudorandom testing technique, Weighted Pseudorandom Testing technique, each technique has its own way of testing of circuit, these testing techniques can be applied to both

Combinational logic and sequential logic circuits.

As referred in [2], [3] LFSR which is test pattern generator used to generate random numbers from 0 to 2^n-1

and all zeros case is not considered because of feedback. LFSR is a Shift Register in which outputs are taken from

Exclusive-Or and the result is fed back to the input, here the sequence generated is pseudo random because the bit can be either 0 or 1 each has an equal value for generation so this sequence is repeatable

As referred in [2], [3], [4] MISR (Multiple Input Signature Register) is an extension of SISR which is used to test single output. There are many ways for to form MISR by changing the inputs of LFSR. It consists of Xor gates and D Flip Flop, since the operation of Xor gate is linear we can use different representations.

As referred in [5] A ripple carry adder can be implemented using basic full adder circuit. A basic full adder is used for adding two 'n' bit numbers which consist of An, Bn and Bn where Cn is the carry propagated after adding two numbers. The output of the adder is sum and carry. Nand and nor are the logic gates used to implement full adder. Ripple carry adder has multiple full adders used for adding n bit numbers and the output carry cout of each adder will be the input cin of the next adder.

2. Built in Self Test (BIST)

2.1 BIST Architecture:

From Fig.1 The basic Idea is to have a VLSI chip that tests itself, the typical BIST architecture is composed of three modules neglecting the circuit under test.

1) Test Pattern Generator
2) Output Response Analyzer
3) BIST Controller

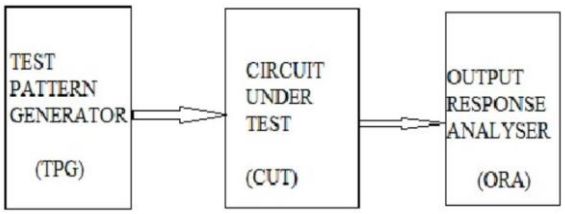


Fig 1: Basic BIST Architecture

2.2 BIST Structure with LFSR and MISR*:*

1) Here LFSR as test pattern generator
2) MISR AS OUTPUT RESPONSE ANALYZER

From the Fig.2 BIST block diagram which uses a linear feedback shift register (LFSR) as test pattern generator to generate the test vectors and multiple input signature register(MISR) to verify the output against the correct response of the circuit under test.

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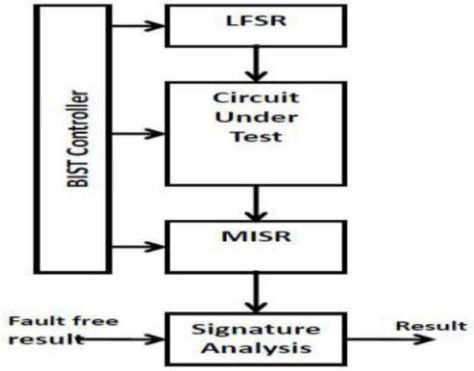


Fig 2: BIST Structure

2.3 Pseudo Random Pattern Generator

From Fig.3 for the CUT to be tested, a Pseudo random pattern generator use mostly linear feedback shift register (LFSR) to generate test vectors at the input side. When the flip-flops are entered with a seed value that is anything except all 0's (which would cause all zero pattern of LFSR) and when the circuit that is LFSR is given clock, it circuit will generate the patterns based on clock input

Standard LFSR

LFSR which is main part of the BIST architecture which can generate random numbers is useful to find the faults in the circuit.

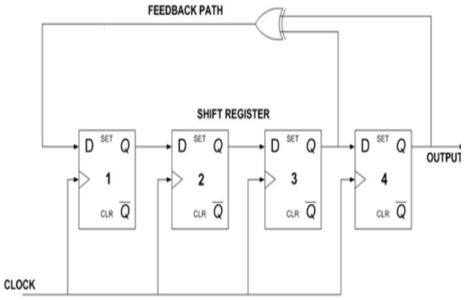


Fig 3: Standard LFSR Representation

A LFSR is a sequential shift register, it generates pseudo random test patterns based on the sequence of a binary values. It consists of D flip flops and linear exclusive Or-Gate as shown in the figure. The working of Standard LFSR is obtained by performing Ex-or operation on the outputs of two flip flops and feeding them to the input of the flip flop. In this way Test patterns are generated in the STANDARD LFSR Using D-flip flop and EX-OR Gate with using combinational logic. Test patterns that are generated by LFSR are fast and at speed with only a clock input.

2. 4 Response Compactions

In BIST architecture, for test patterns that has been generated by LFSR. The circuit under test produces the output value, so for the circuit to be fault free, the output values generated by circuit under test should be compared with the correct theoretical values, even though this is a time taken process, it is required to reduce the faults in circuit.

For example, LFSR has 2 million patterns and CUT has 180 outputs, then it gives 0.4-billion-bit response.

2.5 Output Response Analyser (ORA)

For the storage of the entire test pattern generated by the LFSR and corresponding outputs generated by circuit under test (CUT) RAM is used. When the inputs are applied to the CUT the outputs from CUT are compared with the Outputs stored in the Ram. If the output from the CUT matches the outputs stored in the RAM, then the circuit is said to be the fault free circuit otherwise we can say that it is faulty circuit. In BIST, the Test Pattern Generation and Output Response Analyzer are built inside the circuit.

2.6 Circuit Under Test (CUT)

The System that is tested to check for fault is determined as CUT. It is the system that is to be checked for any faults during its working.

2.7 Signature Analysis

It is a compression technique based on the concept of redundancy checking. The fault and fault free circuits produce different signatures. The outputs from CUT should be compared with our actual sequence to have a good fault free circuit.

2.8 MISR (Multiple Input Signature Register)

From Fig.4 Multiple input Signature register (MISR) is used to test our circuit and it decrease the hardware required to compress a bit stream, it is used in alternative to the to the LFSR for response compaction because it compress the outputs into single LFSR, it functions due to the LFSR is linear and obeys the super position principle and the overall remainder is Xor sum of remainders of polynomial divisions of each primary outputs of the characteristic polynomial.

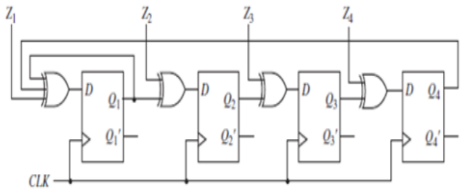


Fig 4: Standard MISR Representation

3. BUILT IN LOGIC BLOCK OBSERVER (BILBO)

From Fig.5 BILBO (built in logic block observer) consists of flip flops with the additional gates. A BILBO is one of the most significant techniques for self-testing of digital IC's; it works on grouping the storage elements of the circuit in the two registers. It can work as both test pattern generation (TPG) and response compactor (RC).

From Table.1 it has four modes of operation with each of its mode operating as independent registers

1) FLIP FLOP (PIPO REGISTER)
   Independent flips flop generally D-FLIP FLOP
2) LFSR pattern generator
   Generates pseudo random test patterns
3) LFSR response compactor
   Analyzer of Multiple input signatures
4) Shift register (scan mode)

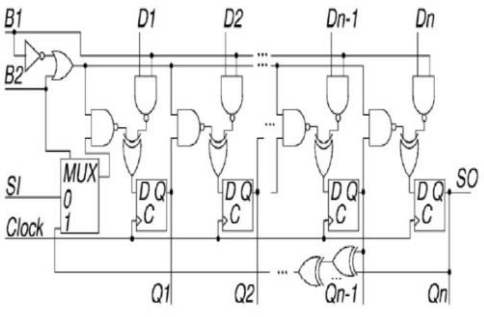


Fig 5: General BILBO Architecture

Table 1: BILBO Modes

Q1	Q2	MODE
0	0	Serial Scan Mode
0	1	LFSR MODE
1	0	D FLIPFLOP MODE
1	1	MISR MODE

4. Ripple Carry Adder

The basic Arithmetic operations like addition, subtraction, multiplication, division can be implemented using AND, OR, NOR, NAND gates etc. Multiplication can be done by repetitive addition, division by repetitive subtraction so if we implement addition it is easy to perform the multiplication and division.

From fig.6 each adder has the input Cin which is the carryout of the previous adder. This kind of adder is called as Ripple Carry Adder, where each bit ripples to the next full adder. The first full adder may be replaced by a half adder. Carry in will be zero for the first full adder. In this project Ripple Carry Adder is used as Circuit under test. Sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Hence the propagation delay occurs inside the logic. Propagation delay is the time elapsed between the application of input and the occurrence of the output. A, B, Cin are the inputs of the logic circuit and the resultant outputs are sum (S) and carry.

The Boolean expression for sum

$$A \oplus B \oplus Cin \quad (1)$$

The Boolean expression for carry

$$AB + (A \oplus B)\, C \quad (2)$$

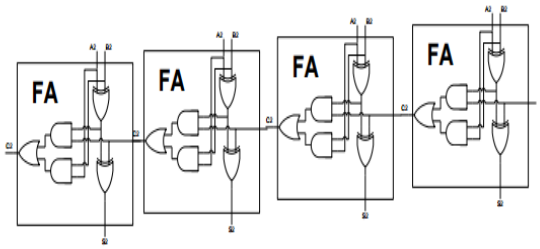


Fig 6: RIPPLE CARRY ADDER

5. Experimental Investigation

VERILOG is a hardware descriptive language which is used to model digital electronic systems; it is mostly used in verification and design of digital circuits at RTL level. Because of this abstraction we can easily simulate analog circuits, mixed signal circuits and also generic circuits.

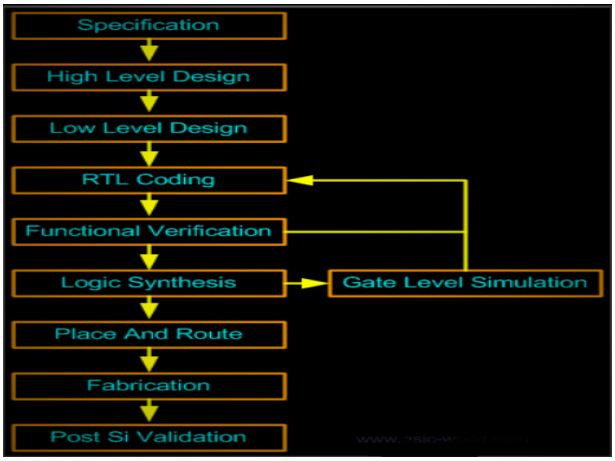


Fig 7: Verilog Design Flow

5.1 verilog Modeling:

1) DATA FLOW MODELING**:** Data Flow Model signifies the moment of data between input/output in a register its operation is based on concurrent execution.
2) STRUCTURAL MODELING**:** It shows graphical representation of components, it is a net-list language; it also works in a concurrent execution.
3)BEHAVIOURAL MODELING**:** It shows a performance of a system for present input values, in this model we design circuit to get desired output for corresponding inputs and it works in sequential execution.

5.2 XILINX ISE

Xilinx ISE is tools used to implement the HDL designs, compile, to perform timing analysis, power estimation and place & routing. Xilinx is primarily used for compiling and designing while ISIM is used for system level testing. The components of Xilinx ISE are
1) EDK (Embedded Development Kit)
2) SDK (Software Development Kit)
3) Chip Scope pro
4) ISIM

6. Results

Bilbo configured in Register mode



Fig 8: BILBO IN REGISTER MODE

Fig 8 shows the operation of BILBO in register mode. In register mode we will get input from another source and return the same value, it is similar to D-Flip Flop

Bilbo configured in LFSR mode

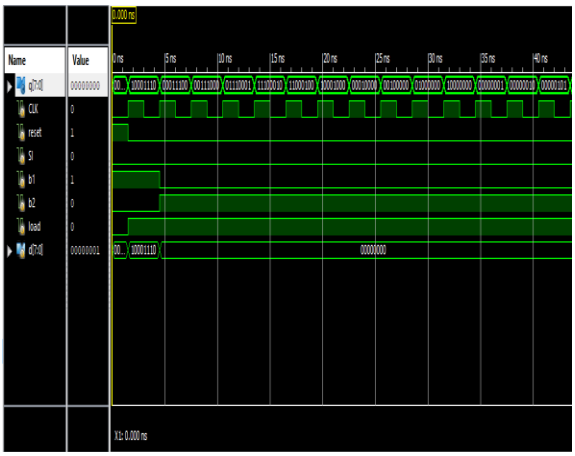


Fig 9: BILBO in LFSR Mode

Fig 9 shows the operation of BILBO in LFSR mode. In LFSR mode initially the BILBO is in register mode. Load the seed value so that BILBO is configured in LFSR mode. The mode can be changed by changing the 'bo' and 'b1' inputs. From Figure 9 we can see that in spite of not giving any input we are getting output from 'q'.

Bilbo configured in MISR mode

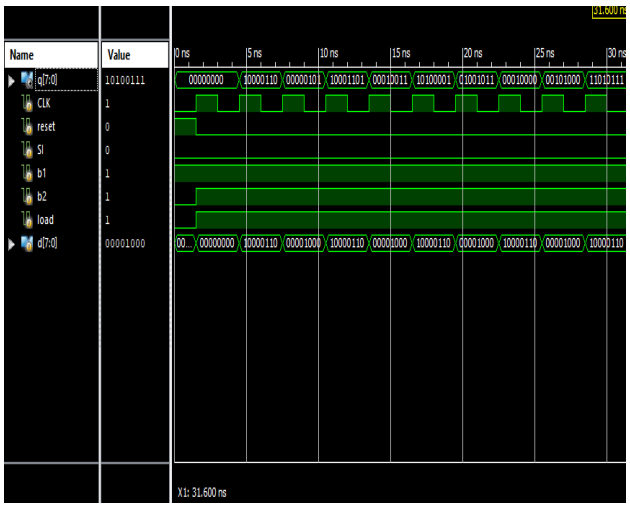


Fig 10: BILBO in MISR mode

Fig 10 shows operation of BILBO in MISR mode. This mode can be configured by changing the 'bo' and 'b1' bits. The 1st seed value of MISR should be zeros then only it can generate signature. We will give LFSR generated output to CUT and the outputs from CUT is given as input to MISR

BIST simulation result

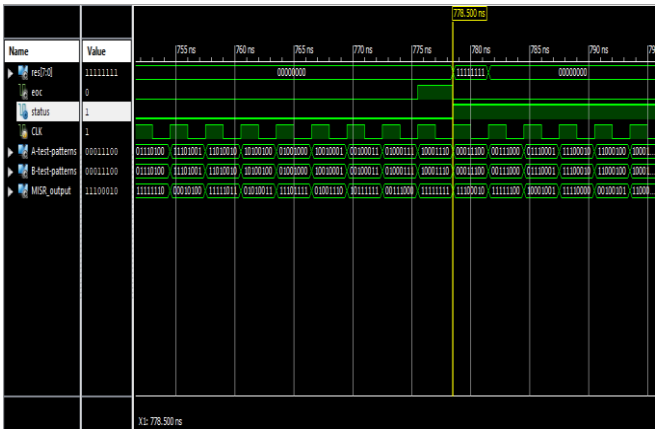


Fig 11: BIST Simulation Result

From Fig 11 we can see that test patters are generated by two 8-bit LFSR and the outputs of LFSR -A and LFSR-B are given as input to 8- ripple carry adder and the outputs of ripple carry adder is given as input of MISR. 'Eoc' indicates the end of one cycle of test patterns and at end of 'Eoc' we will get MISR output from 'res' and that output is signature of that circuit and it is compared with golden signature if it matches the. 'Status' will be one or it will be zero by seeing that we can say our circuit is fault free or faulty circuit

7. Conclusion

We have implemented BIST Architecture as shown in fig using BILBO as a LFSR and MISR. So, we have generated Pseudo random test patterns using 8-bit LFSR and fed that inputs to the circuit under test. We have considered Ripple Carry Adder as a circuit under test and its outputs is given as an input to BILBO which is configured in MISR mode. At first, we have simulated circuit under test without any faults and stored that signature value in the ROM. Then after we have introduced struck-at 0 faults and struck-at 1 fault to the circuit under test (CUT). Then we compared the signature of fault circuit with golden signature and we have observed that signature has changed for faulty circuits then it concludes that using Built in self-test(BIST) architecture we can detect faults automatically with using less resource

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