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***Research Paper***

# Design of Squarer Circuit in Sub-threshold Mode

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**Abstract**

Historically, analog designs have been assumed as a voltage mode based signal processing. However, the necessity of high speed circuits operating at reduced supply voltage has lead to a development of new circuit topology referred as current-mode designs. For low power low voltage designs the applications using translinear principle based circuits has become an area of research and interest. It has wide application in nonlinear signal processing and to build basic active elements. Mode of MOS transistor used in analog circuit realization of is important parameter deciding the performance of the circuit. In this paper, a squarer circuit is proposed based on sub threshold-mode MOS transistors exhibiting the exponential current-voltage characteristic. The simulations have been performed on model files of TSMC 0.18 micrometer technology with the help of ELDO Simulator.

***Keywords***: *Sub Threshold Region, Weak Inversion, Translinear Principle, Squarer Circuit; MOS.*

## 1. Introduction

Device scaling has been the latest trend being followed in VLSI for high speed and high packing density. Scaling of channel length has facilitated the sub micrometer devices to be fabricated on single IC. Few portable devices in medical electronics working on battery like ABCI, insulin pumps; hearing aids etc requires designs in submicron so as to work with reduced power supply. The main goal of any design by designers is to have circuits which should dissipate low power and this has now become a major concern when the application is concerned with biomedical. It is highly desirable as these devices monitors the patient whole day. Various alternatives had been proposed for reducing power consumption while retaining the other performance parameters.

The working of translinear was first introduced by Barry Gilbert which changed the design approach of circuit theory [1]. This translinear principle uses the law of energy conservation (i.e. KVL) across a closed loop. Translinear circuit interpretation came into existence from the concept that the trans conductance is linearly dependent to the collector current in case of bipolar transistors. Alternatively, it means a device whose output current and trans conductance are linearly dependent to each other. In a MOS transistor under sub threshold mode the drain current is an exponential function of the controlling voltage which show a diode behavior and so these circuits is said to obey the translinear principle. The advantage of these current mode approaches makes the complex non-linear mathematical functions easily realizable which is not possible with the standard analog blocks [2, 3] even though they have good linearity. Mostly reported work based on translinear principle is limited to BJT transistors but precision and speed lacks in the designs. In translinear circuits the temperature variation sensitivity is negligible which is an interesting property. The BJT based translinear circuit's work better for low frequency applications. However, nowadays researcher has focused since few years, in synthesis of analog VLSI for sensory information processing systems [4, 5] which employ MOS transistors working in sub threshold region [6, 7].

MOS transistor should operate in sub threshold region so that translinear behavior can be exploited [8-11]. Under sub threshold region, the current-voltage is given by

$$I_{DS} = I_o e^{(kV_G - V_S)/V_T} \quad (1)$$

$$g_m = \frac{d}{dV_G} I_{DS} = \frac{k}{V_T} I_{DS} \quad (2)$$

In this paper, a squarer circuit based on current-mode MOS transistor working on translinear principle is proposed. MOS transistors used for designing the circuit operated in weak inversion region. The work done in this paper is presented in four sections. In section 2, the working of proposed squarer circuit which follows the translinear principle is discussed followed by design on squarer circuit. Section 3 presents the results obtained after simulation of the proposed circuit and section 4 concludes the paper.

## 2. Proposed Squarer Circuit & Translinear Principle

In a translinear circuit, the first step is to design a loop which should have equal number of clockwise and counter clockwise polarities by using forward biased junctions in even multiple. For example a translinear loop is shown in Figure 1.

According to translinear principle, the product of clockwise direction based current densities must be equal to the product of counter-clockwise direction based current densities.

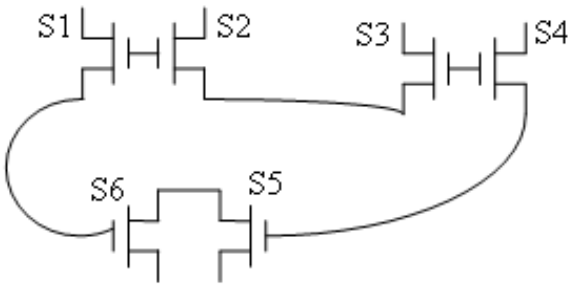


**Fig. 1.** MOSFET based translinear loop

In BJT, the translinear principle is given by

$$\prod_{j\in cw}\frac{I_j}{A_j}=\prod_{j\in ccw}\frac{I_j}{A_j} \tag{3}$$

where CW & CCW denotes the set of indexes of clockwise junctions and counterclockwise junctions respectively. $I_j$ is the output current and $A_j$ is the emitter junction area of $j^{th}$ transistor. In [12], a translinear principle for MOS transistor has been introduced which is referred in literature as "voltage mode translinear principle". MOS transistors loops working in sub threshold region are because of the principle. It takes the form of

$$\sum_{j\in cw}\sqrt{\frac{I_j}{S_j}}=\sum_{j\in ccw}\sqrt{\frac{I_j}{S_j}} \tag{4}$$

where $S_j$ $j^{th}$ MOS transistor is the strength ratio (W/L ratio). In weak inversion mode, there is an exponential I-V characteristic exhibited by the MOS transistors showing a translinear device property as it was originally intended by Gilbert [13]. Compared to BJT, the MOS based translinear circuit can be constructed with lesser number of transistors [14]. In [15], for all levels of inversion, a generalized translinear principle was reported. This principle takes the form of

$$\prod_{j\in cw}^{N}\left(e^{\sqrt{I_j/S_jI_s}}-1\right)=\prod_{j\in ccw}^{N}\left(e^{\sqrt{I_j/S_jI_s}}-1\right) \tag{5}$$

where $I_S$ & $S_j$ are the specific current and aspect ratio respectively of $j^{th}$ MOS transistor. The $I_S$ is given by

$$I_S=2\mu_0C_{ox}\frac{V_t^2}{k} \tag{6}$$

In sub threshold-mode based MOS transistor, $I_j<<S_jI_s$ the expression after the expansion of exponential term above gives:

$$\prod_{j\in cw}^{j\in N}\left(1+\sqrt{\frac{I_j}{S_jI_s}}-1\right)=\prod_{j\in ccw}^{j\in N}\left(1+\sqrt{\frac{I_j}{S_jI_s}}-1\right) \tag{7}$$

$$\prod_{j\in cw}^{j\in N}\sqrt{\frac{I_j}{S_jI_s}}=\prod_{j\in ccw}^{j\in N}\sqrt{\frac{I_j}{S_jI_s}} \tag{8}$$

Assuming circuit consisting of identical MOS transistor having same specific currents. From (6)

$$\prod_{j\in cw}^{j\in N}\sqrt{\frac{I_j}{S_j}}=\prod_{j\in ccw}^{j\in N}\sqrt{\frac{I_j}{S_j}} \tag{9}$$

$$\prod_{j\in cw}^{j\in N}\frac{I_j}{S_j}=\prod_{j\in ccw}^{j\in N}\frac{I_j}{S_j} \tag{10}$$

The relation (10) behaves as per Gilbert proposed in [1].

The circuit performing squaring function is shown in Figure 2. The four P-type MOSFET used $M_1, M_2, M_3$ and $M_4$ forms the translinear loop while the transistors $M_5-M_8$ is a cascode current mirror circuit so as to replicate the exact current. Each of the P-type MOSFET $(M_1-M_4)$ of translinear loop is operating in sub threshold mode. $I_{in}$ & $I_{out}$ are the input current and the output current respectively whereas the reference current is denoted by $I_{ref}$ .

$$\frac{I_3}{S_3}\times\frac{I_4}{S_4}=\frac{I_1}{S_1}\times\frac{I_2}{S_2} \tag{11}$$

Assume each MOS transistor of translinear loop to have same ratio, i.e. $S_1=S_2=S_3=S_4$ , the (11) reduces to

$$I_3\times I_4=I_1\times I_2 \tag{12}$$

For squarer circuit, $I_1=I_2=I_{in}$ $I_3=I_{ref}$ and $I_4=I_{out}$

Using (9)

$$I_{ref}\times I_{out}=I_{in}\times I_{in} \tag{13}$$

Hence

$$I_{out}=\frac{I_{in}^2}{I_{ref}} \tag{14}$$

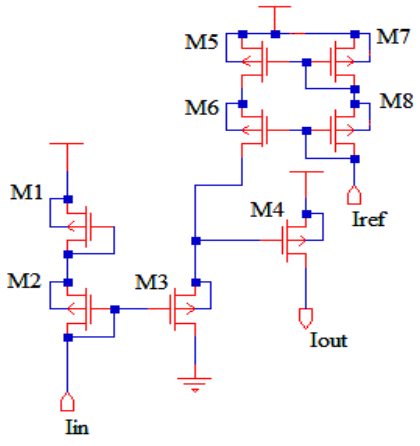


**Fig. 2.** Proposed Squarer circuit.

## 3. Simulation Results

The current-mode squarer circuit proposed in this paper is designed using transistor models of TSMC 0.18 micrometer technology. The MOS transistor dimensions used for designing the proposed circuit is shown in Table 1. In proposed squarer circuit, the input current $I_{ref}$ is taken as a DC current which is 1nA whereas the input current $I_{in}$ is taken as triangular wave current of amplitude 10nA. The plot of output current $I_{out}$ is shown in Figure 3. As observed from simulation results when matched to theoretical calculation $I_{theoritical}$ showed almost similar response.

**Table 1** Transistors Width and Length of Squarer circuit.

| MOSFET | Width (nm) | Length (nm) |
|---|---|---|
| M1 | 3500 | 350 |
| M2 | 3500 | 350 |
| M3 | 3500 | 350 |
| M4 | 3500 | 350 |
| M5 | 36000 | 3600 |
| M6 | 36000 | 3600 |
| M7 | 36000 | 3600 |
| M8 | 36000 | 3600 |

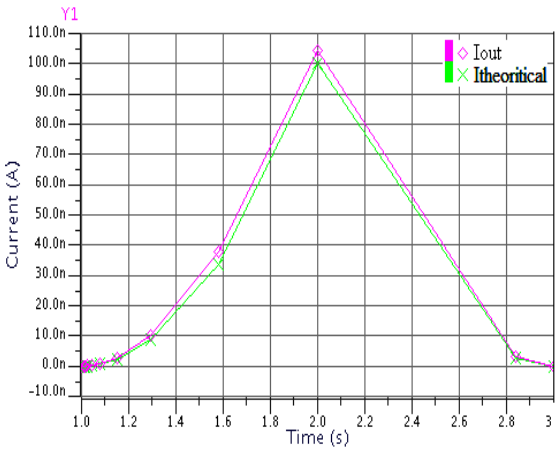


**Fig. 3.** Simulation of squarer circuit for Iin= 10nA, Iref= 1nA.

## 4. Conclusion

This paper proposed a MOS transistor based squarer circuit which follows the translinear principle working in sub threshold region. The advantage of using MOS transistor lies in terms of accuracy which has not been possible with BJT based designs. The application of proposed circuit can be widely found in CMOS based log-domain filters for analysing nonlinear distortion, AGC circuits so that the gain changes linearly with control voltage.

## References

[1] Gilbert, B. (1975). Translinear circuits: A proposed classification. *Electronics letters* 11, 14-16..

[2] Payne, A., & Toumazou, C. (1996, May). Linear transfer function synthesis using non-linear IC components. In IEEE International Symposium on Circuits and Systems ISCAS'96, Vol. 1, pp. 53-56. IEEE.

[3] Mulder, J., Van Der Woerd, A. C., Serdijn, W. A., & Van Roermund, A. H. M. (1996). Current-mode companding/spl radic/x-domain integrator. *Electronics letters* 32, 198-199.

[4] Eskiyerli, M., & Payne, A. (2000). "Square root domain" filter design and performance. *Analog Integrated Circuits and Signal Processing* 22, 231-243.

[5] Mead, C. A., Analog VLSI and Neural Systems. Addison Wesley: Reading, MA, 1989.

[6] Mead, C. (1990). Neuromorphic electronic systems. *Proceedings of the IEEE* 78, 1629-1636.

[7] Vittoz, E., & Fellrath, J. (1977). CMOS analog integrated circuits based on weak inversion operations. *IEEE journal of solid-state circuits* 12, 224-231.

[8] Vittoz, E. A., Micropower techniques, In Y. P. Tsividis and P. Antognetti, eds., VLSI Circuits for Telecommunications, Prentice Hall: 1985.

[9] Andreou, A. G., & Boahen, K. A. (1989). Synthetic neural circuits using current-domain signal representations. *Neural Computation* 1, 489-501.

[10] Andreon, A. G. (1990), Synthetic neural systems using current-mode circuits, in Proceedings of the IEEE International Symposium on Circuits and Systems, New Orleans, pp. 2428-2432.

[11] Andreou, A. G. (1995). Low power analog VLSI systems for sensory information processing. IEEE ISCAS-95 Tutorial Book on Multimedia Communications.

[12] Boahen, K. A. (1996), Retinomorphic vision systems, in proc. Of MicroNeuro-96, IEEE Computer Society Press: Los Alamitos, CA.

[13] Seevinck, E., & Wiegerink, R. J. (1991). Generalized translinear circuit principle. *IEEE Journal of Solid-State Circuits* 26, 1098-1102.

[14] Vittoz, E., & Fellrath, J. (1977). CMOS analog integrated circuits based on weak inversion operations. *IEEE Journal of Solid-State Circuits* 12, 224-231.

[15] Minch, B. A. (2008). MOS translinear principle for all inversion levels. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 55, 121-125.

[16] Thakral B. (2015), Design of Low Power Current Mode Square-Root Circuit. *International Journal of Engineering and Manufacturing* 4, pp. 23-29.