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Research Paper

Development of Framer/Deframer for 5Gbps JESD204B Soft IP

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Abstract

This paper aimed to modify and redesign theJESD204B Full System of Lattice Semiconductor, particularly the TX deframer and RX framer modules used for the 3Gbps JESD204B soft IP to support the recently released 5Gbps JESD204B Soft IP. The modified full system instantiating the new 5Gbps JESD204B Soft IP had to be tested for functionality through RTL and gate simulation and tested for timing through Static Timing Analysis.

The transaction layer's RX framer, TX deframer, and the clock generator modules were identified to be the major blocks of the full system affected by the change in the soft IP. These were redesigned, followed by RTL and gate simulation of the full system. STA was checked through the Lattice Diamond tool. The system passed the simulation tests. Also, STA results showed that timing was still relaxed even if the lane speed was increased, ensuring that timing requirements are achieved by the device. It is recommended that the full system's other blocks, and the testbench for the JESD204B and other soft IP products be investigated to operate at a higher clock frequency without violating the timing requirements and constraints of the ECP5 device.

Keywords: *JESD204B, Soft IP, FPGA, Lattice Semiconductor, RTL, converter*

1. Introduction

In response to the need for a fast and reliable interface between the ADC/DAC converters and the FPGA (which performs the DSP function), the JEDEC Solid State Technology Association standard "JESD204" was released in 2006. This is a serialized interface using a 3.125-Gb/s link rate, and introduces coding and framing, which removes the need for a separate data clock. The latest version of JESD204 standard is JESD204B.01, which was released in 2012. [1] This latest version of the standard provides support for deterministic latency, allowing multiple converters to be phase coherent and synchronized. Also, the maximum speed which the standard supports increased to 12.5Gbps. [2]

Before JESD204B, there were already several published and implemented designs [3] - [11] to interface a converter with an ASIC or FPGA chip. For instance, in the paper of Mahat et. al, [4], the ADC interface consists of a serial to parallel converter block and asynchronous FIFOs. The serial to parallel converter was used to pack serial bits received from quad AD9219 ADC [12] which requires an LVPECL-/CMOS- /LVDS-compatible sample rate clock, into 10-bit data. The packed data are then pushed into asynchronous FIFOs for data buffering. It presented an interface design between a multi-channel ADC and high speed DSP processor for system-on-chip design.

Another is the design of an interface between high speed dual data rate ADCs to programmable logic device which was described in the paper of Tiwari, [6]. FPGA was used to collect data from 8 bit pairs of LVDS compatible ADC channels clocked with Dual Data rate at 200 MSPS. VHDL was used as the hardware description language to describe the logic inside the FPGA.

Although interfaces using LVDS [13]- [15] allowed for a faster transfer of data and has comparable speed to JESD204B, the maximum speed of JESD204 still exceeds that of the LVDS. The drawback with using LVDS is that, as the number of ADC channels increases the pin count also significantly increases, which is not the case for JESD204B. [16]

The recently released configurable 5G JESD204B Soft IP package of Lattice Semiconductor Corporation is an improvement in terms of speed from its previous 3G JESD204B Soft IP. [17] This had a corresponding Sapphire JESD204B Full System for pre-silicon validation of the soft IP in Lattice Sapphire-85H devices. This paper intends to develop a JESD204B Full System for the 5G JESD204B Soft IP.

A working 5G JESD Full System ensures that the 5G JESD Soft IP is thoroughly tested and compatible to the needs of the users of the JESD Soft IP by providing a working full system design. This study focuses mainly on the design of the 5G JESD204B Full System particularly the transaction layer modules like the RX framer and TX deframer modules, its simulation in RTL and gate level, and test timing through static timing analysis (STA).

2. Lattice JESD204B Full System

The JESD204B Full System presents a working implementation of the JESD204B Soft IP by providing the transaction layer modules, and together with the SVP (System Validation Platform), allows verification of the functionality and timing behavior of the JESD soft IP which is released to customers.

Previously, the JESD204B Full System supported the JESD Soft IP of lane speed in 3.125 Gbps. This had a data width (input

and output data of the soft IP) of 16 bits per lane. Now Lattice just released a JESD204B Soft IP which can support channel rates of up to 5Gbps, having a data width of 32 bits in the interface. In response to this, a JESD204B Full System which can support the increased speed of the soft IP must also be designed.

Shown in Figure 1 is the 3G JESD204B Full System instantiating the JESD204B Soft IP. It provides the transaction layer of the JESD204B standard, which connects to the RTL SVP components for testing of the full system during simulation or for connecting the full system to the pc during actual hardware testing. [18]

3. Methodology

This section discusses the processes involved in the design and verification of the 5G JESD Full System shown in Figure 2 is the simple flow diagram in implementing the 5G JESD Full System. First, the changes made in the 3G JESD Soft IP to support the 5Gbps lane speed are identified, and then from this the modifications to be made in the full system to support the 5G JESD Soft IP are determined. Next is the design of the 5G JESD Full System and RTL coding. The resulting modules are tested through RTL simulation. When the tests pass RTL simulation, Lattice Diamond tool [19] is then used to synthesize, translate, map, and perform place and route for the JESD Full System module including the SVP modules. Then, the Verilog netlist is exported to be used for GLS simulation. After both the RTL and GLS simulations are finished, Diamond tool is used again to verify the timing behavior of the JESD Full System using the preference file containing the timing constraints of the JESD Full System. If any of the RTL/GLS simulation or STA analysis fail, the design is rechecked, given the assumption that the testbench and the preference files have no errors. Results are then compared for the 3G and 5G JESD Full Systems.

3.1 Changes in the JESD204B Soft IP

Changes in the soft IP include the FPGA device used, the clock frequencies, and bus width of data and boundary flags. From ECP5UM, the device used was changed to ECP5UM-5G [20], which is capable of serializer/deserializer (SerDes) speed up to 5Gbps per lane. The device (devclk) and SerDes reference (refclk) clocks were modified as listed in Table I. SerDes refclk was increased to 250MHz. The device clock decreased from 156.25MHz to 125MHz, but this is acceptable since the bus width is increased from 16bits to 32bits at a 5Gbps lane speed.

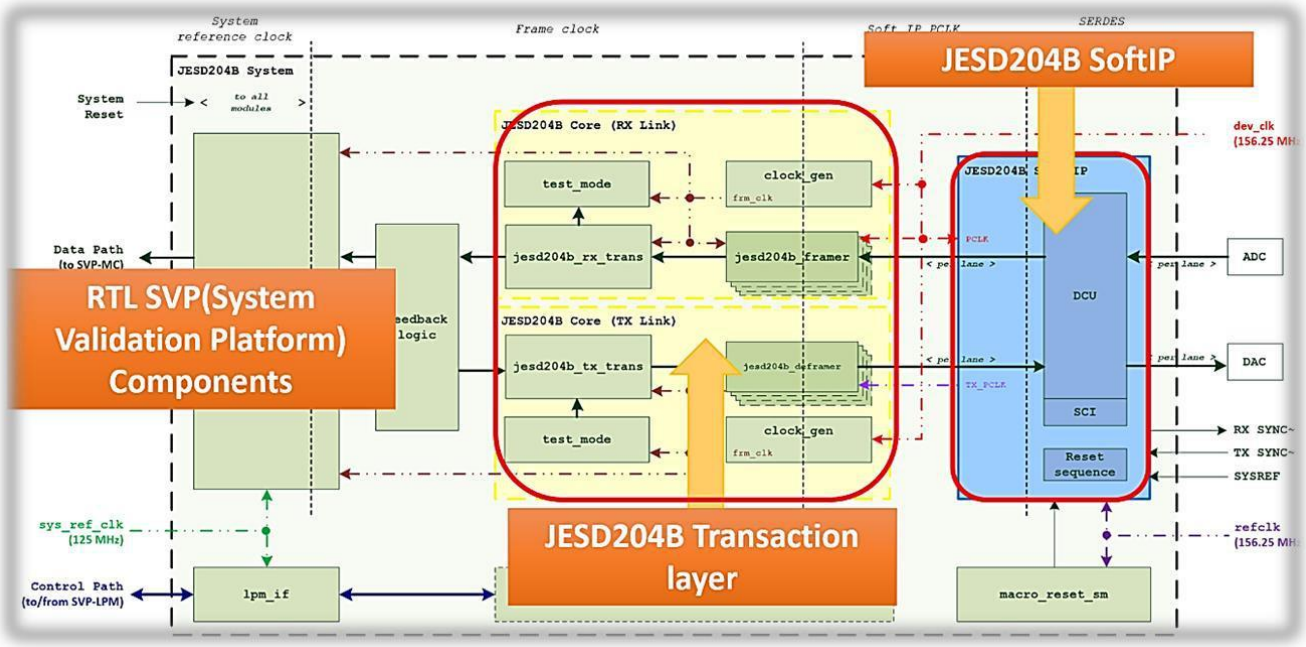

Fig. 1. Block diagram of the JESD204B Full System. [18]

Frame clock depends on the parameter F. The formulas for the frame clock are

For 3G:

$f_{frm\_clk} 2 * f_{pclk} / F$ (MHz) where F number of octets per frame

$f_{pclk} f_{dev\_clk} 156.25MHz$ (1)

For 5G:

$f_{frm\_clk} 4 * f_{pclk} / F$ (MHz) where F number of octets per frame

$f_{pclk} f_{dev\_clk} 125MHz$ (2)

Since the data bus width doubled in size, new boundary flags were also added.

Table 1. Clocks in the JESD204B Full System

	3G Full System	5G Full System
Devclk	156.25 MHz	125MHz
SerDes Refclk	156.25 MHz	250MHz
Data bus width	16 bits	32 bits
Frame Clock		
at F =2	156.25 MHz	N/A
at F =3	104.1667 MHz	N/A
at F =4	78.125 MHz	125 MHz
at F =5	62.5 MHz	100 MHz
at F =6	52.0833 MHz	83.333 MHz
at F =7	44.6429 MHz	71.429 MHz
at F =8	39.0625 MHz	62.5 MHz

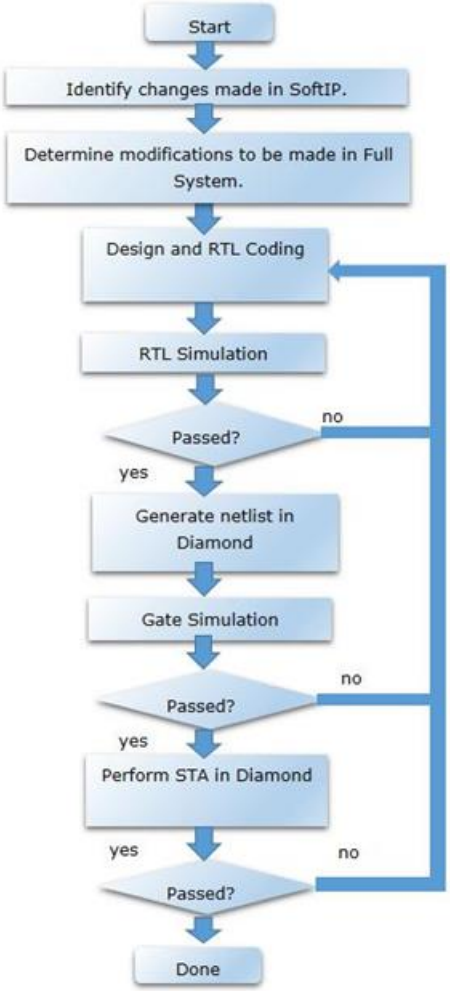

Fig. 2. Flow diagram in implementing the 5G full system.

3.2 Modifications in the Full System

The 3G JESD204B Full System used the soft IP package but this full system for 5G would use the RTL source code instead of the package. For the changes in the Full System, Figure 3 shows modules with red and purple boxes. The red boxes were the modules modified for the 5G JESD Full System. These are the RX framer, TX deframer, and the clock generator modules. Those with purple rectangles also have modifications but not on the logic of design.

These are the only modules which need modification since they are affected by the changes in the soft IP. For the RX framer and TX deframer, they are affected by the device data bus width and the boundary flags while the clock gen modules are affected by the change in frame clock frequencies. For the purple rectangles, these are the modules affected by the use of the JESD Soft IP RTL source code instead of using the JESD soft IP package.

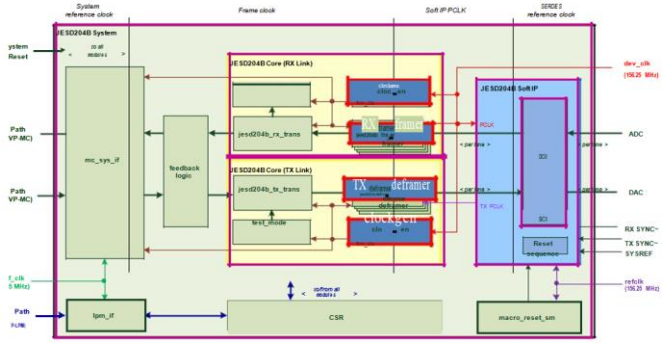

Fig. 3. JESD Full System modifications.

3.2.1 Redesign of the RX framer module

The RX framer module within the JESD204B transaction layer, transfers data from the device clock domain to the frame clock domain. It converts the data from the soft IP into frames of the transaction layer.

From the previous implementation of the framer module, two whole frames were formed and saved in the Distributed Dual Port RAM (DPRAM) hard IP [21] generated in Diamond Tool's Clarity Designer. The previous and new DPRAM modules' block diagram are shown in Figure 4. Instead of 2 frames, the new DPRAM module's input are 4 frames (maximum F*8*4 = 8*8*4=256bits for 5G). This is because input data of framer is now 32bits where to form the right frames, 4 frames are saved at a time.

Low or high byte of data is considered through the boundary flags. Then four whole frames are formed as input to the DPRAM. Write is enabled and write address is incremented every after 4 whole frames saved in the DPRAM. Reading is then enabled in the DPRAM every frame clock cycle, after enough delay is attained when 4 multiframes have been received during initial lane alignment sequence (ILAS—a FSM state in JESD204B, before data state), signifying start of data. Read address is incremented every 4 frames. The output frame is taken from the DPRAM.

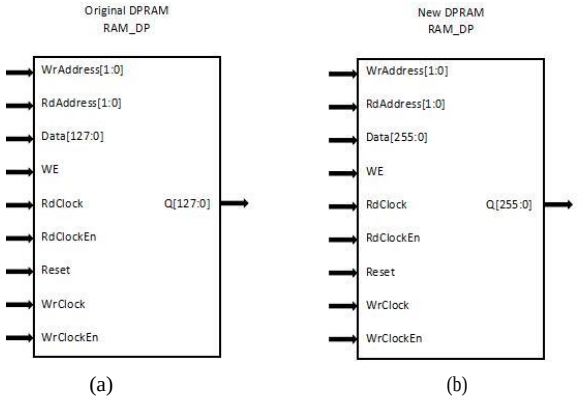

Fig. 4. DPRAM modules for (a) 3Gbps and (b) 5Gbps RX framer

3.2.2 Redesign of the TX deframer module

The TX DUT's deframer module is used to convert the frames into group of octets, which becomes the input of the JESD soft IP. For the 3G Full system, received frames are grouped into 2 before being written into a DPRAM module. In 5G JESD Full System, 4 frames every write cycle are written into the DPRAM module. The 3G and 5G DPRAM modules of the deframer are shown in Figure 5 below.

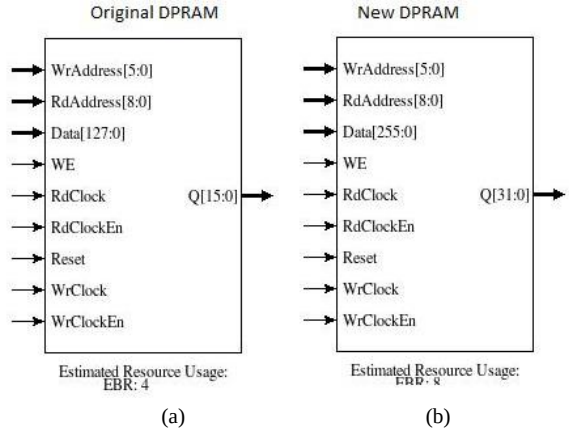

Fig. 5. Deframer DPRAM module for (a) 3Gbps and (b) 5Gbps JESD Full System

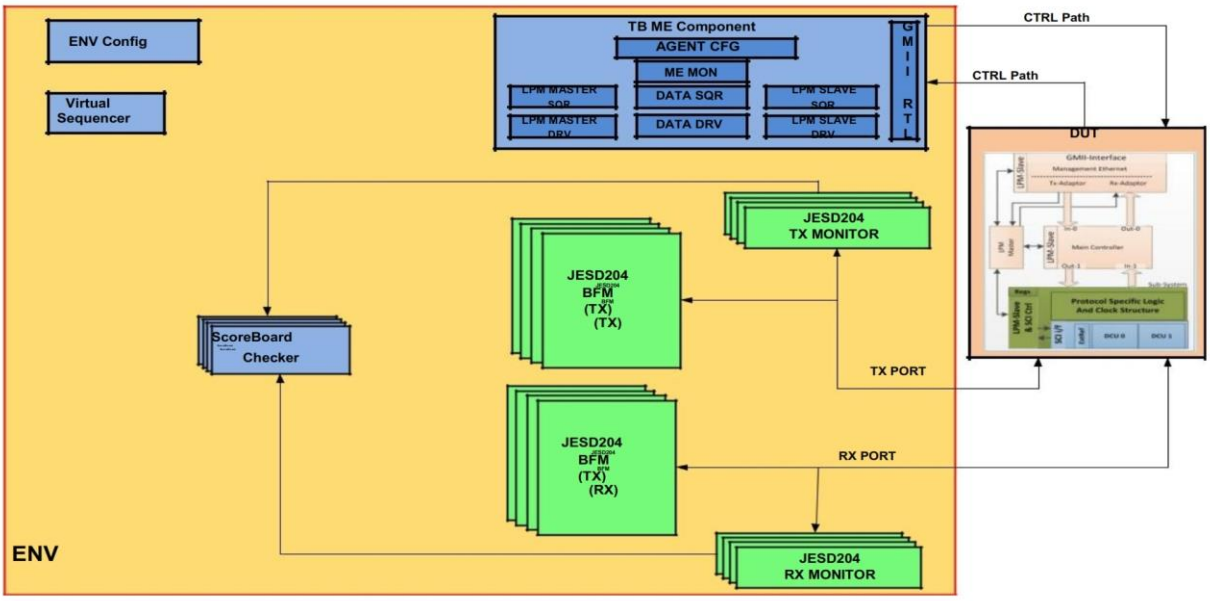

Fig. 6. JESD204B Full System Testbench Architecture Diagram. [22]

Table 2. RTL AND GLS SIMULATION TESTS.

Script File	JESD Configuration	Test1
rtl_rx_short.csh	RX CFG1	rx_short_pattern_test
rtl_tx_cfg2.csh	TX CFG1	tx_short_pattern_test
		tx_long_pattern_test
rtl_ext.csh	RXTX CFG1	board_to_board_test
		bidir_throughput_ext_test
		reset_on_ext_loopback_test
rtl_rx_cfg1.csh	RX CFG2	rx_long_pattern_test
		rx_tmderr_test
		rx_disparity_err_test
		rx_not_in_table_err_test
		rx_ucc_err_test
		cm_err_test
		rx_ms_err_test
		reset_on_rx_txn_test
		rx_reinit_test
		rx_k_reassert_test
Script File	**JESD Configuration**	**Test 2**
rtl_lb.csh	RXTX CFG1	transport_loopback_test
		mc_sys_loopback_test
		tx_constant_tail_bits_test
		tx_random_tail_bits_test
		tx_idle_mode_test
		reset_on_tx_txn_test
		tx_reinit_test
		tx_sync_reassert_test
		core_noise_test
		register_test
		dcu_register_test
		dcu_register_memory_test
rtl_rx_cfg1_mult.csh	RXRX CFG1	multiple_rx_test
		multiple_rx_sync_combine_test
rtl_tx_cfg2_mult.csh	TXTX CFG1	multiple_tx_test
		multiple_tx_sync_combine_test

3.3 STA Analysis

STA simulation for the JESD Full System was performed using the logic preference file where the frequencies of the clocks are declared or constrained, and the false paths and clock-domain crossing are blocked to prevent the tool from calculating the delays of these paths that might cause false timing violations, since these signals are already synchronized.
For the 5G constraints, the clock frequencies are modified, with the signal names adapted to the changes in the full system. The constraints of other unchanged modules are also the same, like the ME (Management Ethernet module).

4. Results

This section discusses the results obtained during RTL and gate simulation. Also, it shows the STA summary and area utilization of the full system.

4.1 RTL and Gate Simulation

RTL simulation was performed using the following default JESD204B parameter values: F is 4 (octets per frame), K is 9 (frames per multiframe) and M equals 2 (number of converters). All 128 tests passed for RTL simulation.
To test at different values of F, RX and TX long pattern tests, which are the basic tests, were iterated for values of F from 4 to 8 at default K. Later, these were tested for K equal to 3 to 32 based from the 3G Full system's range of K values. At default F of 4, TX and RX long pattern test passed for K values from 5 to 32.
For the gate simulation, test settings are the same as that of the RTL simulation. All 128 tests passed for GLS simulation. Input and output of the deframer module for default parameter values is shown in Figures 7 and 8, respectively. This is for the basic test for TX, which is the TX long pattern test. For F equal to 4, the 32bit data is simply swapped since 32bits is exactly 4 octets which equates to 1 frame.

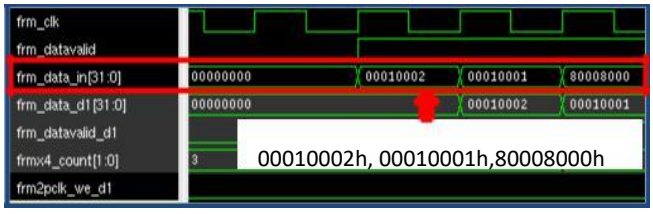

Fig. 7. TX deframer input for F=4.

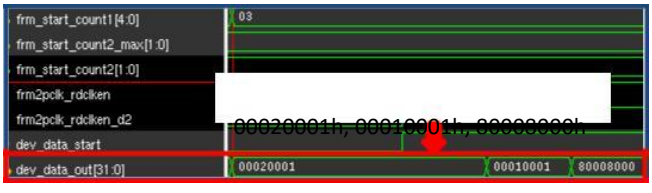

Figure 8. TX deframer output for F=4.

Range of F is from 4 to 8 for 5G. For 3G, F data width is 16bits and F has a range from 2 to 8. This is a design limitation specifically in the part of the RX framer as shown in the piece of Verilog code in the RX framer:

```
`ifdef JESD_5G
if (!rst_n) begin frmx4_data_count
    <=2'd0;
end
else if (mf_start_framer_d2) begin
  if (frmx4_data_count==(NUM_OCTET_PER_FRM-1)) begin //4 oc-
tets in 1 dev_clk
frmx4_data_count <=2'd0;
end
else begin
    frmx4_data_count <= frmx4_data_count +1;end

end
else begin
    frmx4_data_count <=2'd0;end

`else           // 3G
```

Four octets are received every device clock cycle, which has a maximum value of 125MHz when F equals 4. Unless the maximum frame clock frequency is twice that of the device clock, which is 250MHz, the minimum value of F is 4. 250MHz is beyond 200MHz which is the maximum frequency the FPGA logic can handle.

For the RX framer, the input and output data are shown in Figures 9 and 10, respectively.

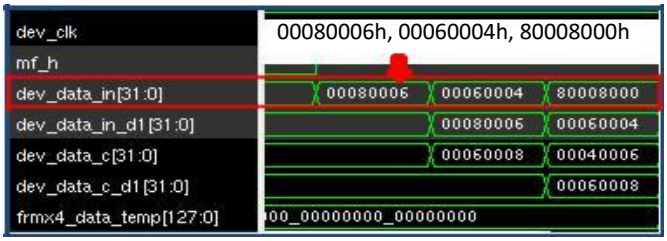

Figure 9. RX framer input for F=4.

Figure 10. RX framer output for F=4.

4.2 STA Results

All preferences were met for the hold and setup time of each implementation in Diamond. Table III gives the report summary of the preference for some signal in one particular RX configuration. There is no direct comparison between the 3G and 5G for these results since they have different constraint values. However, from the table we can say that the timing is relaxed for the previous 3G and the current 5G implementation; actual frequency for example for devclk_c of 5G is 184MHz while constraint is just 125 MHz.

Table 3. Report summary for some preference.

Signal with Preference	Constraint	Actual
3G:		
dev_clk	156.250 MHz	368.189 MHz
dev_clk_c	156.250 MHz	178.190 MHz
Refclk	156.250 MHz	238.777 MHz
frm_clk0_c	156.250 MHz	199.880 MHz
5G:		
dev_clk	125.000 MHz	296.736 MHz
dev_clk_c	**125.000 MHz**	**184.400 MHz**
refclk_l0	250.000 MHz	304.878 MHz
frm_clk0_c	125.000 MHz	179.856 MHz

4.3 Area Results

To get a comparison of device utilization between the 3G and 5G JESD Full System, Table IV summarize the registers and other FPGA resources utilized by the design for 6 implementations. Register utilization for RX is 12% while TX has only 10%. This makes RXRX configuration to have the highest number of registers utilized, which is up to 15%, while RXTX only has 14%.

Area utilization, as expected, increased for 5G. RX has larger area than the TX soft IP and transaction layer modules. This is because more logic is required for RX than TX.

Table 4. Area utilization for selected implementation.

Implementation	FPGA Resources (total)	3G	5G
1. RX CFG2, sc0, scr0	registers (84735)	10343(12%)	11389(13%)
	SLICEs (41820)	8369 (20%)	9280(22%)
	LUT4s (83640)	9924(12%)	11050(13%)
	PIO sites used	81 (22%)	85(23%)
	block RAMs	23(11%)	23(11%)
2. TX CFG1, sc1, scr1	registers	8439(10%)	9260(11%)
	SLICEs	6681(16%)	7560(18%)
	LUT4s	8207(10%)	9362(11%)
	PIO sites used	81(22%)	85(23%)
	block RAMs	23(11%)	31(15%)
3. RXTX CFG1, sc0,scr 1	registers	11544(14%)	13401(16%)
	SLICEs	9431(23%)	11219(27%)
	LUT4s	11336(14%)	13552(16%)
	PIO sites used	77(21%)	81(22%)
	block RAMs	33(16%)	41(20%)
4.RXTX CFG1, sc1, scr0	registers	11544(14%)	13371(16%)
	SLICEs	9388(22%)	10997(26%)
	LUT4s	11373(14%)	13136(16%)
	PIO sites used	77(21%)	81(22%)
	block RAMs	33(16%)	41(20%)
5.RXRX CFG, sc1, scr1	registers	12683(15%)	11755(14%)
	SLICEs	10471(25%)	9590(23%)
	LUT4s	12347(15%)	11446(14%)
	PIO sites used	77(21%)	81(22%)
	block RAMs	27(13%)	23(11%)
6.TXTX CFG, sc1, scr1	registers	9553(11%)	11237(13%)
	SLICEs	7612(18%)	9353(22%)
	LUT4s	9480(11%)	11711(14%)
	PIO sites used	77(21%)	81(22%)
	block RAMs	31(15%)	47(23%)

5. Conclusion

A 5G JESD204B Full System instantiating the 5G Lattice JESD204B Soft IP was successfully implemented and tested, ensuring the functionality and timing behavior of the soft IP. Main modules modified were the TX deframer and RX framer modules. These were redesigned by resizing their DPRAMs, adjusting the read and write timing in the DPRAM, and generalizing an equation for the counter when to start sending and receiving data based on the boundary flags.

Increasing the bus width while retaining the system clock frequency added a restriction to the design's minimum supported parameter values like F (number of octets per frame given that the maximum frame clock is equal to the device clock). For F equal to 2, the minimum supported F is 4 for the 5G JESD Full System.

Recommendations

This project provided 5G support for the JESD204B Full System, and retained the Lattice System Validation Platform (SVP) RTL and most of the testbench components. As a recommendation, the Lattice SVP can be investigated to operate at a much higher speed,

and even backward compatible to the previous designs for validation. The system clock of the SVP components in the full system is 125MHz. The maximum frequency that the ECP5 FPGA devices can handle is in 200MHz. The system clock can be investigated to operate at a much higher frequency without violating the timing requirements of the system and device

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