International Journal of Engineering & Technology, 7 (2.8) (2018) 617-621

SPC

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research Paper

The reordered deblocking filter and SAO architecture for HEVC system

N. Nandhagopal [1*], S. Navaneethan [2], C. Arul Murugan[3]

[1]*Associate Professor, Department of Electronics and Communication Engineering, Excel Engineering College, Tamilnadu, India.*
[2]*Research Scholar, Anna University, Chennai, India.*
[3]*Assistant Professor, Department of Electronics and Telecommunication Engineering, Karpagam College of Engineering, Coimbatore, Tamilnadu, India.*
**Corresponding Author Email:nandhaphd@gmail.com*

Abstract

High Efficiency Video Coding (HEVC) used in broad band and wireless applications employs two in-loop filters to remove the blurring artifacts, blocking artifacts and ringing artifacts. The standard h.264/AVC deblocking filter which requires more memory initially filters the horizontal borders, followed by the vertical borders. The results of vertical borders filtering are utilized in the horizontal filtering process and the obtained results are further stored in temporary memory. The proposed system comprises of a reordering filter to reduce the order of the filter and a SAO to modify the decoded samples to a new offset value inorder to perform robust encryption mechanism. Hence reorder filter reduces the memory needed for this filtering process. In HEVC, SAO is an in-loop filter and located next to deblocking filter. The idea of SAO is to compensate renovated samples by adding an offset to each pixel, so that the distortion between renovated picture and original one can be reduced. Implementation of proposed simulation work is done by Verilog HDL and implemented using Virtex 6 FPGA to compute the power and hardware requirements in terms of LUT and slice registers.

Keywords: *HEVC, SAO, H.264/AV*

I. Introduction

Deblocking filter is the purposeful blocks in H.264/HEVC. Deblocking filter is the major time consuming part in H.264 & HEVC video decoder. The H.264 & HEVC architecture produces blocking artifacts. The main reason behind the happening of blocking artifacts is due to the transform coefficient quantization and block based motion compensation. Therefore, the blocking artifacts are revamped in this article for higher efficiency. In order to lessen blocking artifacts and upgrade compression efficiency, all the video frames are subdivided into macroblocks. Moreover, each macroblocks are further divided into 4x4 pixel blocks where deblocking filters are applied other than the boundary edges of a frame.

In HEVC, several artifacts are removed by imposing double in-loop filters. The deblocking filter (DBF) is applied to the boundaries of renovated block to diminish the blocking artifacts. Besides, the renovated samples from DBF are fed as input to sample adaptive offset (SAO) filter. SAO is helpful to minimize the ringing artifacts, which is contributed by the quantization errors produced due to transform coefficients [1-10]. Control analyses for systems [11-20].

The organization of this work is categorized as follows. In section II, the literature review of the deblocking filter and SAO are discussed. Section III explains proposed work of modified filter order and SAO. Section IV shows the experimental setup and simulation results. Finally, conclusion is arrived in Section V.

2. Literature Review

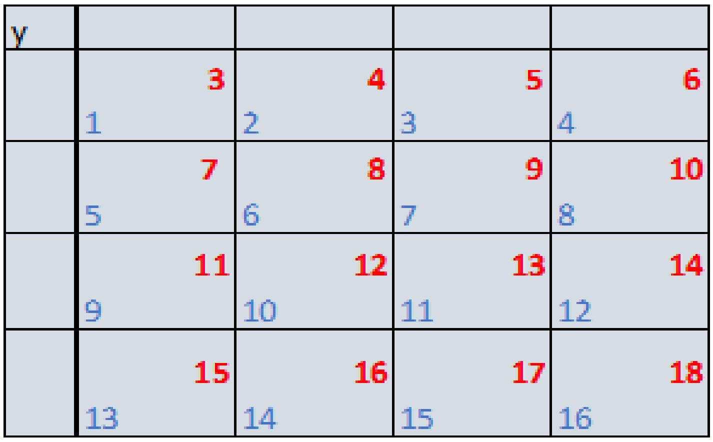
In [1], WMV9 post-processing technique, the flickering artifacts from image to image leads to critical issues. The deringing filter which is applied for decreasing ringing artifacts. The SAO in JCTVC-E049 [2], reduced the encoding latency by local adaptation and sequential stages are collective into one stage by selecting only one classifier per region. Yang Zhang [3] is indicated to restrict edge offset sign to decrease visual artifact caused by edge offset. The number of band offset is weakened to facilitate implementation. A. Norkin [4] has introduced a design especially at block barriers to minimize visible artifacts. In addition, the filters were selected and applied at the code boundaries over the artifacts. The HEVC de-blocking filter has the potential to perform parallel processing with reduced computational complexity to decrease the visual artifacts. M. Esche [5] has presented a Wiener-based in-loop filtering method to reduce the hardware requirements of HEVC. E. Ozcan [6] introduced a first HEVC de-blocking filter hardware. In this hardware, two parallel data paths were used to achieve better performance.

3. Proposed Method

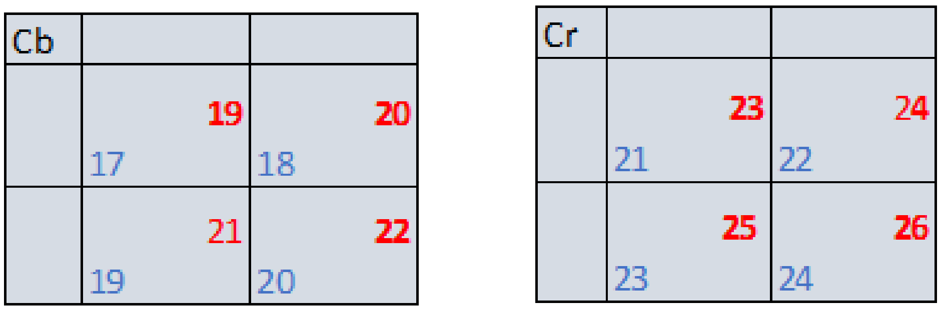
In the H.264/AVC & HEVC, the deblocking filter is applied after the inverse transform in encoder and decoder (before displaying macroblocks). The designed filter softens the block boundary and further enhances the quality of resultant decoded pictures.

A. Reorder filter

The deblocking filter algorithm is utilized as a part of H.264/HEVC standard is more complex. The standard H.264 deblocking filtering order is Modified and implemented in this work. Reformed filtering order is pointed in fig 1. The filtering order looks similar to two vertical edges have been filtered, the horizontal edge and vertical edge can be filtered. All luma pixels have to be filtered before filtering a Chroma pixel. If it takes this in pipeline concept for entering of vertical filter it will allow Chroma pixels while luma pixels are still present in the pipeline. Use of pipeline limits the count of slices and registers needed for constructing the filter. Moreover, by using this filtering order the quantity of memory required for storing filtered 4 * 4 blocks is also reduced.



a) Luma Component



b) Chroma Components

Fig. 1: Reorder filter

B. De-blocking filter Process

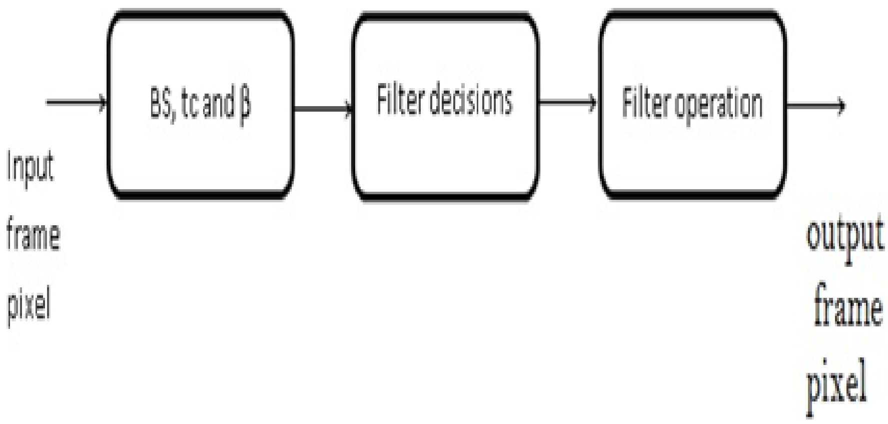


Fig. 2: Deblocking filter

The deblocking filter takes information about the pixels, threshold values and boundary strength that are to be filtered. Filtering decisions are represented by the equations [7]. Before the boundary filtering, it is necessary to decide whether the boundary should be filtered or not and also to determine which filtering modes, either normal or strong, required to be assigned on a boundary. With the assistance of filtering decisions, DF avoids blocking artifacts and it filters only those which are artificially generated by the coding process. Filtering operations are computed by the filtering decisions unit for normal and strong filters.

C. Sampling adaptive offset

SAO often uses two offset sample and their parameters are customized from one region to other region. The HEVC Edge offset (EO) and Band Offset (BO) are two different types of SAO. In EO grouping samples are formed by comparing the current samples with the neighboring samples. Whereas, in BO, a group samples are formed by many different sample values. The Region Size is fixed to one coding tree block (CTB) to minimize the encoding latency and buffer requirement. The side information is reduced further by merging multiple code tree units (CTU) to share SAO parameters.

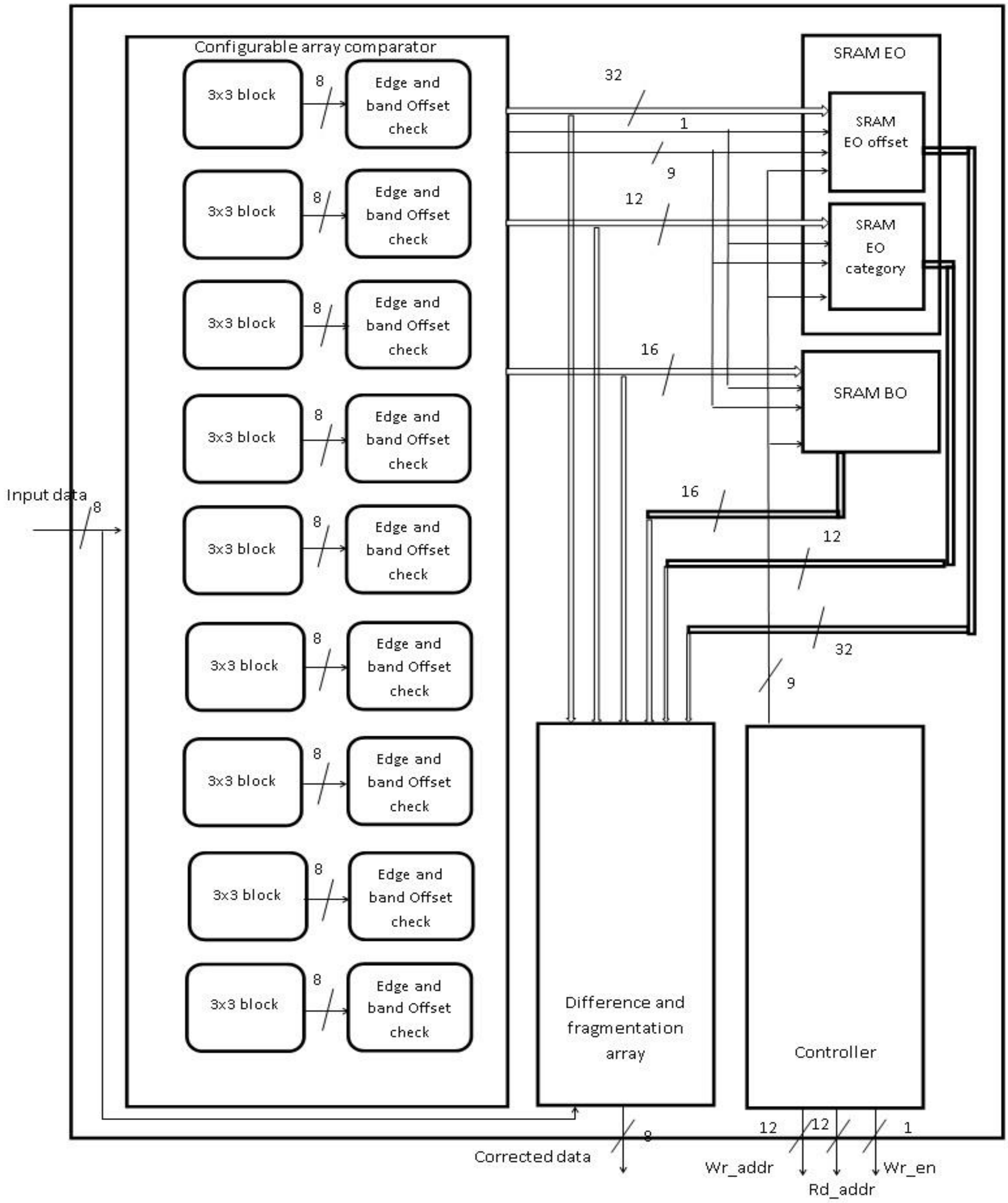


Fig. 3: Architecture of SAO block

4. Experimental Results

The simulation of improved deblocking filter and SAO is carried out using Verilog HDL and tested in Altera - Modelsim 10.5a simulator with waveform. The resultant waveforms are showed in the Figure.4 and Figure 5.

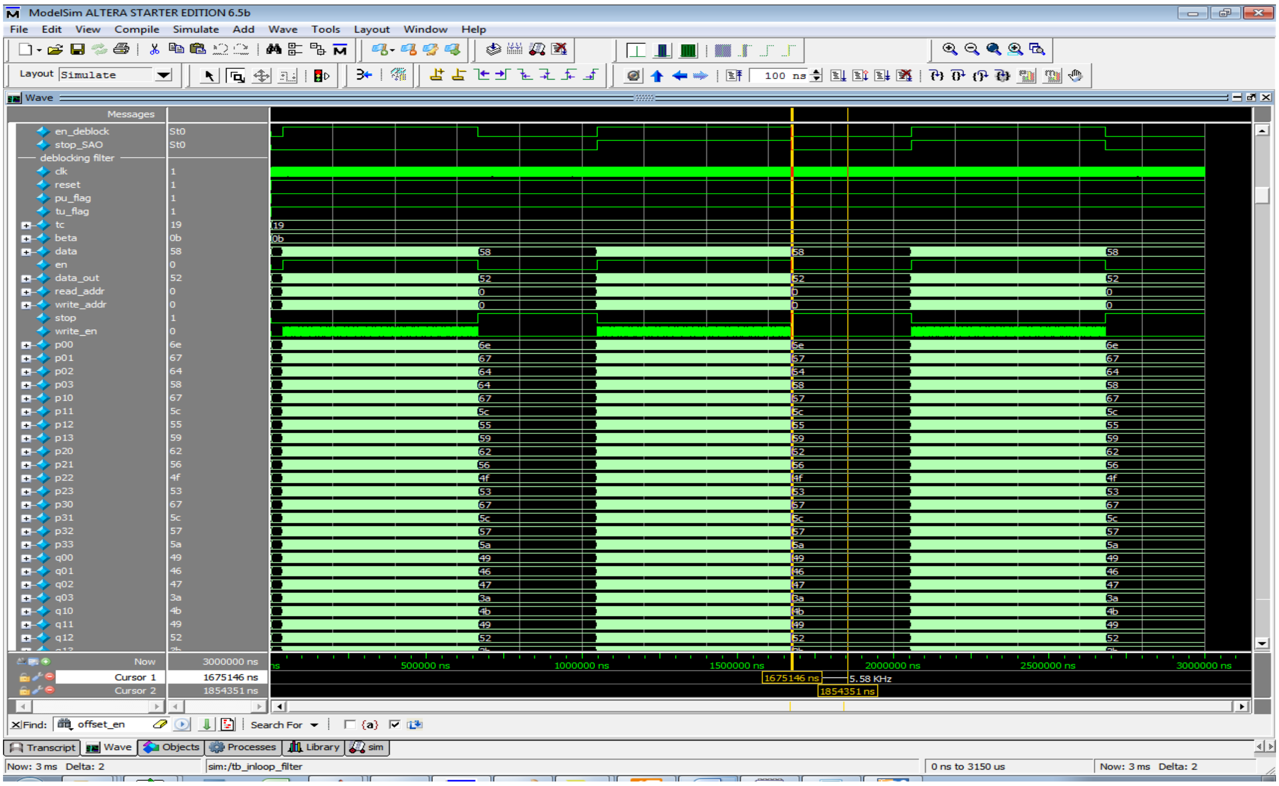


Fig. 4: Deblocking filter

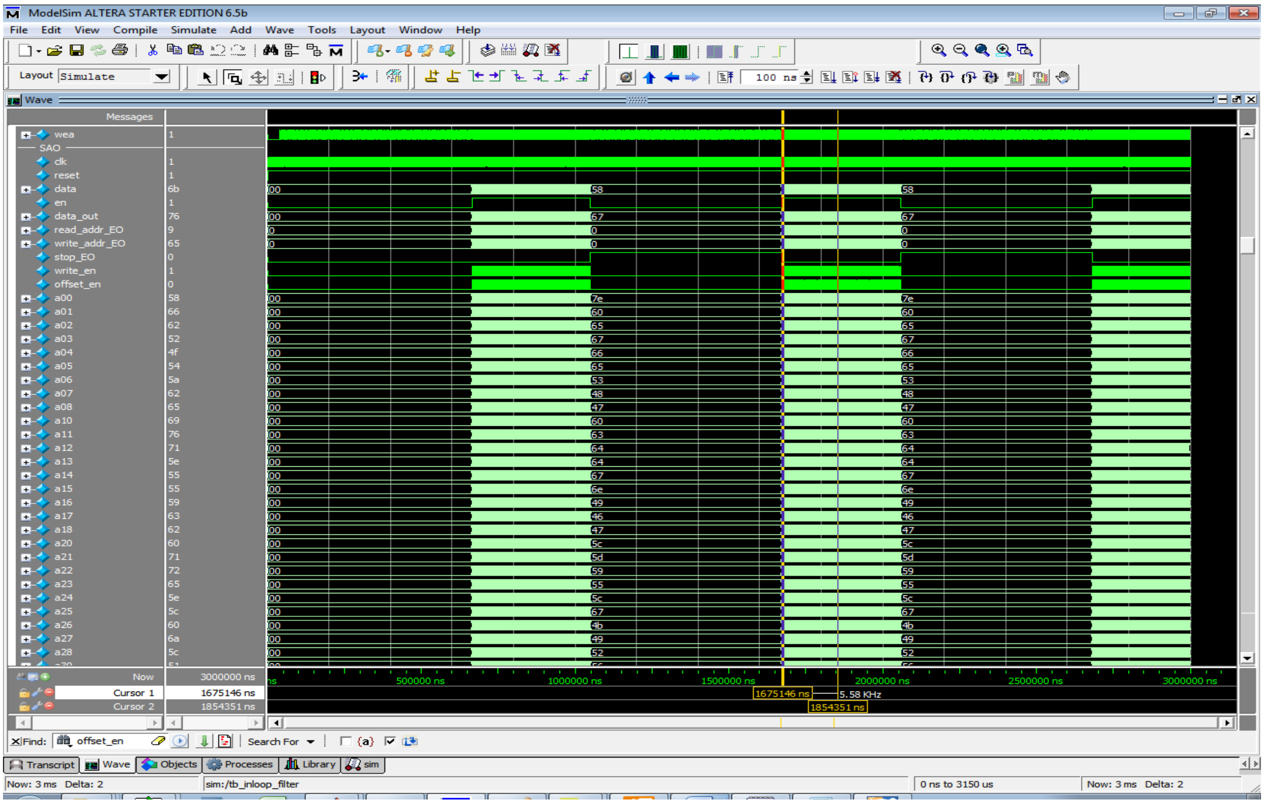


Fig. 5: SAO

The Synthesize results are obtained by Xilinx ISE 14.7 platform which is targeted for Virtex -6 XC6VLX130T device. The results are discussed in table 1 & 2.

Table 1. Virtex6 FPGA synthesize result for Deblocking filter – HEVC

Deblocking filter	
Power consumption(W)	3.347
Delay(ns)	6.438
Area (LUT)	10070

Table 2. Virtex6 FPGA synthesize result for SAO in HEVC

SAO	
Power consumption(W)	2.367
Delay(ns)	5.631
Area (LUT)	9256

5. Conclusion

In this work, low complexity of altered deblocking filter order and SAO is proposed to decrease the ringing artifacts and to improve video frame quality. SAO and Deblocking filter minimizes the hardware complexity of HEVC decoder which results in table 1&2. By this modified filter order and SAO architecture give less register memory, Look up table ,slices when compare to previous systems.

References

[1] S.Srinivasan, "Windows Media Video 9: Overview and applications," Signal Process. Image Communcation., vol. 19,no. 9, pp. 851–875, Oct. 2004.

[2] C.-M. Fu, CE13: „Sample Adaptive Offset with LCU-Independent Decoding", JCTVC-E049, Mar. 2011.

[3] Yang Zhang, Zhi Liu, Jianfeng Qu : "Sample Adaptive Offset Optimization in HEVC" , Sensors & Transducers, Vol 182, Issue11,Nov.2014, pp. 237-243

[4] Norkin, A., Bjontegaard, G., Fuldseth, M., Ikeda, M., Andersson, K., Zhou, M. and Van der Auwera, G., 2012. HEVC deblocking filter. IEEE Transactions on Circuits and Systems for Video Technology, 22(12), pp.1746-1754.

[5] Esche, M., Glantz, A., Krutz, A. and Sikora, T., 2012. Adaptive temporal trajectory filtering for video compression. IEEE Transactions on Circuits and Systems for Video Technology, 22(5), pp.659-670.

[6] Ozcan, E., Adibelli, Y. and Hamzaoglu, I., 2013. A high performance deblocking filter hardware for high efficiency video coding. IEEE Transactions on Consumer Electronics, 59(3), pp.714-720.

[7] Vanne, J., Viitanen, M., Hamalainen, T.D. and Hallapuro, A., 2012. Comparative rate-distortion-complexity analysis of HEVC and AVC video codecs. IEEE Transactions on Circuits and Systems for Video Technology, 22(12), pp.1885-1898.

[8] Description of Core Experiment 1 (CE1): Sample Adaptive Offset Filtering, JCTVC-H1101, eb. 2012.

[9] R. Song, H. Cui, Y. Li, and X. Song, "A five-stage pipeline design of binary arithmetic encoder in H.264/AVC," in Proc. Asia-Pacific Signal Inform. Process. Assoc. Annu. Summit Conf., Dec. 2012, pp. 1–4.

[10] V. Rosa, L. Max, and S. Bampi, "High performance architectures for the arithmetic encoder of the H.264/AVC CABAC entropy coder," in Proc. IEEE 17th Int. Conf. Electron., Circuits, Syst., Dec. 2010, pp. 383–386.

[11] R. Kalaivani, K. Ramash Kumar, S. Jeevananthan, "Implementation of VSBSMC plus PDIC for Fundamental Positive Output Super Lift-Luo Converter," Journal of Electrical Engineering, Vol. 16, Edition: 4, 2016, pp. 243-258.

[12] K. Ramash Kumar,"Implementation of Sliding Mode Controller plus Proportional Integral Controller for Negative Output Elementary Boost Converter," Alexandria Engineering Journal (Elsevier), 2016, Vol. 55, No. 2, pp. 1429-1445.

[13] P. Sivakumar, V. Rajasekaran, K. Ramash Kumar, "Investigation of Intelligent Controllers for Varibale Speeed PFC Buck-Boost Rectifier Fed BLDC Motor Drive," Journal of Electrical Engineering (Romania), Vol.17, No.4, 2017, pp. 459-471.

[14] K. Ramash Kumar, D.Kalyankumar, DR.V.Kirbakaran" An Hybrid Multi level Inverter Based DSTATCOM Control, Majlesi Journal of Electrical Engineering, Vol. 5. No. 2, pp. 17-22, June 2011, ISSN: 0000-0388.

[15] K. Ramash Kumar, S. Jeevananthan, "A Sliding Mode Control for Positive Output Elementary Luo Converter," Journal of Electrical Engineering, Volume 10/4, December 2010, pp. 115-127.

[16] K. Ramash Kumar, Dr.S. Jeevananthan," Design of a Hybrid Posicast Control for a DC-DC Boost Converter Operated in Continuous Conduction Mode" (IEEE-conference PROCEEDINGS OF ICETECT 2011), pp-240-248, 978-1-4244-7925-2/11.

[17] K. Ramash Kumar, Dr. S. Jeevananthan," Design of Sliding Mode Control for Negative Output Elementary Super Lift Luo Converter Operated in Continuous Conduction Mode", (IEEE conference Proceeding of ICCCCT-2010), pp. 138-148, 978-1-4244-7768-5/10.

[18] K. Ramash Kumar, S. Jeevananthan, S. Ramamurthy" Improved Performance of the Positive Output Elementary Split Inductor-Type Boost Converter using Sliding Mode Controller plus Fuzzy Logic Controller, WSEAS TRANSACTIONS on SYSTEMS and CONTROL, Volume 9, 2014, pp. 215-228.

[19] N. Arunkumar, T.S. Sivakumaran, K. Ramash Kumar, S. Saranya, "Reduced Order Linear Quadratic Regulator plus Proportional Double Integral Based Controller for a Positive Output Elementary Super Lift Luo-Converter," JOURNAL OF THEORETICAL AND APPLIED INFORMATION TECHNOLOGY, July 2014. Vol. 65 No.3, pp. 890-901.

[20] Arunkumar, T.S. Sivakumaran, K. Ramash Kumar, "Improved Performance of Linear Quadratic Regulator plus Fuzzy Logic Controller for Positive Output Super Lift Luo-Converter," Journal of Electrical Engineering, Vol. 16, Edition:3, 2016, pp. 397-408.

[21] S.V.Manikanthan and K.Baskaran "Low Cost VLSI Design Implementation of Sorting Network for ACSFD in Wireless Sensor Network", CiiT International Journal of Programmable Device Circuits and Systems,Print: ISSN 0974 – 973X & Online: ISSN 0974 – 9624, Issue : November 2011, PDCS112011008.

[22] T. Padmapriya and V. Saminadan, "Distributed Load Balancing for Multiuser Multi-class Traffic in MIMO LTE-Advanced Networks", Research Journal of Applied Sciences, Engineering and Technology (RJASET) - Maxwell Scientific Organization , ISSN: 2040-7459; e-ISSN: 2040-7467, vol.12, no.8, pp:813-822, April 2016.