International Journal of Engineering & Technology, 7 (2.8) (2018) 578-582

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research Paper

Performance analysis of different designs of all-optical D flip flop

K.Archana*, R.Manohari, Shanthi prince

Department of ECE, SRM University, Chennai, Tamilnadu-603203, India
**Corresponding Author E-mail: archukams5@gmail.com*

Abstract

All optical flip flops play an important role in optical networks as well as in the field of optical computing. Optical memories are used for storing decisions in photonic packet routers temporarily. In this paper all optical D-flip flop is designed based on all optical gates. The nonlinear effects such as XGM (Cross Gain Modulation), XPM (Cross Phase Modulation) and FWM (Four Wave Mixing) are used to design all optical gates. We designed the D flip flop based on two logic that are NAND-NAND logic and NAND-NOR logic. The performance of both the designs is analyzed and the functionality of all optical D-flip-flop is verified using the truth table. It is proved that NAND-NAND logic is more effective than NAND-NOR logic.

Keywords: *Semiconductor optical amplifier, All optical gates, Cross Gain Modulation, All optical flip flops, Cross Phase Modulation, Four Wave Mixing*

1. Introduction

All optical flip-flops are attractive as they can be used as one of the main components in packet switched networks of optical domain which constitutes of packet forwarding, packet buffering and packet routing, leading to wider bandwidth of the fiber and increased forwarding capability of the routers.

The functionality of optical switched networks is mainly dependent on functions of signal processing which include recognition of optical headers, conversion of wavelength and switching. Semiconductor optical amplifiers exhibit a promising future for the evolution of optical networks and will continue to become a versatile technology for the upcoming generations of optical networks. Semiconductor optical amplifiers avoid the need of conversion from electrical to optical signal. SOAs not only function as general gain unit but also function as modulator, wavelength converter and optical switch in optical networks [1]. Some of the challenges associated with performance of SOA are higher noise, polarization dependence and high nonlinearity with fast transient time [2]. In this paper, D flip flop is designed using all optical NAND and all optical NOR gates.

2. SOA-MZI

All optical logic gates are implemented using Semiconductor optical amplifiers(SOA) and Mach-Zehnder interferometer. Semiconductor optical amplifiers show a considerable change in refractive index combined with increased gain. Apparently, the non linear behaviour of SOA which is a drawback can be used as a considerate option for an optical gate that is controlled optically. The non linear effects associated with semiconductor optical amplifiers are cross gain modulation, cross phase modulation and four wave mixing [3]. The self phase modulation is one of the nonlinear effect of SOA in which the amplifier output phase is modulated due to the variation of refractive index caused by the change in input signal power. The cross phase modulation is almost same as self phase modulation but it refers to variation in refractive index due to an optical signal which constitutes of either a control signal or a pump signal that leads to a change in phase of any other optical signal, like a probe signal which is travelling at the same time in the semiconductor optical amplifier structure. In the active regions of SOA, gain saturation effect is employed due to conversion of optical wavelength. Conversion of signal involves phase change and reduction in gain causing amplitude imbalance in the interferometer. So, cross phase modulation enhances the wavelength conversion efficiency. The cross gain modulation occurs due to change in amplifier gain with respect to input signal power. The decrease in amplification gain and carrier density of the semiconductor optical amplifier is caused due to increment in input signal power. Four wave mixing is a third order non-linear process. The phenomenon occurs in a matter of picoseconds. It is not dependent on modulation format and has a capability to compensate for dispersion occurrences. Therefore, conversion of wavelength based on four wave mixing provides transparency and has the capability of multiple wavelength conversions [4]. It is produced when two channels beat at different frequencies modulating the signal phase and generating new tones.

3. Design of NAND Gate Based on SOA-MZI

The Boolean expression for NAND gate is $Y = \overline{A.B}$. The condition for NAND gate is that if the two inputs given to the gate are high, the output of the gate is low, otherwise the output of the NAND gate is high. If the two input signals given to the gate are logic "1" ,then the resulting output of the gate is logic "0" or otherwise output of the gate is logic "1"[5]. The input signals which enter the gate at the port1 and port 3 are as shown in Fig 1. The control signal is the CW laser (Continuous Wave laser) which generates the probe pulses and enters the device at port2.

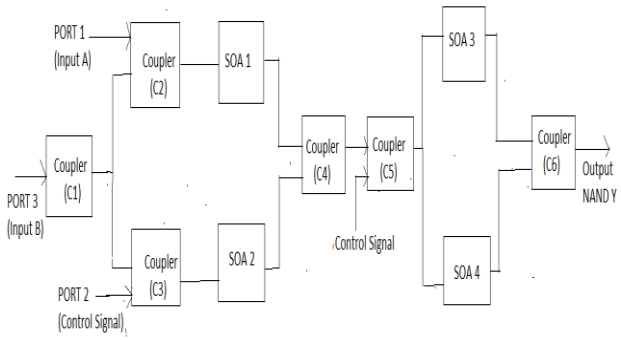

Fig. 1: Block diagram of NAND gate based on SOA-MZI.

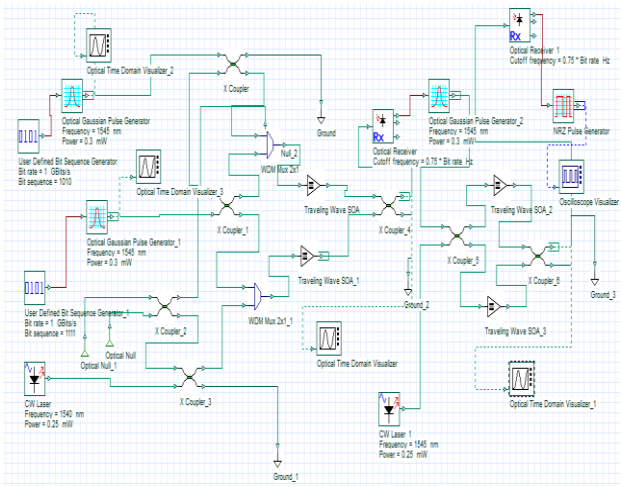

Fig. 2: Simulation setup of NAND gate based on SOA-MZI.

The NAND gate is simulated as shown in Fig 2. The Optical Gaussian Pulse Generators are used to generate the input data signals, operating at 1545nm and the power is set up to 0.3mw. A Continuous Wave laser operates at 1540nm with 0.25mw power. A Gaussian optical filter operates at 1540nm with a bandwidth of 20 GHZ . This Gaussian optical filter is used to filter the signals so that the required signals are only obtained at the output. The signal from coupler (C1) is split and given to input ports of coupler (C2) and coupler (C3). The coupled signals from coupler (C2) and coupler (C3) pass through SOA 1 and SOA 2 having injection current of 0.15A.The signals from SOA 1 and SOA 2 are coupled by coupler (C4). The output signal from coupler (C4) is given as input to coupler (C5) along with the control signal. The signals that are split from coupler (C5) are amplified by SOA 3 and SOA 4, which are then coupled by a coupler (C6), which gives the final output of NAND gate.

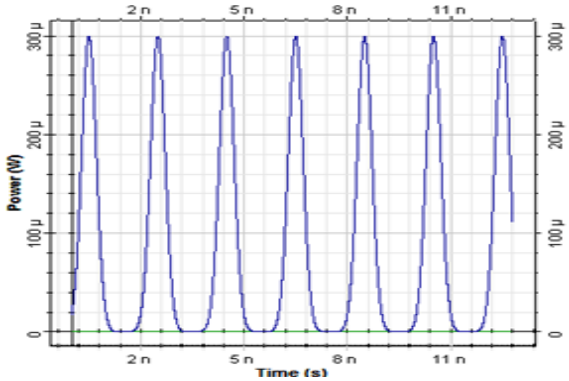

Fig. 3: Input A (1010) for NAND Gate

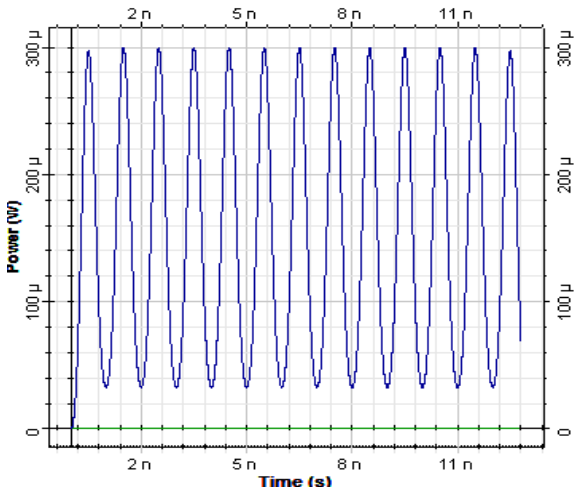

Fig. 4: Input B (1111) for NAND Gate

Table 1: Truth table for NAND gate

Input A	Input B	Output $Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

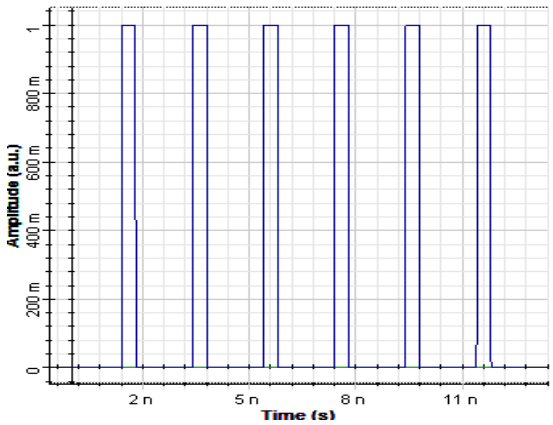

Fig. 5: Output Y (0101) for NAND Gate

The Input A of NAND Gate is 1010 as shown in Fig 3 and the Input B is 1111 as shown in Fig 4. The Output Y of NAND Gate is 0101 as shown in Fig 5 and it is verified with its truth table shown in Table 1.

4. Design of NOR Gate Based on SOA-MZI

The input data signals are coupled using the coupler (C1) as shown in Fig 6. The coupled signal undergoes amplification as it passes through SOA1.The amplified signal from SOA 1 is given as input to Coupler (C2) along with the control signal. The signals that are split from coupler (C2) are amplified by SOA 2 and SOA 3, which are then coupled by a coupler (C3) gives the final output of NOR gate. The NOR gate based on SOA-MZI is simulated as shown in Fig 7.

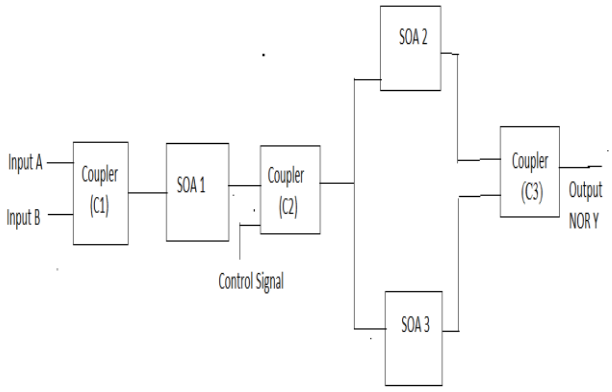

Fig. 6: Block diagram of SOA-MZI based NOR gate.

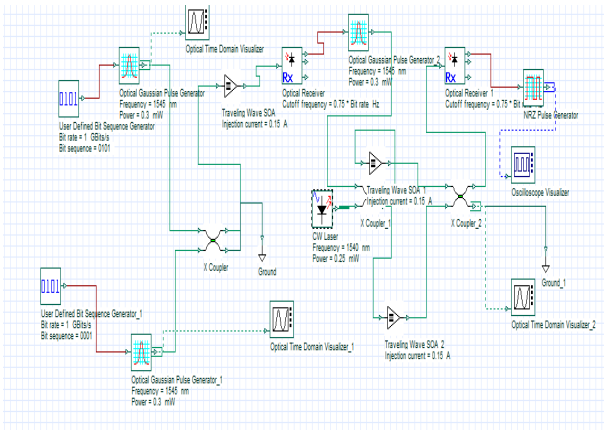

Fig. 7: Simulation setup of SOA-MZI based NOR gate.

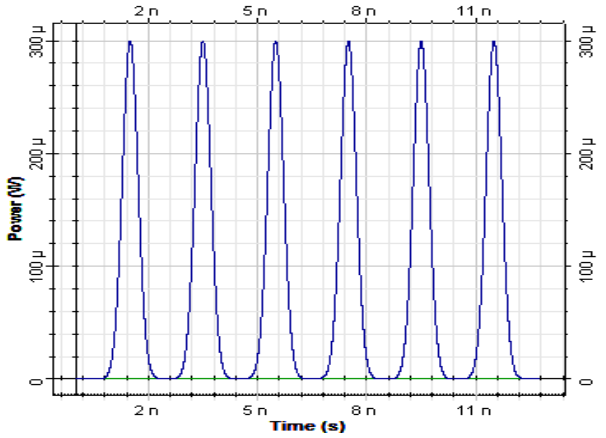

Fig. 8: Input A (0101) for NOR Gate

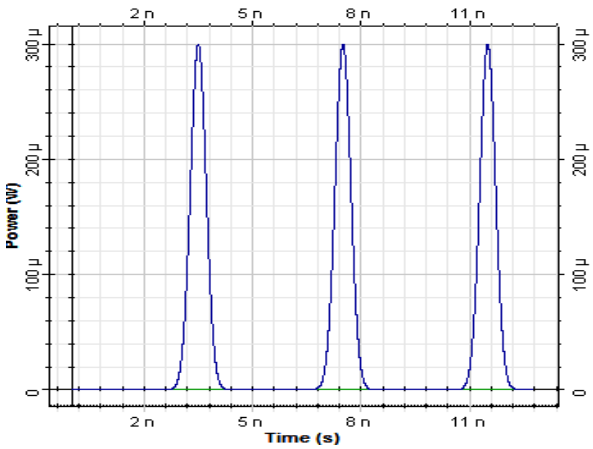

Fig. 9: Input B (0001) for NOR Gate

Table 2: Truth Table for NOR gate

Input A	Input B	Output $Y=\overline{(A+B)}$
0	0	1
0	1	0
1	0	0
1	1	0

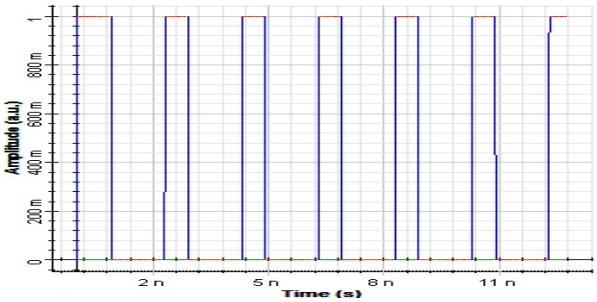

Fig. 10: Output Y (1010) for NOR Gate

The Input A of NOR Gate is 0101shown in Fig 8 and the Input B is 0001 show in Fig 9. The Output Y of NOR Gate is 1010 shown in Fig 10 and the verification is done using the truth table shown in Table 2.

5. Design of D Flip Flop Based on SOA-MZI

The D flip flop stores the value present on the data line, hence it is also known as data flip flop. The D flip flop behaves as a basic memory cell [8]. It is even called as a delay flip flop because the D input state is taken by Q output.The input that appears at the D input, will appear at output Q in the presence of active clock signal. If the current state D = 0 and CLK= 1, then Q= 0 will appear as the next state and it is same as D [9]. The block schematic for D flip flop using NAND-NAND logic is shown in Fig 11 and design of D flip flop based on NAND-NOR logic is shown in Fig 12.

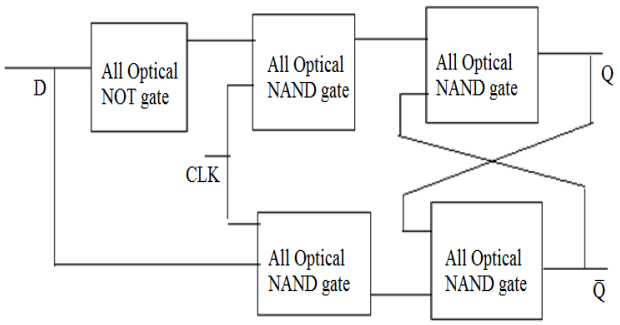

Fig. 11: D flip flop based on NAND-NAND logic

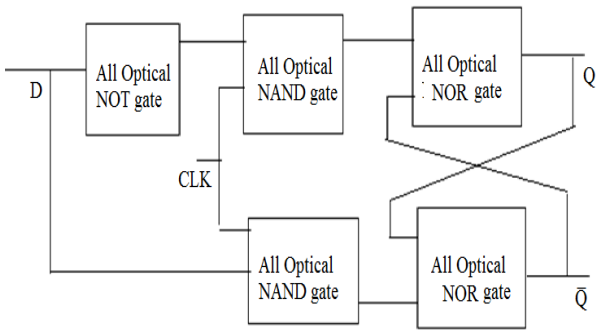

Fig. 12: D flip flop based on NAND-NOR logic

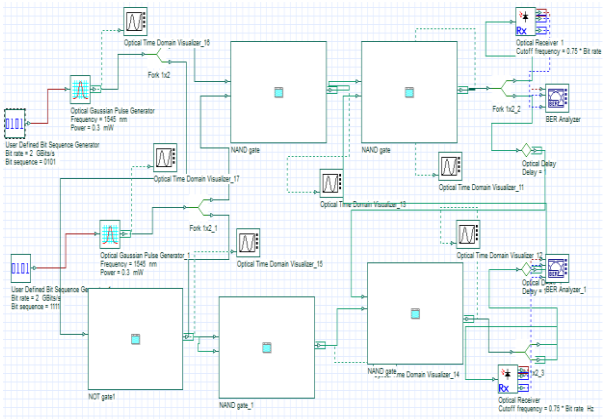

Fig. 13: Simulation setup of D flip flop based on NAND-NAND logic

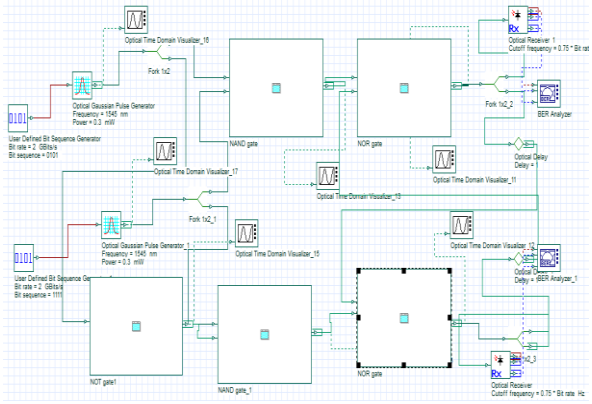

Fig. 14: Simulation setup of D flip flop based on NAND-NOR logic

The D flip flop is designed using NAND-NOR logic and NAND-NAND logic. The inputs given for both the designs of D flip flop is the same. The simulation layout for D Flip Flop design using NAND-NAND logic is shown in Fig 13 and the simulation layout for D flip flop using NAND-NOR logic is shown in Fig 14.

Table 3: Truth table for D flip flop

CLK	D	Q(t+1)	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	Q	$\bar{Q}$
1	0	0	1
1	1	1	0

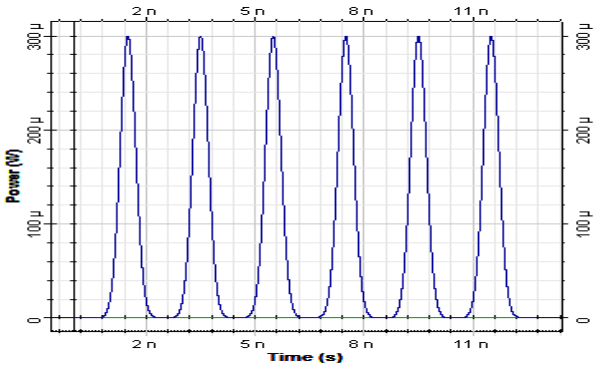

Fig. 15: Input D (0101) of D flip flop

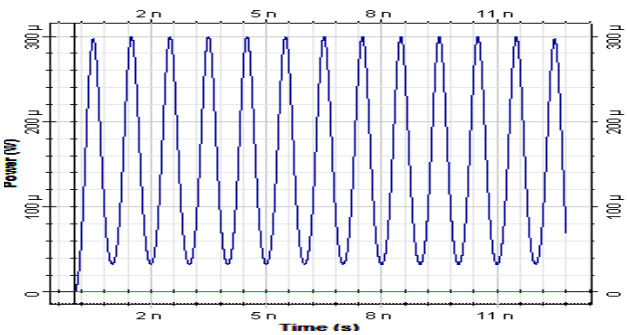

Fig. 16: CLK (1111) of D flip flop

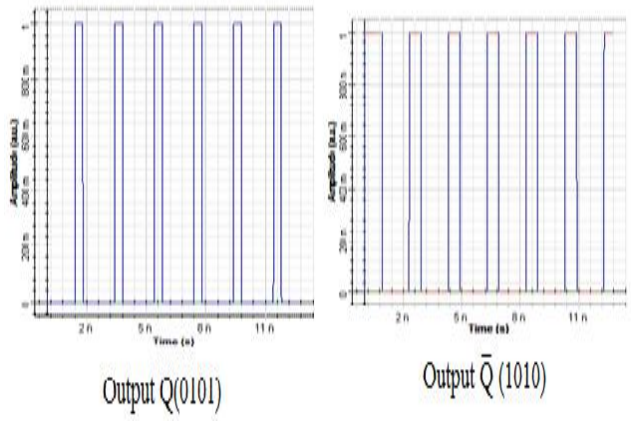

Fig. 17: Output Q (0101) and $\bar{Q}$ (1010) of D flip flop using NAND- NAND logic

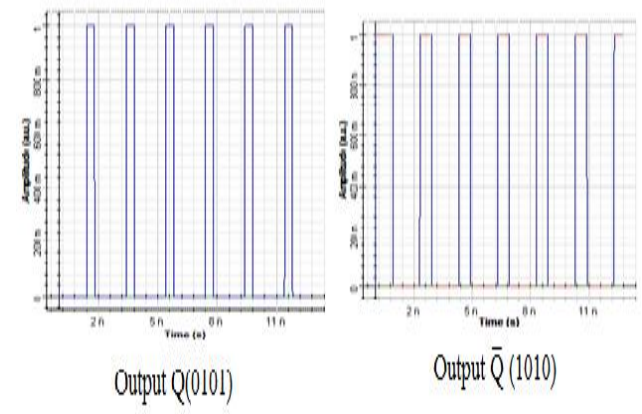

Fig. 18: Output Q (0101) and $\bar{Q}$ (1010) of D flip flop using NAND-NOR logic

The inputs for both the designs of D Flip Flop using NAND-NAND logic and NAND-NOR logic are the same, D=0101, CLK=1111 shown in Fig 15 and Fig 16. The outputs of D Flip Flop design using NAND-NAND logic are Q = 0101, $\bar{Q}$=1010 as shown in Fig 17 and the outputs of D Flip Flop design using NAND-NOR logic are Q =0101, $\bar{Q}$=1010 shown in Fig 18.The design of D flip flop is verified using truth table shown in Table 3.

6. Comparision of the Two Flip Flop Designs

The performance of D flip flop designs are analyzed in terms of Bit Error Rate (BER) and Quality factor as shown in Table 4. The bit error rate for the NAND-NAND logic design is lower than the NAND-NOR logic design and the quality factor for the NAND-NAND logic design is higher than the NAND-NOR logic design. So, all optical D flip flop design based on NAND-NAND logic is proven to be more effective than NAND-NOR logic.

Table 4: Comparision of the two flip flop designs

Data rate	BER		Quality factor	
	NAND - NAND	NAND-NOR	NAND-NAND	NAND-NOR
1 Gb/s	0.00425	0.00769	3.39	2.98
2 Gb/s	0.00652	0.00827	3.36	2.57

7. Conclusion

In this paper, all optical gates are designed based on non linearities of SOA and D flip flop is designed using all optical gates. Theoretical analysis and simulations are performed to validate the proposal using optisystem software. All optical D flip flop is designed using two methodologies based on NAND-NAND logic and NOR-NOR logic. All optical D flip flop design using NAND-NAND logic is proven to be more effective which is used for the design of shift registers.

References

[1] Lina Wang Su, Yongjun Wang Su, Shuai Wang , Sichuan Geng , Mingxiao Zhang, "All optical Flip Flop based on SOA-MZI", Progress in electromagnetic research symposium, November10,2016.

[2] LinaWang , YongjunWang, ShuaiWang , ChenWu , Mingxiao Zhang, "All optical Flip Flop based on SOA-PSW", PHOTONIC SENSORS / Vol No. 4, 2016: 366–371 Jul,2016.

[3] Youssef Said and Houria Rezig "SOAs Nonlinearities and Applications for Next Generation of Optical Networks" , National Engineering School of Tunis (ENIT) Tunisia; Feb 14, 2013.

[4] Eman M. El-Saeed; Ahmed Abd El-Aziz; Heba A. Fayed; Moustafa H. Aly, "Optical logic gates based on SOA, Mach–Zehnder interferometer: design and simulation", SIPE Journals, Optical Engineering Volume 55, Issue 2,2016.

[5] Satya.s, R.Manohari, Shanthi Prince, "Design of full adder – subtractor based on SOA-MZI ", IEEE, Signal processing and engineering(SPACES),INSPEC14984708,March 2015.

[6] Hongyu Hu1 , Xiang Zhang1 and Shuai Zhao, High-speed all-optical logic gate using QD-SOA and its application, Hu etal.,CogentPhysics(2017),4: 1388156,26 september,2017.

[7] Meloni, G.; Berrettini, G.; Potì, L; Bogoni, A. All- Optical D Flip-Flop and Optical AND Gate, accepted for publication at ECOC 2014.

[8] Berrettini, G.; Meloni, G.; Potì, L.; Bogoni, A. (2009). All-Optical clocked D type flip flop exploiting SOA-based optical SR latch and logic gates, accepted for publication at Photonics in Switching 2013.

[9] S. Pitris, C. Vagionas, T. T. R. B. G. K. and Pleros, N. "Wdm-enabled optical ram at 5gb/s using a monolithic flip-flop chip." IEEE Photonics Journal, 1943 0655, 2015.

[10] T.Padmapriya and V.Saminadan, "Utility based Vertical Handoff Decision Model for LTE-A networks", International Journal of Computer Science and Information Security, ISSN 1947-5500, vol.14, no.11, November 2016.

[11] S.V.Manikanthan and V.Rama "Optimal Performance Of Key Predistribution Protocol In Wireless Sensor Networks" International Innovative Research Journal of Engineering and Technology, ISSN NO: 2456-1983, Vol-2, Issue –Special – March 2017.