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Research Paper

Performance evaluation and analysis of 64-quadrature amplitude modulator using Xilinx Spartan FPGA

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Abstract

This paper proposes the design of 64-Quadrature Amplitude Modulation using the Very High Speed Integrated Circuit Hardware Description Language (VHDL) coding and XILINX SPARTAN Field Programmable Gate Array (FPGA) real-time implementation for validation. QAM is used in modern digital communication applications like set-top box, satellite TV, wireless and cellular technology etc. In this paper, 64-QAM is implemented and compared with three different XILINX SPARTAN FPGA devices say 3A DSP, 3E and 6E. The power, current and thermal parameters are performed and compared. The power consumed for the design of 64 QAM using the Xilinx SPARTAN 6E FPGA device is 0.014W and 15.9 C/W of Effective TJA for the XILINX SPARTAN 3A DSP FPGA. The device utilization of the 64-QAM design using the XILINX SPARTAN 3A DSP is low.

Keywords: *Digital Modulation, ASK, PSK, QPSK, QAM, VHDL language, XILINX FPGA.*

1. Introduction

Modulation can be broadly classified as analog modulation and digital modulation. The digital modulation is advantages compared to the analog modulation with respect to accuracy, high performance, easy design and debug, less in area, minimum power consumption and reliability. The digital modulation can be further divided into ASK, PSK and QPSK or QAM. The ASK involves with the amplitude level changes with respect to the carrier signal. The PSK refers to the phase changes with the carrier signal.

The QPSK or QAM is a digital modulation technique which combines both the ASK and PSK. Depending on the resolution (2N bits), the QAM is referred as 16-QAM for N=4, 64-QAM for N=6 and 256=QAM for N=8. For the 16-QAM, the N=4 gives the combination of bits for 24 bits starting from 0000 to 1111. The 4 bits B3B2B1B0 are split into equally as B3B2 bits for cosine and B1B0 for sine wave. Here B0 is used for the phase shift or direction of the sine wave. That is B0 is used for PSK with the sine wave. B1 is used for the amplitude level or ASK. Similarly, B3 for the ASK with the cosine wave and B2 uses the PSK for the cosine wave. The 64-QAM could be elaborated with higher order ASK and PSK.

The QAM with the resolution of 2^2 bits is referred as Quadrature Phase Shift Keying (QPSK). QPSK are immune to noise and improves the Signal-to Noise Ratio (SNR) [1]. QPSK-like differential encoding aides in high baud rate transmission [2]. The QAM is easily designed with the use of common logic circuits such as multiplier, adder, incrementer, decrementer, row counter, and column counter [3]. The QAM used in the turbo MIMO scheme using arithmetic extended mapping scheme improves the SNR by 1.8 dB at BER of 10^{-4} [4].

The Versatile digital QAM modulator with innovative logic structure, enhanced dedicated DSP blocks, and the revolutionary memory blocks and FPGAs are perfect for cable head-end system designers who desire flexibility and speedy time to market [5].

Embedded multiplier based QAM [6] using the FPGA is advantages of technology mapping in terms of time [7], area and power consumption [8].QAM based on the system generator tool is performed and analysed to prove its feasibility [9]. QAM has its application with OFDM transmission [10], Digital Television Modem and Digital Satellite TV. Non-linear system analysis using digital controllers [11-20].

In this paper, the 64 QAM is designed using the VHDL and real time implemented using the FPGA device. The FPGA design performance is validated and compared with respect to current, power and thermal properties for the three Xilinx SPARTAN FPGA devices namely 3A DSP, 3E and 6E.

2. Proposed 64-QAM Design Methodology

The block diagram of the proposed 64-QAM design is as given Figure.1. The 2^6 bit are divided into 2^3 bits for MSB as Q1, Q0, Q' and 2^3 bits for LSB as I1, I0, I'. The Q' and I' indicate the shift of the cosine and sine wave respectively. The Q1, Q0 and I1, I0 represent the amplitude levels of the cosine and sine wave respectively. Carrier oscillator is provided as the reference for the sine and cosine wave. The function of the summation is for the addition of the cosine and sine signals as per the value given in 2^6 bits.

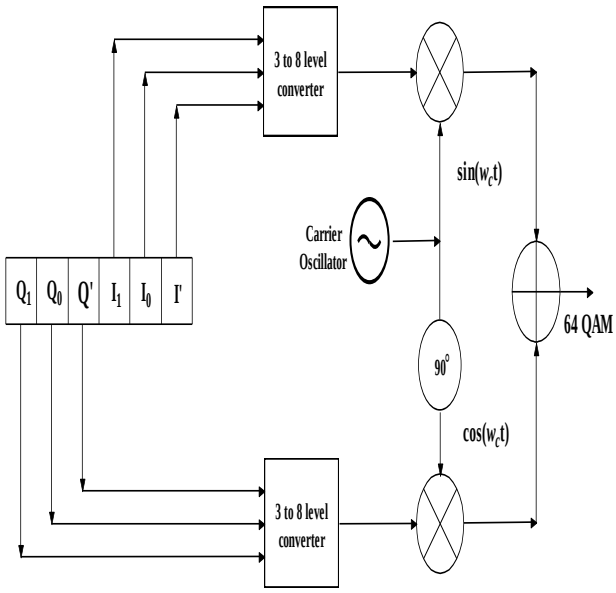


Fig. 1: Block diagram for the 64-QAM

Table 1: Indicates the amplitude levels of cosine and sine wave for all possible 2^3 bits

Cosine wave				Sine wave			
Q_1	Q_0	Q'	selected wave	I_1	I_0	I'	selected wave
0	0	0	1V	0	0	0	1V
0	0	1	-1V	0	0	1	-1V
0	1	0	0.75V	0	1	0	0.75V
0	1	1	-0.75V	0	1	1	-0.75V
1	0	0	0.5V	1	0	0	0.5V
1	0	1	-0.5V	1	0	1	-0.5V
1	1	0	0.25V	1	1	0	0.25V
1	1	1	-0.25V	1	1	1	-0.25V

Table 2 indicates the Amplitude Levels (AL) for all possible combination of sine and cosine wave form. The negative sign refers to the 180° in the wave. In this design, the 64 QAM uses levels like 1V, 0,75V, 0.5V and 0.25V along with their 180° phase shifted wave. Thus the 64-QAM constitutes 16 signals in which 8 are for sine wave and 8 are for cosine wave.

Table 2: Detailed bit description for the 64-QAM

2^6 binary values	B_5	B_4	B_3	B_2	B_1	B_0
2^6 bit values are split into two 2^3 bits as MSBs ($B_5B_4B_3$) and LSBs ($B_2B_1B_0$)	2^3 MSB ($B_5B_4B_3$) used for the cosine wave representation			2^3 LSB ($B_2B_1B_0$) used for the sine wave representation		
	B_5 & B_4 indicate the Amplitude Levels (AL) for the cosine wave B_5B_4 = 00, AL = 1V B_5B_4 = 01, AL =0.75V B_5B_4 = 10, AL = 0.5V B_5B_4 = 11, AL =0.25V		B_3 indicates the shift of the cosine wave. If B_3=0; 0° shift. If B_3=1; 180° shift.	B_2 & B_1 indicate the Amplitude Levels (AL) for the Sine wave B_2B_1 = 00, AL = 1V B_2B_1 = 01, AL =0.75V B_2B_1 = 10, AL = 0.5V B_2B_1 = 11, AL =0.25V		B_0 indicates the shift in the sine wave If B_0=0; 0° shift. If B_0=1; 180° shift.

The 2^6 bit values are coded accordingly starting from 000000 to 111111. The 64 bit QAM is designed with the following methodology

i) The 2^6 bits are divided into two parts of length 2^3 bits as MSBs and LSBs

ii) The 2^3 bits of the LSBs (say B2B1B0) are utilized for defining the sine wave. The B0 indicating the sine wave shift. If B0 = 0, the sine wave is not shifted, and if B0 = 1, the sine wave is 180° shifted.

iii) The remaining two bits B2B1 represent the level of the sine wave. As given in the Table 2, the B2B1 values decide the AL of the sine wave.

iv) Similarly, the MSBs (say B5B4B3) are considered for the cosine wave generation. The B3 indicating the cosine wave shift. If B3 = 0, the cosine wave is not shifted, and if B3 = 1, the sine wave is 180° shifted.

v) The cosine wave and sine wave are added depending on the given 2^6 value.

vi) For example, consider the 2^6 value is 101110. Now 101 is the MSB for cosine wave and 110 is the LSB for sine wave. The LSB corresponds to B2B1=11 indicate the AL as 0.25V and B0=0 indicating the sine is not shifted. The MSB corresponds to B5B4=10 indicate the AL as 0.5V and B3=1 indicating the cosine is 180° shifted.

Table 3: Maximum Value (r) and its corresponding angle (θ) for 2^6 values with rectangle form in (x,y) co-ordinates

Values	Angle Theta (θ)	Magnitude (r)	cos θ	sin θ	x = r cos θ	y = r sin θ
0	45°	1.4142	0.707107	0.707107	0.99999	0.99999
1	315°	1.4142	0.707107	-0.70711	0.99999	-0.99999
2	37°	1.25	0.798636	0.601815	0.998294	0.752269
3	323°	1.25	0.798636	-0.60182	0.998294	-0.75227
4	27°	1.118	0.891007	0.45399	0.996145	0.507561
5	333°	1.118	0.891007	-0.45399	0.996145	-0.50756
6	14°	1.03078	0.970296	0.241922	1.000161	0.249368
7	346°	1.03078	0.970296	-0.24192	1.000161	-0.24937
8	135°	1.4142	-0.70711	0.707107	-0.99999	0.99999
9	225°	1.4142	-0.70711	-0.70711	-0.99999	-0.99999
10	143°	1.25	-0.79864	0.601815	-0.99829	0.752269
11	217°	1.25	-0.79864	-0.60182	-0.99829	-0.75227
12	153°	1.118	-0.89101	0.45399	-0.99615	0.507561
13	207°	1.118	-0.89101	-0.45399	-0.99615	-0.50756
14	166°	1.03078	-0.9703	0.241922	-1.00016	0.249368
15	194°	1.03078	-0.9703	-0.24192	-1.00016	-0.24937
16	53°	1.25	0.601815	0.798636	0.752269	0.998294
17	307°	1.25	0.601815	-0.79864	0.752269	-0.99829
18	45°	1.06066	0.707107	0.707107	0.75	0.75

19	315°	1.06066	0.707107	-0.70711	0.75	-0.75
20	34°	0.90137	0.829038	0.559193	0.74727	0.50404
21	326°	0.90137	0.829038	-0.55919	0.74727	-0.50404
22	18°	0.79055	0.951057	0.309017	0.751858	0.244293
23	342°	0.79055	0.951057	-0.30902	0.751858	-0.24429
24	127°	1.25	-0.60182	0.798636	-0.75227	0.998294
25	233°	1.25	-0.60182	-0.79864	-0.75227	-0.99829
26	135°	1.06066	-0.70711	0.707107	-0.75	0.75
27	225°	1.06066	-0.70711	-0.70711	-0.75	-0.75
28	146°	0.90137	-0.82904	0.559193	-0.74727	0.50404
29	214°	0.90137	-0.82904	-0.55919	-0.74727	-0.50404
30	162°	0.79055	-0.95106	0.309017	-0.75186	0.244293
31	198°	0.79055	-0.95106	-0.30902	-0.75186	-0.24429
32	63°	1.118	0.45399	0.891007	0.507561	0.996145
33	297°	1.118	0.45399	-0.89101	0.507561	-0.99615
34	56°	0.90137	0.559193	0.829038	0.50404	0.74727
35	304°	0.90137	0.559193	-0.82904	0.50404	-0.74727
36	45°	0.70711	0.707107	0.707107	0.500002	0.500002
37	315°	0.70711	0.707107	-0.70711	0.500002	-0.5
38	27°	0.559	0.891007	0.45399	0.498073	0.253781
39	333°	0.559	0.891007	-0.45399	0.498073	-0.25378
40	117°	1.118	-0.45399	0.891007	-0.50756	0.996145
41	243°	1.118	-0.45399	-0.89101	-0.50756	-0.99615
42	124°	0.90137	-0.55919	0.829038	-0.50404	0.74727
43	236°	0.90137	-0.55919	-0.82904	-0.50404	-0.74727
44	135°	0.707	-0.70711	0.707107	-0.49992	0.499924
45	225°	0.707	-0.70711	-0.70711	-0.49992	-0.49992
46	153°	0.559	-0.89101	0.45399	-0.49807	0.253781
47	207°	0.559	-0.89101	-0.45399	-0.49807	-0.25378
48	76°	1.03078	0.241922	0.970296	0.249368	1.000161
49	284°	1.03078	0.241922	-0.9703	0.249368	-1.00016
50	72°	0.79055	0.309017	0.951057	0.244293	0.751858
51	288°	0.79055	0.309017	-0.95106	0.244293	-0.75186
52	63°	0.559	0.45399	0.891007	0.253781	0.498073
53	297°	0.559	0.45399	-0.89101	0.253781	-0.49807
54	45°	0.35355	0.707107	0.707107	0.249998	0.249998
55	315°	0.35355	0.707107	-0.70711	0.249998	-0.25
56	104°	1.03078	-0.24192	0.970296	-0.24937	1.000161
57	256°	1.03078	-0.24192	-0.9703	-0.24937	-1.00016
58	108°	0.79055	-0.30902	0.951057	-0.24429	0.751858
59	252°	0.79055	-0.30902	-0.95106	-0.24429	-0.75186
60	117°	0.559	-0.45399	0.891007	-0.25378	0.498073
61	243°	0.559	-0.45399	-0.89101	-0.25378	-0.49807
62	135°	0.35355	-0.70711	0.707107	-0.25	0.249998
63	225°	0.35355	-0.70711	-0.70711	-0.25	-0.25

vii) The 2^6 values from 000000 to 111111 are split as 2^3 MSBs and 2^3 LSBs, assigned with sine and cosine wave with desired AL accordingly.

viii) The maximum value indicated as "Magnitude (r)" for each of the 2^6 values is extracted along with its angle denoted by "Theta (θ)".

ix) The r and θ corresponds to the polar form of the coordinates. In order to convert the polar form to the rectangular form, the following formulation is utilized

$$x = r\cos(\theta) \text{ and } y = r\sin(\theta)$$

Table 3 depicts the manipulation of the r, θ and its rectangular form in x and y.

x) The coordinate values of (x,y) are plotted to obtain the constellation diagram.

xi) The design procedure is coded using the VHDL code. The behavioural and mixed styles are used within the code.

xii) Resolution of 2^6 bits is maintained for the 64-QAM.

xiii) The real time implementation of the synthesized 64 QAM VHDL code is performed using the XILINX ISE 12.1.

The XILINX Spartan 3A DSP, 3E and 6E FPGA devices are utilized for the analysis and comparison with respect to current, power and thermal parameters.

3. Results and Discussions

The VHDL code for the sine wave and cosine wave is designed using the mixed style of modelling. For the 64 bit QAM, the sine wave and cosine wave with their 180° shifted waves are considered in the VHDL coding. The resolution of sine wave and cosine wave is 2^8 bits. That is, the time samples are divided into 256 samples. The amplitude levels are assigned with the levels of 0.25V, 0.50V, 0.75V and 1V are digitized with the resolution of 2^8 bits. Thus amplitude levels are considered as 64 bits for 0.25V, 128 bits for 0.50V, 192 bits for 0.75V and 256 bits for 1V.

The sine wave and cosine wave simulated using the MODEL SIM software are given in Figure. 2 and Figure 3 respectively. According to the 2^6 values, the sine and cosine waves are added to give 64-QAM output. The simulated output waveform for the 64-QAM modulator is depicted in the Figure 4. The constellation diagram for the 64-QAM using the MATLAB tool is shown in Figure 5. The constellation proves the accuracy of the proposed design and the RTL view for implementation of the 64-QAM VHDL code is shown in Figure 6. Table 4, 5 and 6 show the power, current and thermal of the 64-QAM using XILINX SPARTAN 3A DSP, XILINX SPARTAN 3E and XILINX SPARTAN 6E FPGA respectively. Table 7, 8 and 9 show the device utilization chart of the 64-QAM using FPGA devices. Table 10 presents the performance comparison for the 64-QAM

using FPGA devices. Form the Table 10, the power consumption and temperature of the proposed 64-QAM modulator using XILINX SPARTAN 6E FPGA is low. Table 11 refers to the comparison of device utilization for the proposed 64-QAM modulator using FPGA devices. The device utilization of the proposed method using the SPARTAN 3A DSP holds good and satisfactory.

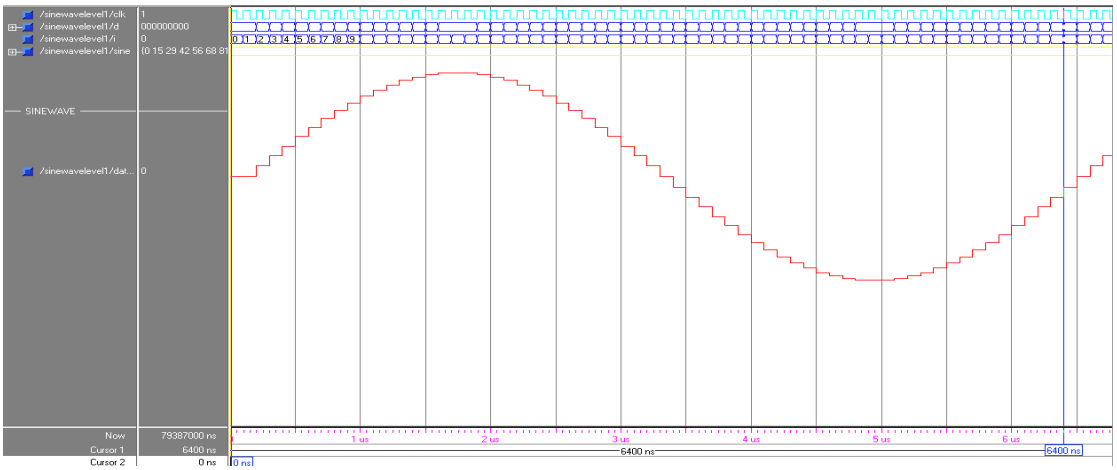


Fig. 2: Model SIM output for the sine wave generation

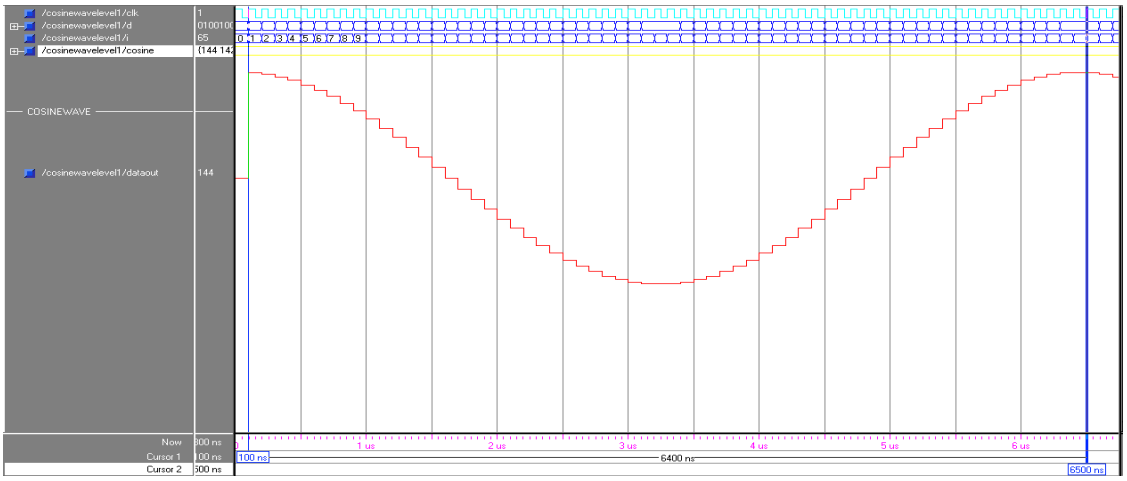


Fig. 3: ModelSIM output for the cosine wave generation

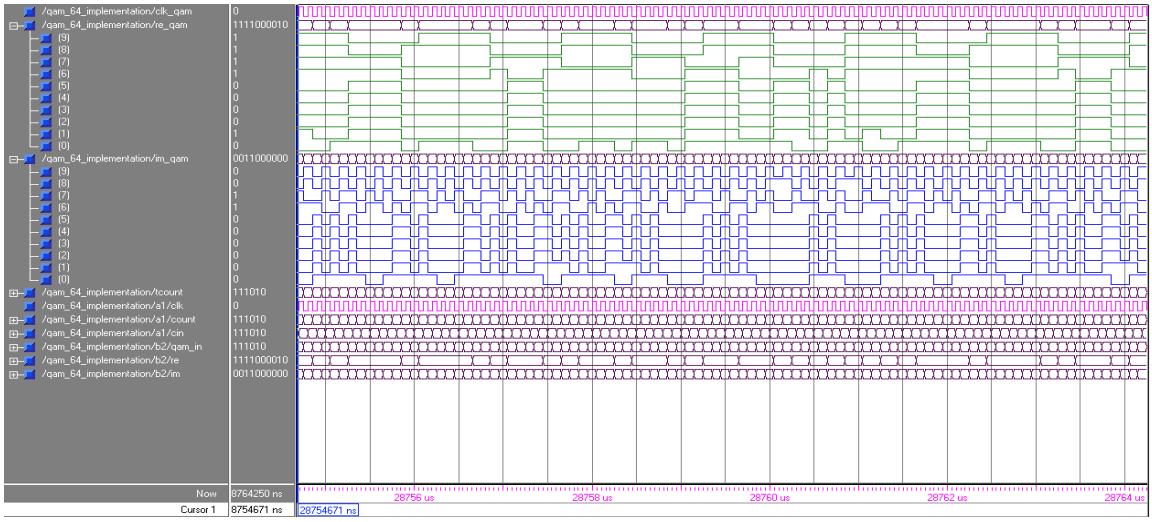


Fig. 4: 64 QAM output using the MODELSIM software

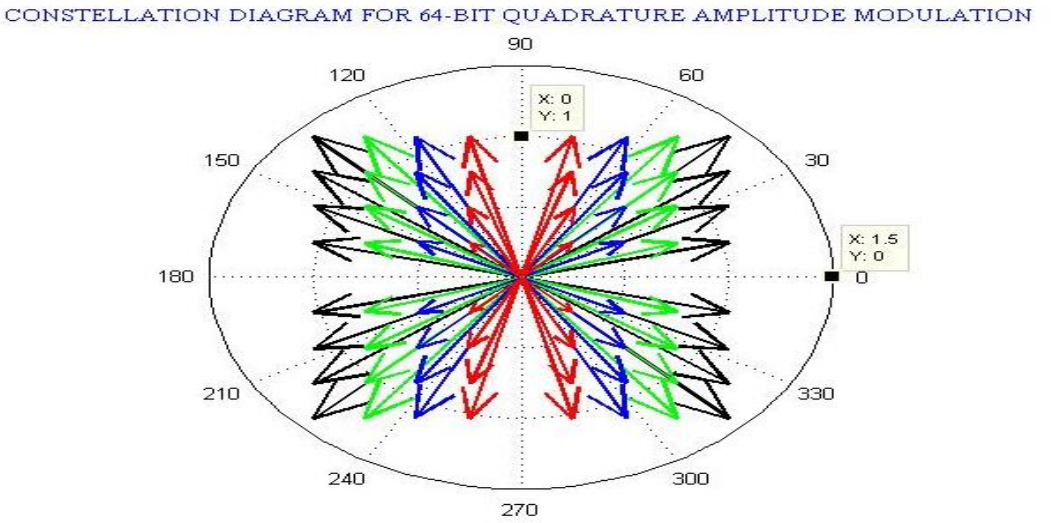


Fig. 5: Constellation plot for the 64 QAM using the MATLAB tool

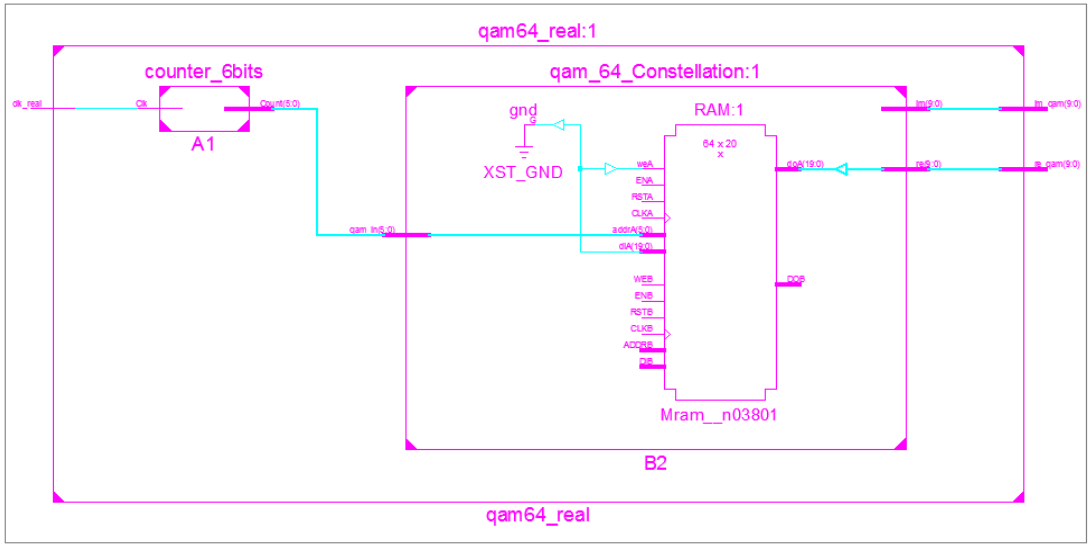


Fig. 6: Detailed RTL view of the 64-QAM using the XILINX ISE 12.1

Table 4: Performance analysis for power, current & temperature using the XILINX SPARTAN 3A DSP

Device	
Family	Spartan3adsp
Part	xc3sd1800a
Package	fg676
Grade	Commercial
Process	Typical
Speed Grade	-4

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

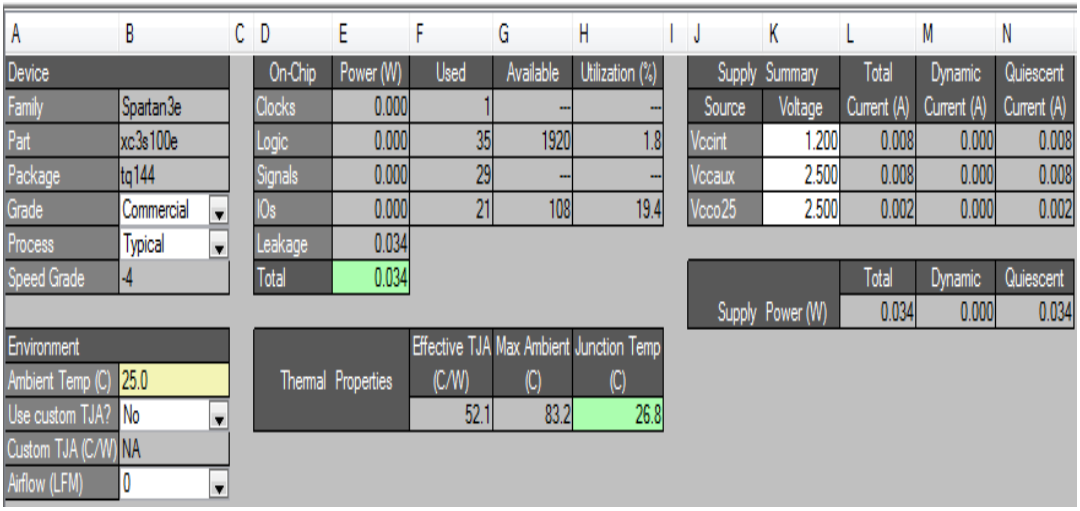
On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.001	1	---	---
Logic	0.000	35	33280	0.1
Signals	0.000	29	---	---
IOs	0.000	21	519	4.0
Leakage	0.114			
Total	0.115			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	15.9	83.2	26.8

Supply Summary Source	Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.200	0.043	0.001	0.042
Vccaux	2.500	0.025	0.000	0.025
Vcco25	2.500	0.000	0.000	0.000

	Total	Dynamic	Quiescent
Supply Power (W)	0.115	0.001	0.114

Table 5: Performance analysis for power, current & temperature using the XILINX SPARTAN 3E



Device	
Family	Spartan3e
Part	xc3s100e
Package	tq144
Grade	Commercial
Process	Typical
Speed Grade	-4

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	--	--
Logic	0.000	35	1920	1.8
Signals	0.000	29	--	--
IOs	0.000	21	108	19.4
Leakage	0.034			
Total	0.034			

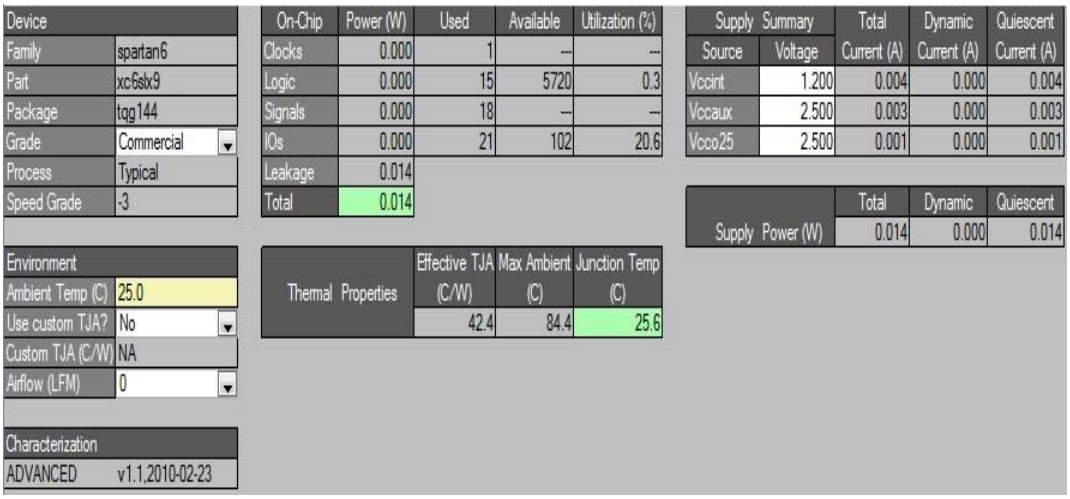
Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.008	0.000	0.008
Vccaux	2.500	0.008	0.000	0.008
Vcco25	2.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.034	0.000	0.034

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	52.1	83.2	26.8

Table 6: Performance analysis for power, current & temperature using the XILINX SPARTAN 6E



Device	
Family	spartan6
Part	xc6slx9
Package	tqg144
Grade	Commercial
Process	Typical
Speed Grade	-3

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	--	--
Logic	0.000	15	5720	0.3
Signals	0.000	18	--	--
IOs	0.000	21	102	20.6
Leakage	0.014			
Total	0.014			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.004	0.000	0.004
Vccaux	2.500	0.003	0.000	0.003
Vcco25	2.500	0.001	0.000	0.001

	Total	Dynamic	Quiescent
Supply Power (W)	0.014	0.000	0.014

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	42.4	84.4	25.6

Characterization	
ADVANCED	v1.1,2010-02-23

Table 7: Device Utilization Chart for the 64-QAM using the XILINX SPARTAN 3A DSP

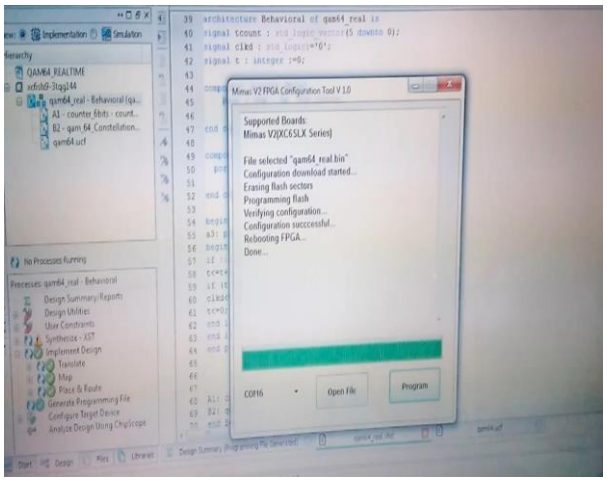
Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	6	33,280	1%
Number of 4 input LUTs	34	33,280	1%
Number of occupied Slices	18	16,640	1%
Number of Slices containing only related logic	18	18	100%
Number of Slices containing unrelated logic	0	18	0%
Total Number of 4 input LUTs	35	33,280	1%
Number used as logic	34		
Number used as a route-thru	1		
Number of bonded IOBs	21	519	4%
Number of BUFGMUXs	1	24	4%
Average Fan-out of Non-Clock Nets	5.69		

Table 8: Device Utilization Chart for the 64-QAM using the XILINX SPARTAN 3E

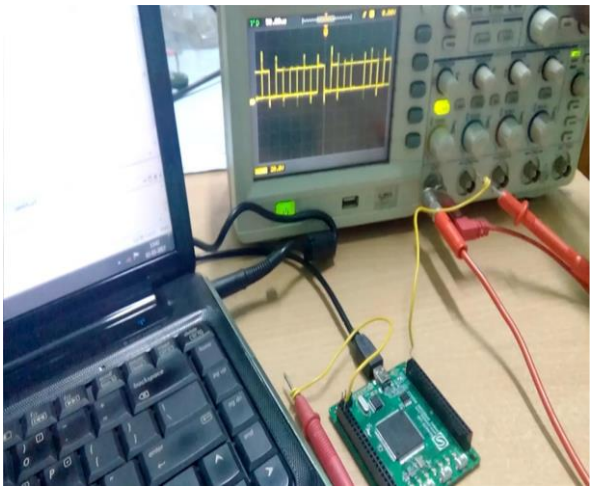
Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	6	1,920	1%
Number of 4 input LUTs	34	1,920	1%
Number of occupied Slices	18	960	1%
Number of Slices containing only related logic	18	18	100%
Number of Slices containing unrelated logic	0	18	0%
Total Number of 4 input LUTs	35	1,920	1%
Number used as logic	34		
Number used as a route-thru	1		
Number of bonded IOBs	21	108	19%
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	5.69		

Table 9: Device Utilization Chart for the 64-QAM using the XILINX SPARTAN 6

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	6	11,440	1%
Number of Slice LUTs	15	5,720	1%
Number of occupied Slices	11	1,430	1%
Number with an unused Flip Flop	9	15	60%
Number of fully used LUT-FF pairs	6	15	40%
Number of slice register sites lost to control set restrictions	2	11,440	1%
Number of bonded IOBs	21	102	20%
Number of BUFG/BUFGMUXs	1	16	6%
Average Fan out of Non-Clock Nets	4.79		



7 (a)



7 (b)

Fig. 7: (a) (b). Experimental setup for the 64-QAM using the XILINX SPARTAN 6E FPGA

Table. 10: Comparison of performance evaluation for the Xilinx Spartan FPGA devices

PARAMETERS	XILINX SPARTAN FPGA DEVICES		
	6E	3E	3A DSP
Total Power	0.014	0.034	0.115
Total Current for Vccint 1.2V	0.004	0.008	0.043
Total Current for Vccaux 2.5V	0.003	0.008	0.025
Total Current for Vcco 2.5V	0.001	0.002	0
Junction Temperature (C)	25.6	26.8	26.8

Table 11: Comparison for Device Utilization for the Xilinx Spartan FPGA family device

DEVICE UTILIZATION	XILINX SPARTAN FPGA DEVICES					
	6E		3E		3A DSP	
Number of Slice Registers	6 out of 11440	1%	6 out of 1920	1%	6 out of 33280	1%
Number of Slice LUTs	15 out of 5720	1%	34 out of 1920	1%	34 out of 33280	1%
Number of occupied Slices	11 out of 1430	1%	18 out of 960	1%	18 out of 16640	1%
Number of LUT Flip Flop pairs used	15 out of 30	50%	35 out of 1920	1%	35 out of 33280	1%
Number of bonded IOBs	21 out of 102	20%	21 out of 108	19%	21 out of 519	4%
Number of BUFG/BUFGMUXs	1 out of 16	6%	1 out of 24	4%	1 out of 24	4%
Average Fan-out of Non-Clock Nets	4.79		5.69		5.69	

4. Conclusion

The design of 64 bit QAM is coded using VHDL and verified by using MODELSIM software. The real time implementation of the 64 QAM is performed with the three XILINX SPARTAN family devices namely 3A DSP, 3E and 6E. The current and power leakages are minimal for XILINX SPARTAN 6E compared to other XILINX SPARTAN FPGA devices. The thermal property of the XILINX SPARTAN 3A DSP FPGA was found to be satisfactory. The device utilization chart proves good for the XILINX SPARTAN 3A DSP FPGA device. Future work could be directed towards the implementation of 64-QAM receiver, 256-QAM and OFDM transceiver.

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