



Area, power and delay efficient 2-bit magnitude comparator using modified gdi technique in tanner 180nm technology

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Abstract

Of late, low power configuration took shape into the most important concentrations in designing the latest VLSI circuits. By considering the same at the maximum priority, another outline of two-bit GDI based Magnitude or Digital Comparator are recommended and actualized with the assistance of Modified GDI transistors. Comparators are building blocks in advanced VLSI configuration circuits. In the current patterns the necessity for occupying less area in chip and low power compact devices. In this paper we introduced another Magnitude Comparator which will utilize low power, and gives a quick results and occupying less chip area in Modified GDI technology. The modified GDI procedure dependent extent comparator has favorable position of less control utilization as for different outline parameters; few on-chip zones secured as small number of transistors are utilized in circuit configuration when related with traditional CMOS size comparator. Either of the circuits is outlined and executed utilizing Tanner EDA Tool version 16.0 at 180nm processing technologies.

Keywords: GDI (Gate Diffusion Input), Modified or Updated GDI technique, Magnitude Comparator;

1. Introduction

The designing of a circuit depends upon three major factors namely less power, more speed and few on chip area for an efficient performance and better marketing of the product .So a wide angle researches is going on in embedded systems because for low power utilization and high speed performance of the system utilized as a part of mobiles, tablets and so forth has prompted scale down technology to Nano regime, permit to actualize huge usefulness on one chip.

A Magnitude Comparator is a device which is used to compare 2 n-bit values and the comparison is takes place in three types one $A > b$, another one is $A = b$ and the last is $A < B$ those are shown in Fig1.this comparator is used in chip development where the comparison application takes place like arithmetic operation, in MCU IDE software instructions like MOV, JUMP, SJUMP, LJUMP, ACALL and COM these instructions uses the comparison technique to access the data in a memory. Comparator also used in a Digital Signal processing for handling of data. Some of the live examples of Digital or Magnitude Comparator includes in CMOS 4063, 4085 and TTL 74682 and 7485

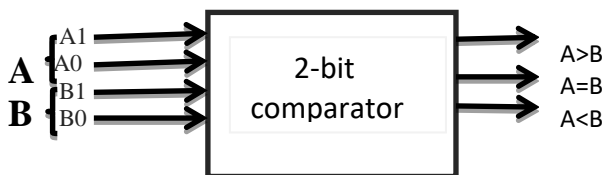


Fig. 1: 2-bit Magnitude Comparator block diagram

Figure 1 shows about the block diagram of 2-bit magnitude comparator and the input is A and B for which each input contains

2 bits for A and B and the outputs are three i.e. F1, F2 and F3. The internal functioning or processing of the circuit in block diagram is as follows F1 is equals to $A > B$, F2 is equals to $A = B$ and F3 is equals to $A < B$. The functioning of circuit can be identified by using truth table that is shown in the Table1. The inputs are A0, A1 and B0, B1 which provided 0 to 16 bits for input to analysis of output that will provide

the circuit analysis. Customarily Two-bit comparator will be executed with sixty six transistors utilizing complementary-MOS logic.

The basic function of the comparator is to compare two n-bit numbers and determine the output based on the comparison results. The output results can be anything of the three possible outcomes i.e., whether and which number is greater then, equal to or less then. The output of the compared is represented through a 3 binary variables those indicates either of A greater than B, A equals to B, or A less than B.

Table 1: Magnitude Comparator Truth Table

A1	A0	B1	B0	F3	F2	F1
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

$$F1=A1B1'+A0B1'B0'+A1A0B0' \rightarrow (1)$$

$$F2=(A0B0+A0'B0')(A1'B1'+A1B1) \rightarrow (2)$$

$$F3=A1'B1+A01B0 (A1'+B1) \rightarrow (3)$$

Now in section 2 it describes the existed GDI Magnitude Comparator and conventional CMOS comparator, the sec 3 Describes about the Modified or updated GDI technique that is proposed in this paper and the sec 4 describes about the final outputs of Proposed Comparator.

2. Existing Comparators

A. The Conventional CMOS Magnitude Comparator

Logical Functions for the magnitude comparator are also been acknowledged customarily utilizing sixty six transistors as appeared in Figure 1.2 As for the utilizes more no. of transistors it involves more territory and more Power Dissemination takes place.

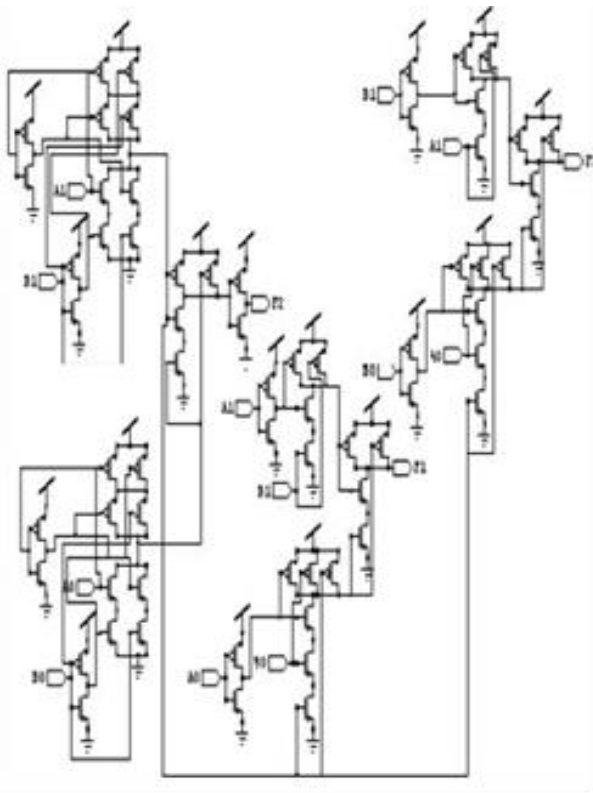


Fig. 2: Block diagram of a 2-bit Magnitude Comparator

B. Existed GDI Magnitude Comparator

A primary GDI cell consists of 4 terminals –

1. G → Common input for the transistors NMOS and PMOS.
2. P → Outer dissemination hub for the transistor PMOS.
3. N → External dispersion hub for the transistor NMOS and
4. D hub → Diffusion contact for the both transistors.

P, N and D can be utilized either as input or output ports, contingent upon the circuit design. GDI empowers simpler gates. Bringing down the number of transistors increases the execution speed and decreases the power dissipation compared to that of standard CMOS and Pass-Transistor logic procedures

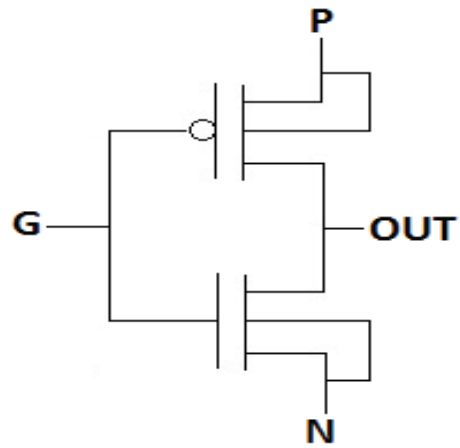


Fig. 3: Basic GDI Cell

A large variety of combinational capacities can also be executed with just 2 MOS transistors using Gate diffusion input (GDI). Points of interest in GDI method are high through output. Decreased control utilization and fewer zones as this method diminish the transistor check. In GDI essential cell looks like a fundamental Complimentary-MOS inverter. P,N &G are consider as contributions for the GDI cell.

Table 2: The logic functions that are obtained using single GDI cell

N	P	G	D	Function
0	B	A	HB	F1
B	1	A	H+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	HB+AC	MUX
0	1	A	H	NOT

In comparison to other logic designs that are designed by utilizing CMOS, Accessing of gates in GDI technique is worthwhile with fast performances or even low power usage of circuit and less taking of chip area.

The figure shown in below is a 2-bit magnitude comparator using GDI technology with utilization of 30 transistors in the circuit as shown in Fig 4.

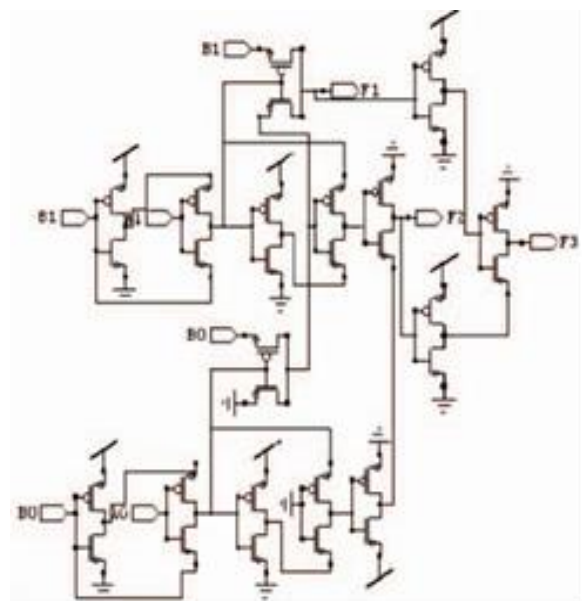


Fig. 4: GDI cell

The GDI method for implementation of circuit takes low power, less area and less delay compare to the existing methods like CMOS technology and Pass Gate NMOS technology for implantation of the circuits in chip designing.

3. Techniques Proposed for Comparator Circuit Design

3.1. Modified or Updated Technique

In spite of having many advantages with GDI, its execution is delayed when utilized less than 90 nm. Fundamental GDI experiences some pragmatic restrictions like Swing Corruption. Complexity for fabrication is more in standard CMOS Process. To overcome this problem, we preferred the Modified GDI technology. In Modified GDI, Terminals in substrate for PMOS and NMOS are associated with GND and VDD respectively as appeared in Figure.5

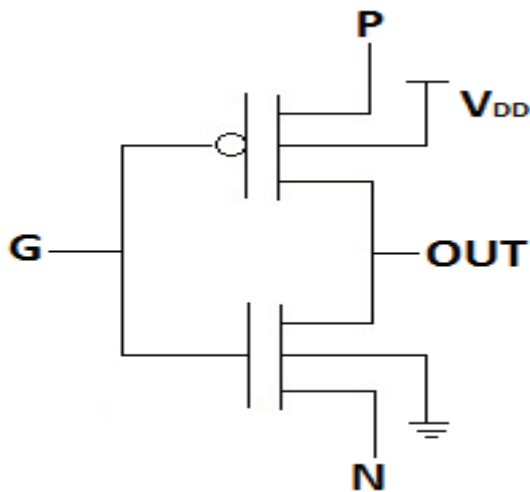


Fig. 5: Basic Modified GDI Cell

The CMOS fabrication Process supports modified GDI. Leakage streams can be perceived in sub-threshold advancements. When compared to static CMOS process Modified or Updated GDI Provides extensive decrease of both sub-limit and leakage current for gate.

3.2. Operational Analysis

Table 3: The Operational analysis of Basic Modified GDI cell.

N	P	G	OUT	FUNCTION
B	A	A	AB	AND
B	A	B	A+B	OR
B	A	Sel	SelA+SelB	MUX

3.3. Implementation of 2-bit magnitude comparator

Area, delay and power efficient area simple architecture using 18 transistors to create 2-bit magnitude comparator.

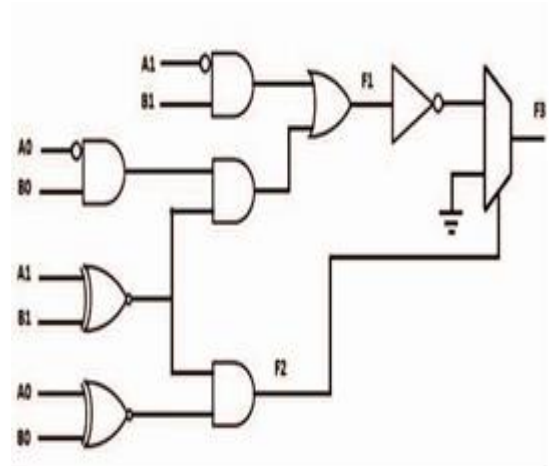


Fig. 6: Gate level design of proposed new 2-bit magnitude comparator.

4. Results

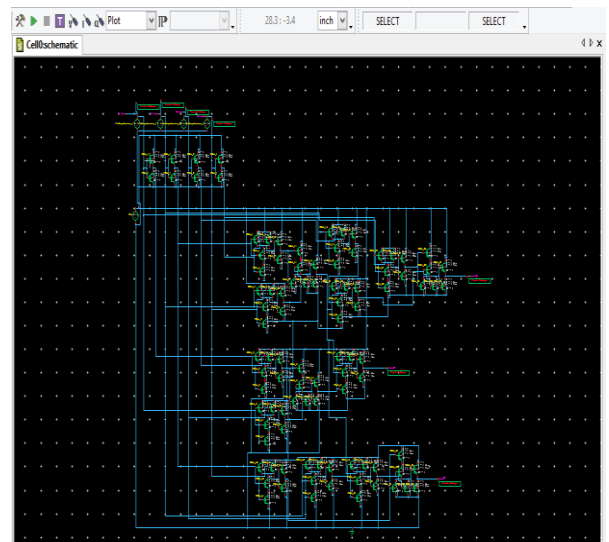


Fig. 7: Transistor level of CMOS Magnitude Comparator

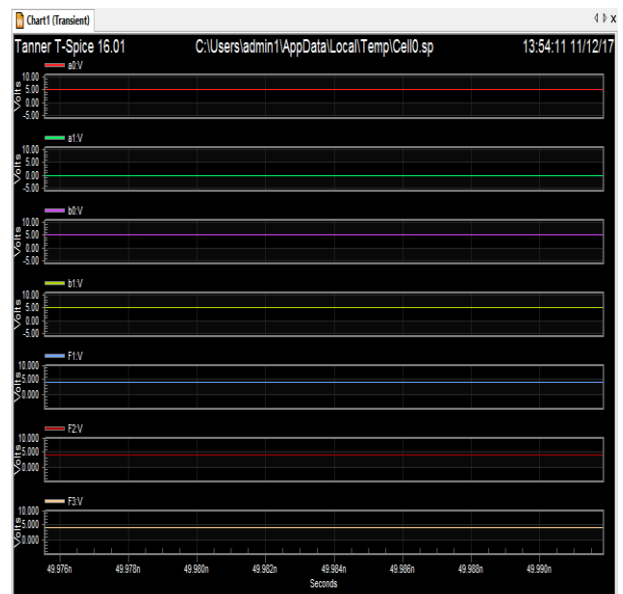


Fig. 8: CMOS Magnitude comparator waveforms

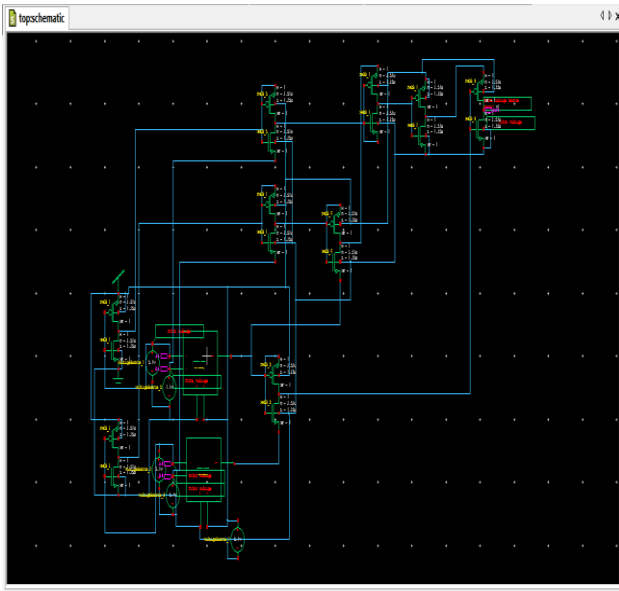


Fig. 9: Modified GDI magnitude comparator

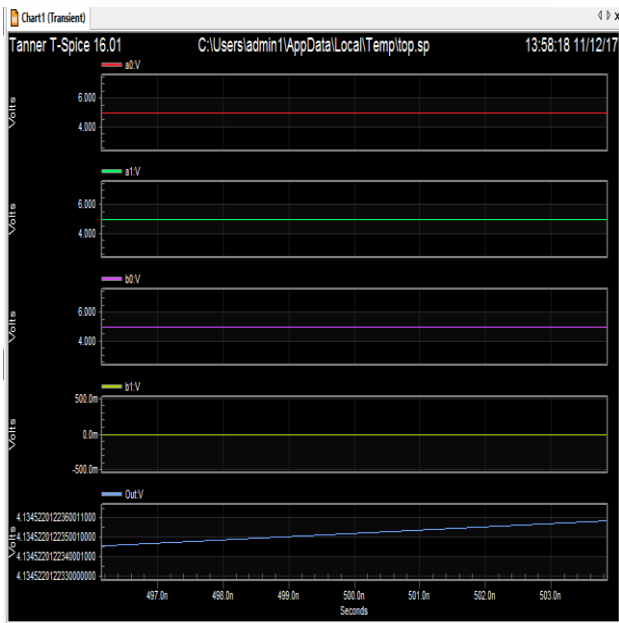


Fig. 10: Modified GDI Magnitude Comparator

TECHNOLOGY	AREA	POWER	DELAY
CMOS	98(Transistors)	1.76 μ Watts	0.44sec
MODIFIED GDI	34(Transistors)	0.612 μ Watts	0.02sec

Fig. 11: Comparison of Results

Simulated status

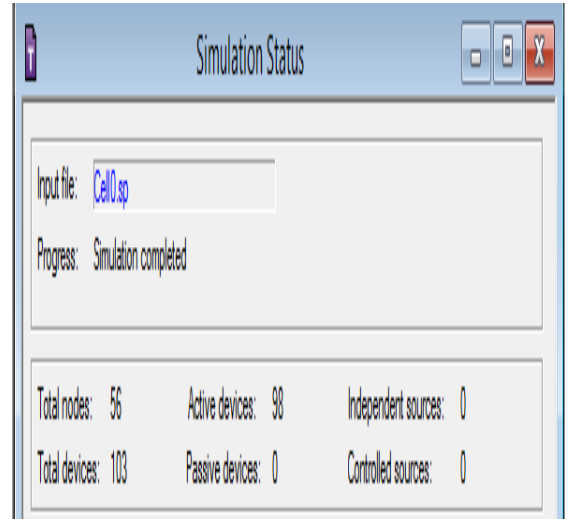


Fig. 12: CMOS magnitude Comparator

Simulation of two bit Magnitude comparator is done in two different techniques those techniques are simulated in Tanner EDA software and results are displayed as screen shots in fig.7,8,9 and 10 the circuits implemented in CMOS technology shown in Fig.7 and another circuit implemented using enhanced or modified GDI technique shown in Fig.9.

For the implementation of two circuits we have got zero threads and the DC operating point for CMOS Magnitude comparator is 0.73 seconds and for enhanced GDI Magnitude comparator is 0.03 seconds this results shows that enhanced GDI gives a quick response than the CMOS Magnitude Comparator. The comparison of results for both implemented circuits are shown in Fig.11 as a tabular column comparison takes place in three factors i.e. power ,delay and area these analysis gives a better understand that Enhanced GDI is better than the CMOS technology.

5. Conclusions

The use of electronic devices increasing day by day in life so the new electronic devices are introducing in the market for the user need as the usage is more the customers are looking for fast response, low power utilization and less area of devices these three needs are done by introducing new techniques to designing of chip inside the electronic devices. So many designing methods are existing to create a circuit but we have introduced a one technique named as modified or updated GDI technology for development of comparator circuit, we simulated the circuit in Tanner EDA software and the results are obtained. With those results we identified that modified or Updated GDI Technology of magnitude comparator circuit takes low power, less delay time and takes less area compared to the circuit implemented in CMOS technique.

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